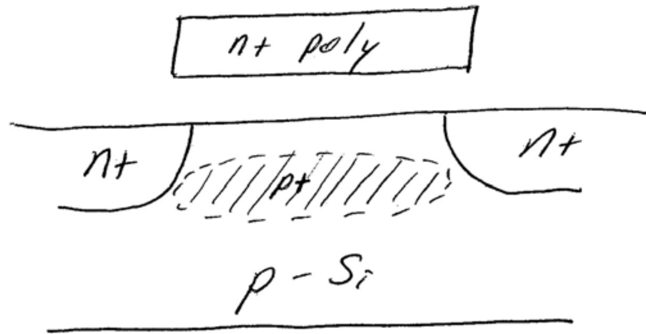
Homework # 7

EE 3161 - Spring 2008

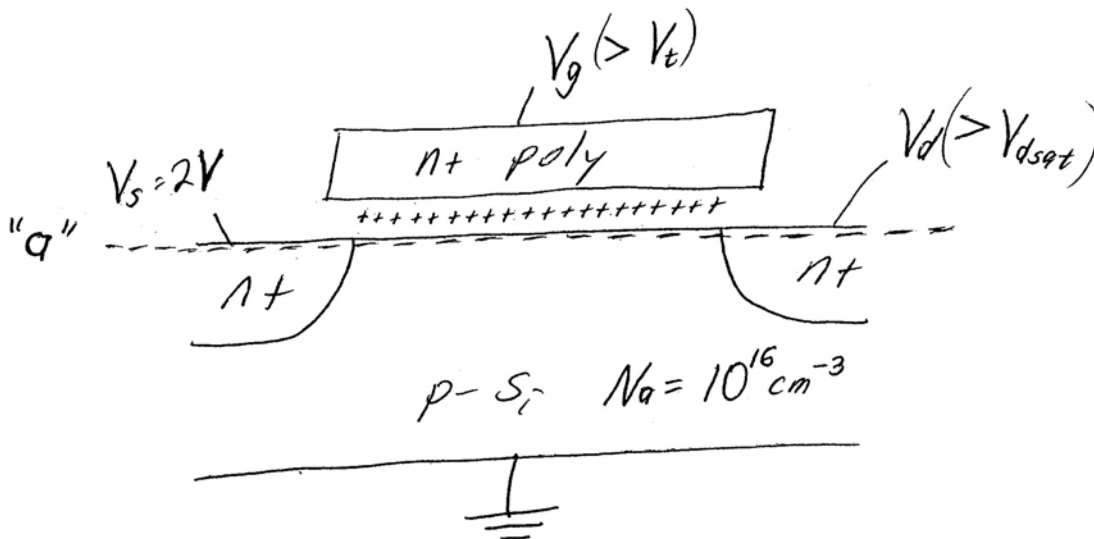
Due Friday, May 9 in class

1) A common procedure in MOS transistor fabrication is to place an implant beneath the surface of the silicon; this is called a punchthrough implant because it prevents subsurface punchthrough. Using the figure below, sketch the C-V curve on the same set of axes for the MOSFET before and after the implant. How does the implant affect the channel mobility, the flat band voltage, the maximum depletion width, and the threshold voltage?



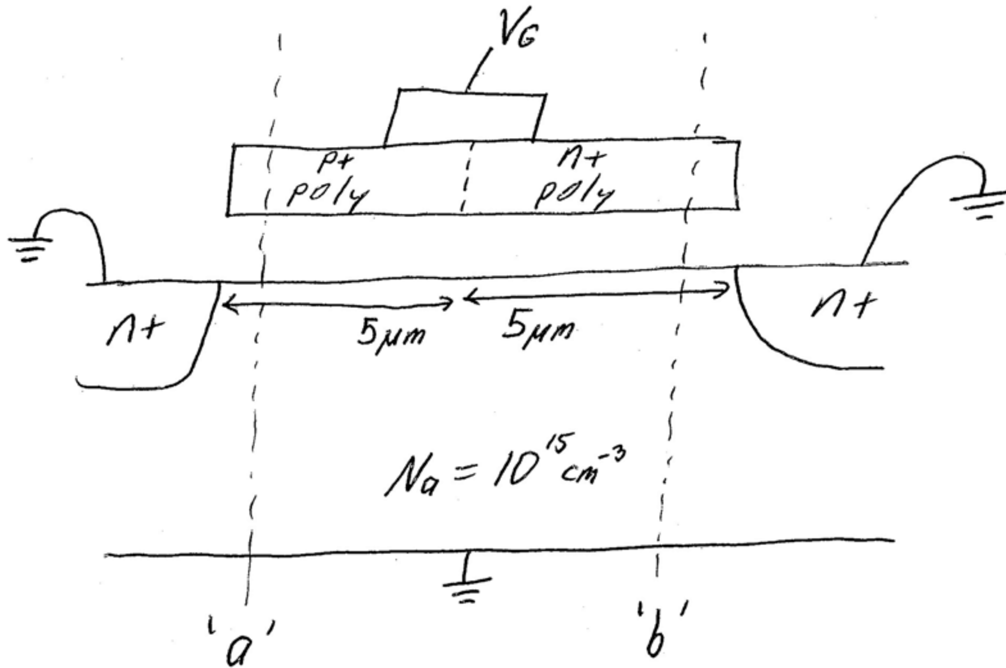
2) In the following MOSFET, let Z = L = 5μm. The polysilicon Fermi level is 0.1eV above the conduction band edge. T_{ox} = 300Å and $\overline{\mu}_n$ = 550 cm^2/V-s. There is a fixed oxide charge of $Q_f = 2\times10^{-8}$ Coulombs/cm^2 positioned midway between the gate and the substrate.

a) What is V_{FB}?
b) What is V_T?
c) Using the square law and V_g = 5V, what is $I_{D\ sat}$?
d) Plot the C-V curve and numerically label the important points. Qualitatively, how does the curve shift if the substrate and poly dopings are switched from n to p and vice versa?
e) Sketch a band diagram along the "channel" (the dotted line "a") for the device if V_g = 0V. Numerically label the band offsets.



3) For the MOSFET drawn below, the left hand side of the polysilicon gate is doped p^+ while the right hand side of the gate is doped n^+. Assume that the p^+ gate has $E_f = E_v$ and that the n^+ gate has $E_f = E_c$. The transistor width Z = 10 microns. The electron affinity for silicon is $\chi = 4.05$ eV. The thickness of the oxide is 300Å.

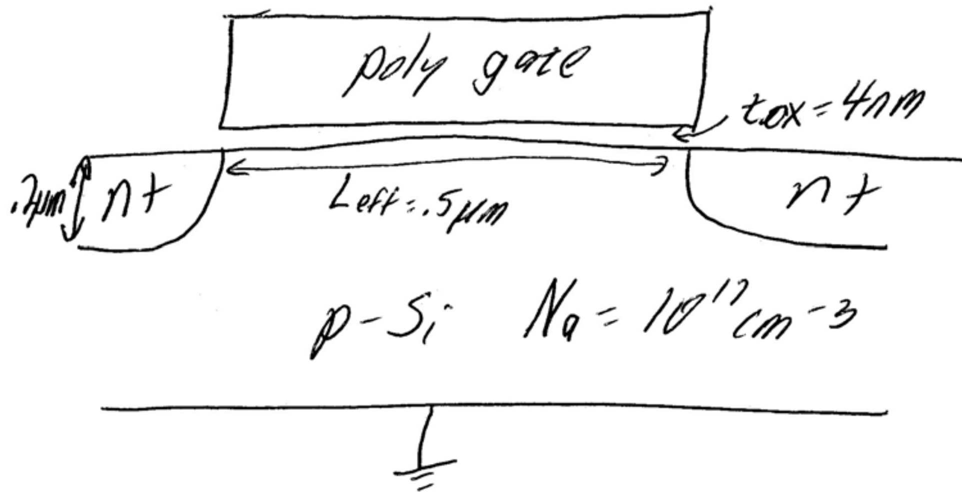
a) Find C_{ox}.
b) What are the flatband voltages at positions "a" and "b"?
c) What are the threshold voltages at positions "a" and "b"?
d) What is the threshold depletion width of the substrate?
e) Draw a C-V curve for the structure assuming that the AC measurement frequency is 1MHz. Label the key voltages and capacitances with calculated numbers.



4) [*Problem 1, final exam, spring 2007*]
A MOSFET is shown below (see next page). The gate length and width of the device are 0.5μm. The channel and bulk doping is 10^{17} cm^{-3} and the gate oxide thickness is 4nm. The depth of the n^+ implants is 0.2μm. Assume there are no oxide charges or interface states. The gate is polysilicon, doped such that $E_f - E_c = 0.2$eV.

a) Do short channel effects impact this device? Why or why not?
b) What is the threshold voltage for small V_d? What does this tell you about the device?
c) Using the square law, what is the drive current for $V_g = 1$V and $V_d = 3$V? (You will need to guess and explain a mobility value; use physical intuition to get a ballpark number, not equations.)
d) Let's say we replace the channel region by strained silicon (which has a higher mobility than normal Si) and the gate dielectric by hafnium dioxide (which has a higher dielectric constant than SiO_2). Qualitatively, which of these two changes will have the biggest impact on threshold voltage if all dopings, lengths, thicknesses, etc. are kept the same? Be sure to state your reasoning and any equations or graphs that support it.

e) Sketch a C-V curve of: i) the MOSFET of parts a) – c), and ii) the MOSFET of part d). Sketch both C-V plots on the same axes and label V_{fb}, V_t, C_{ox}, and C_{min} for the MOSFET of parts a) – c).



5) [*Problem 3, final exam, spring 2007*]
A structure that has been used in the past to minimize hot carrier effects in MOSFETs is called a "Lightly Doped Drain" or LDD MOS, as shown below. In the diagram, n^- means a low-doped n region. Recall from our discussion in class that hot carriers are usually electrons that have been accelerated to high energies by the electric field in the MOSFET.

a) Why do you think the LDD structure reduces hot carriers? Show any graphs or equations that might support your argument.
b) An interesting feature of LDD MOSFETs is that the effective channel length, L_{eff}, seems to increase when high gate voltages are used to drive the device. Why would this be?