A Switched Decoupling Capacitor Circuit for On-Chip Supply Resonance Damping

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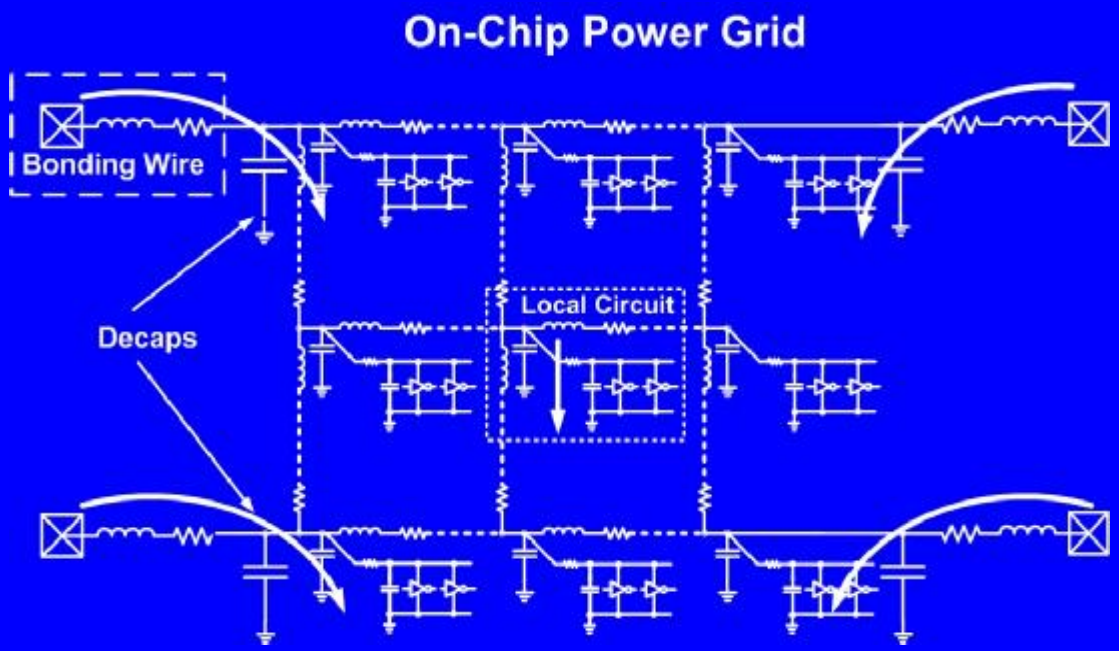
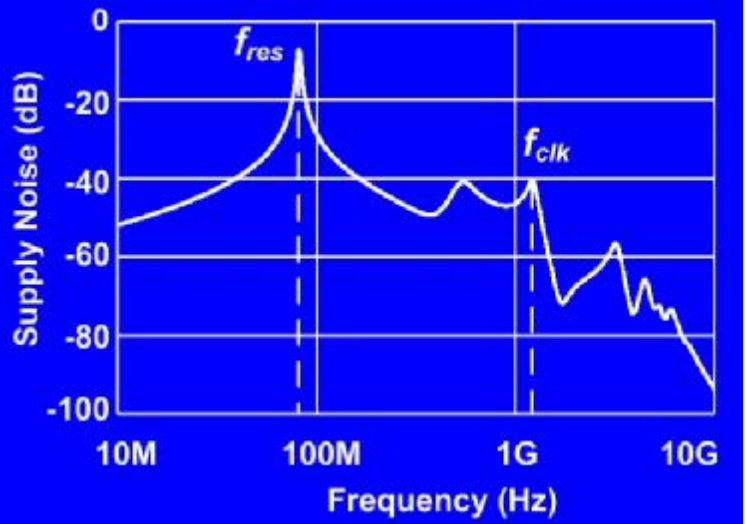
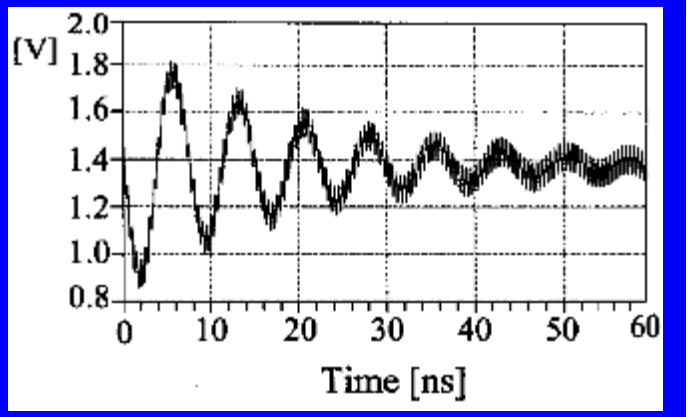
Outline

- Introduction to resonant supply noise
- Proposed switched decap circuit
- Simulated supply noise suppression
- Test chip implementation
- Supply noise measurement results
- Conclusion

IC Power Supply: Underdamped RLC Network





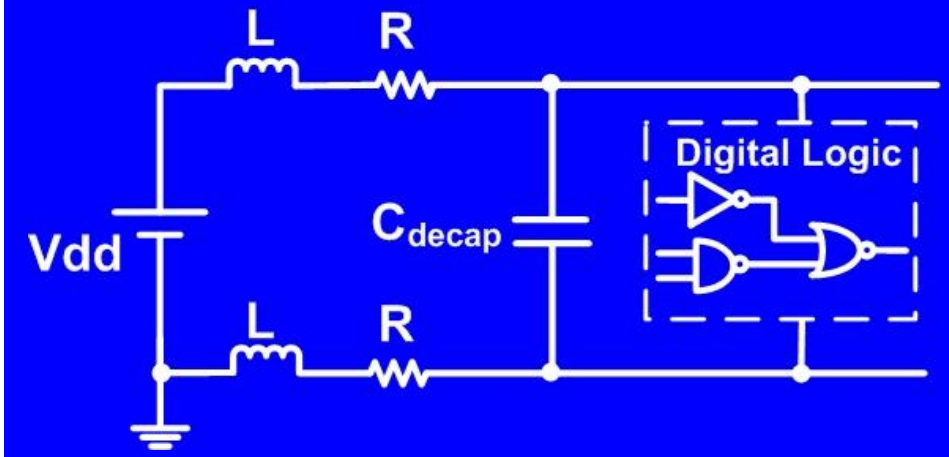


N. Na, IBM, ECTC 2004

- Resonant noise exhibits large magnitude and long duration
- Causes timing violation, clock skew and reliability issue
- Excited by μP loop operation or sudden current spike

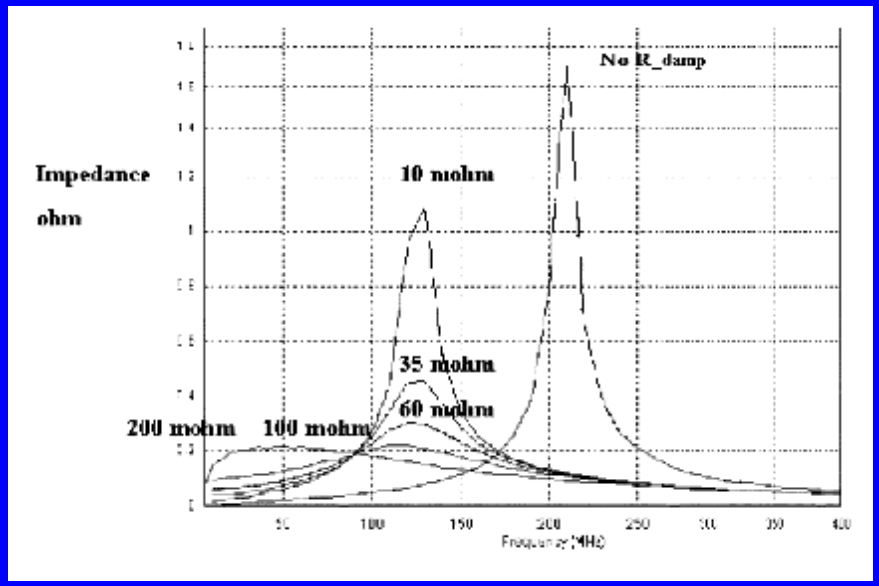
Previous Passive Damping Techniques

Add on-chip decap



$$Q = \frac{1}{R_{wire}} \bullet \sqrt{\frac{L}{C}}$$

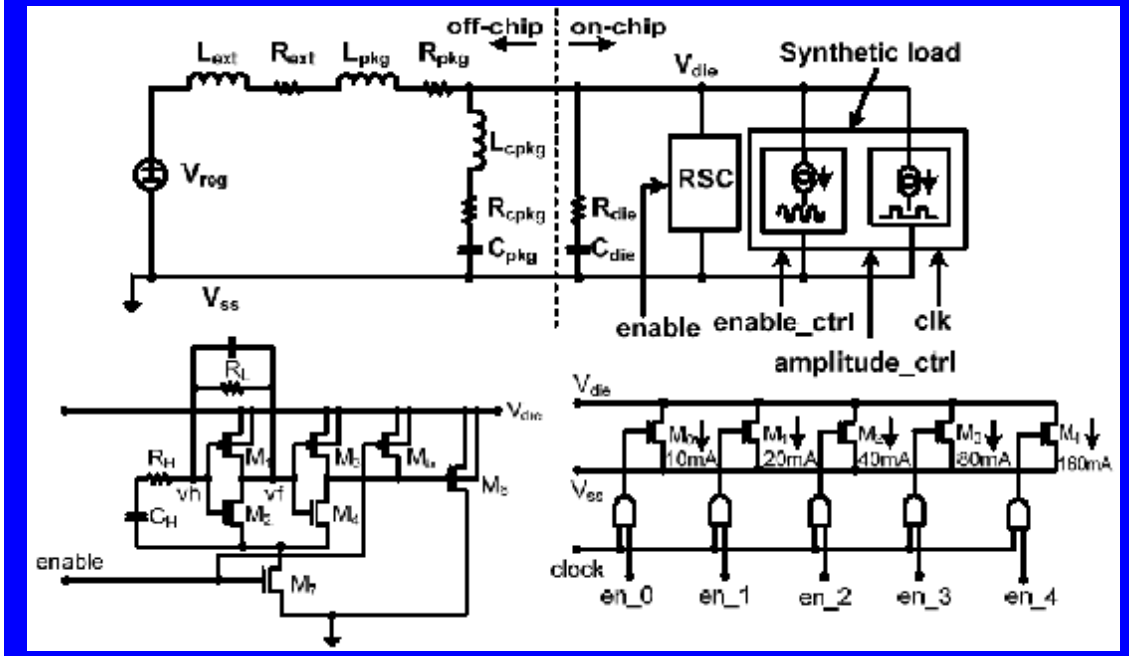
Add on-chip resistance

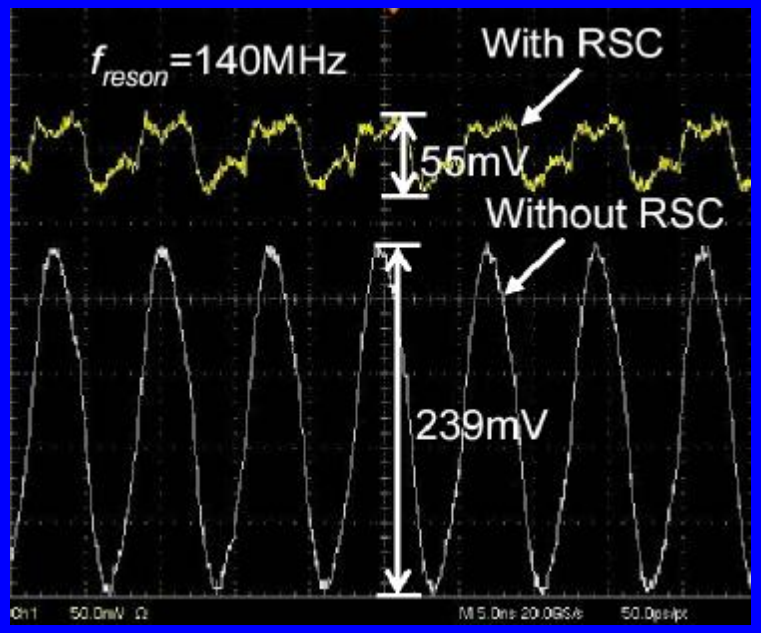


G. Ji, et al., Intel, T. Adv. Packaging, 2005

- Increase R and C to bring down the Q factor
- Decap consumes large area and gate leakage
- Resistive damping worsens IR drop

Previous Active Damping Techniques

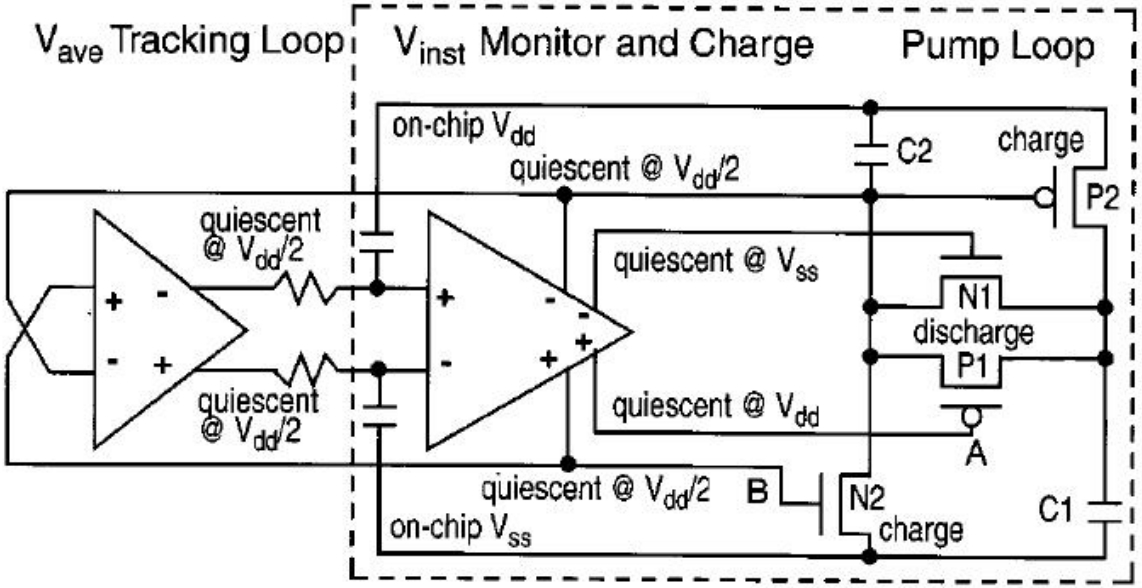


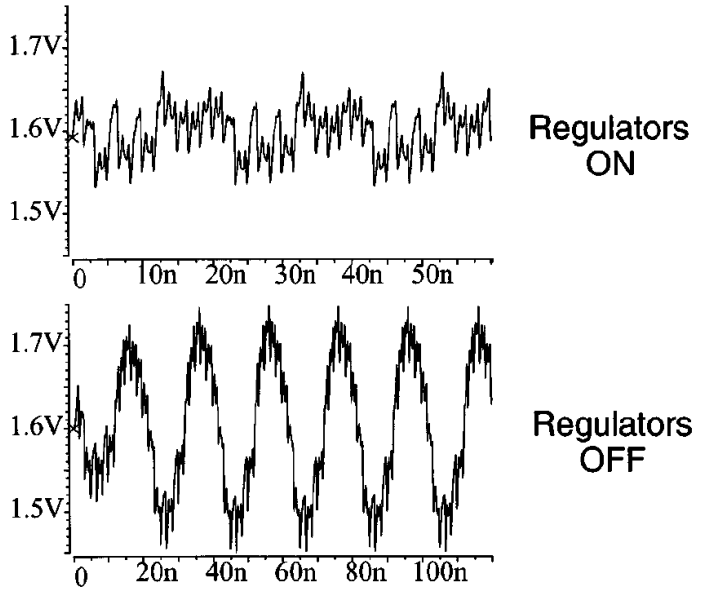


J. Xu et al., Intel, ISSCC 2007

- Detect resonant noise and clamp the overshoot
- 1mA static current per 3mA load
- Hard to control trip points under PVT variation
- Only compensates voltage overshoot

Previous Active Damping Techniques

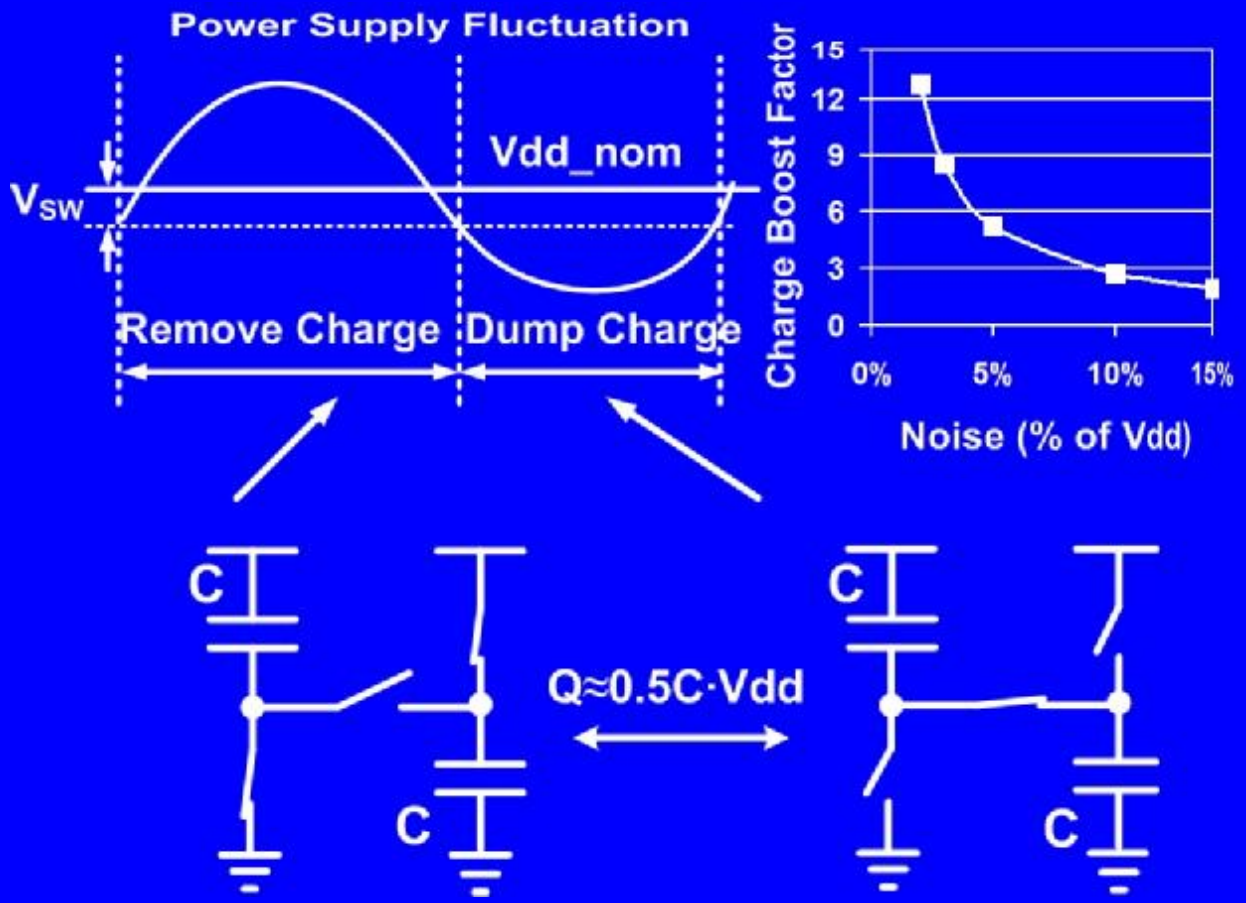




M. Ang et al., Sun Microsystems, ISSCC 2000

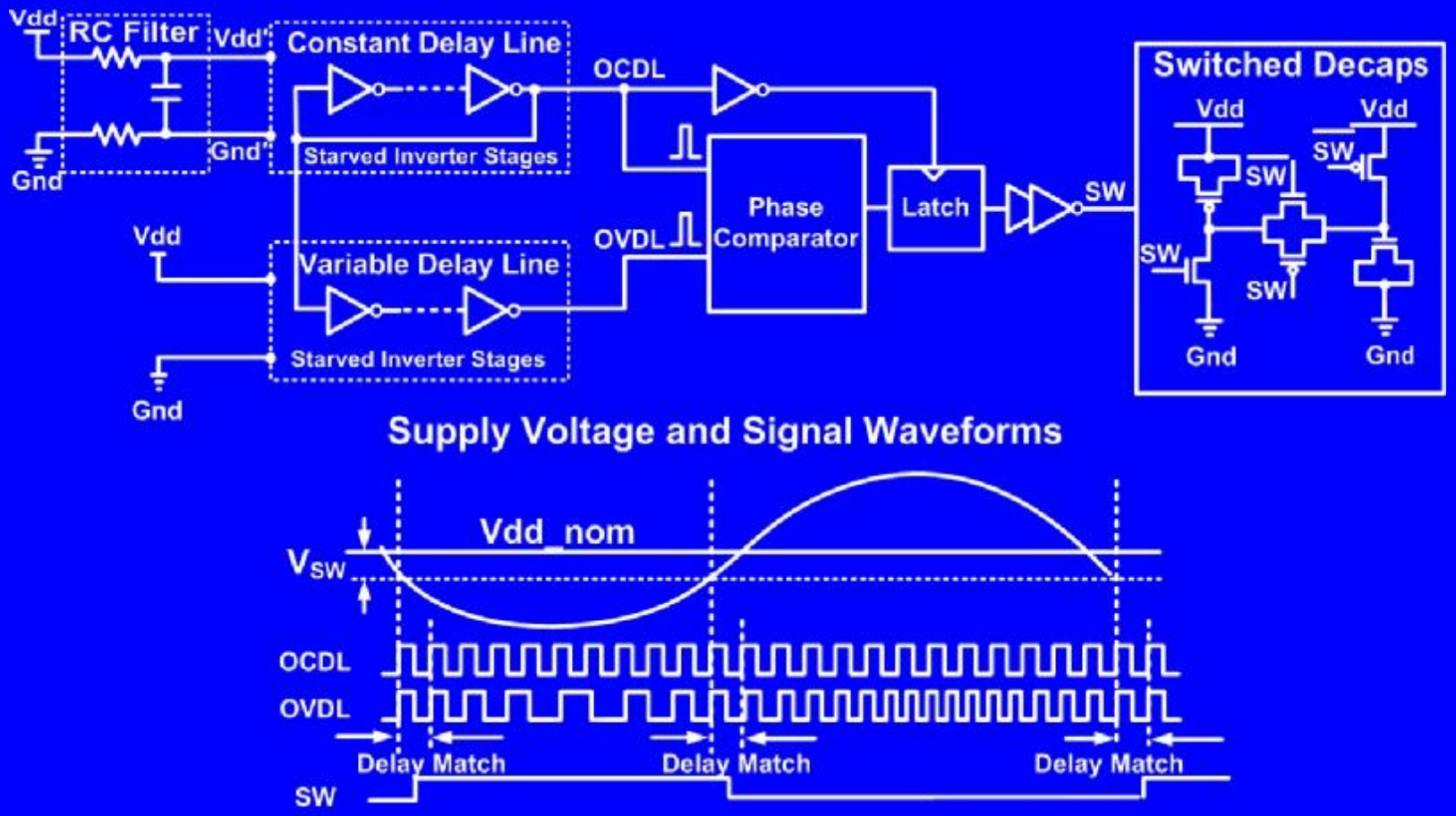
- Switching decaps to boost the total charge
- 5mA quiescent current per regulator
- Limited swing and PVT sensitivity in opamp

Principle of Switched Decap Circuit



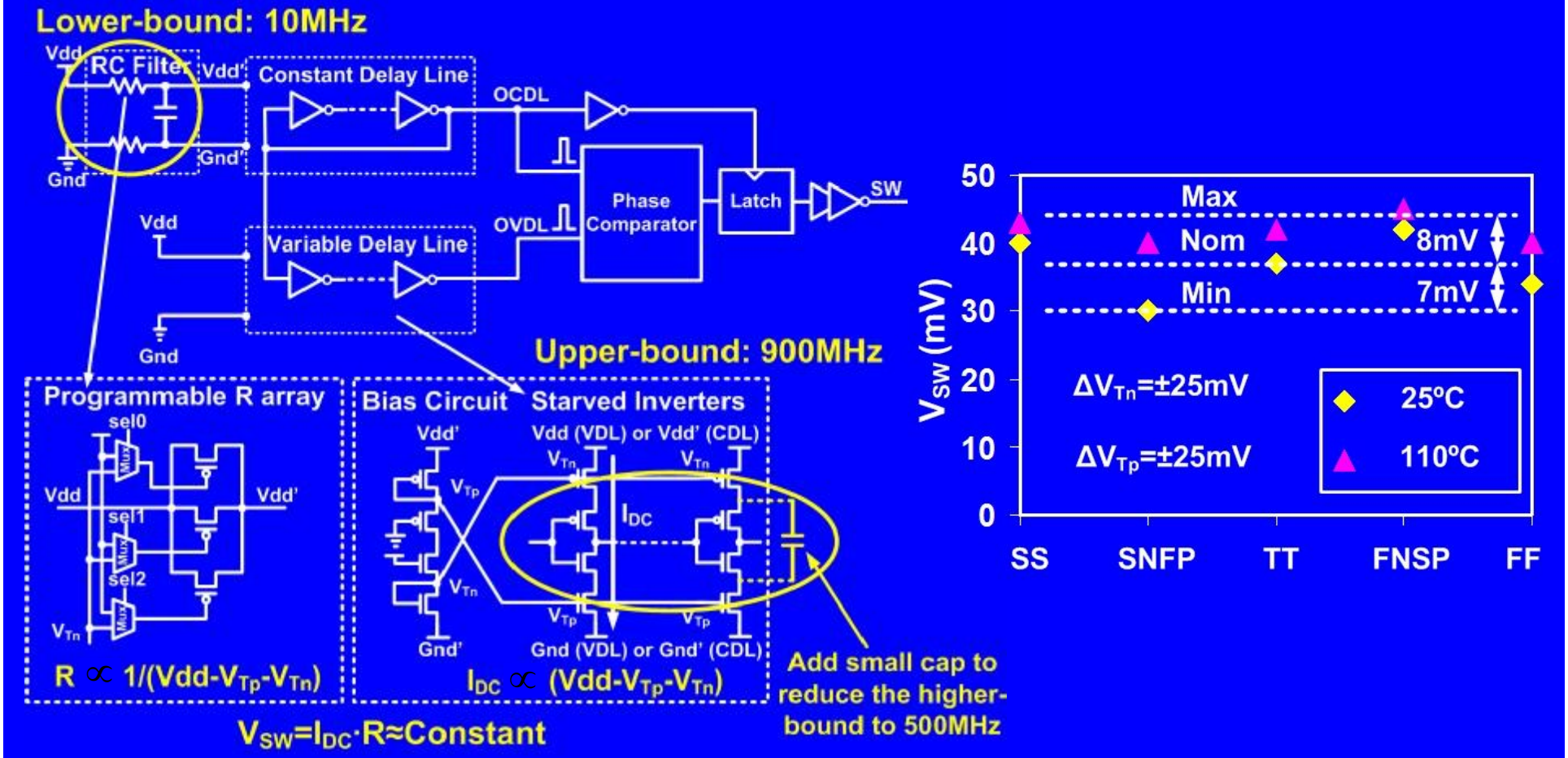
- $Q_{swdecap}=0.5C\cdot V_{dd}+C\cdot\Delta V_{dd}/2$
- $Q_{pdecap}=2C\cdot\Delta V_{dd}$
- 5−13X charge boosting factor (i.e. $Q_{swdecap}/Q_{pdecap}$)

Proposed Digital Switched Decap



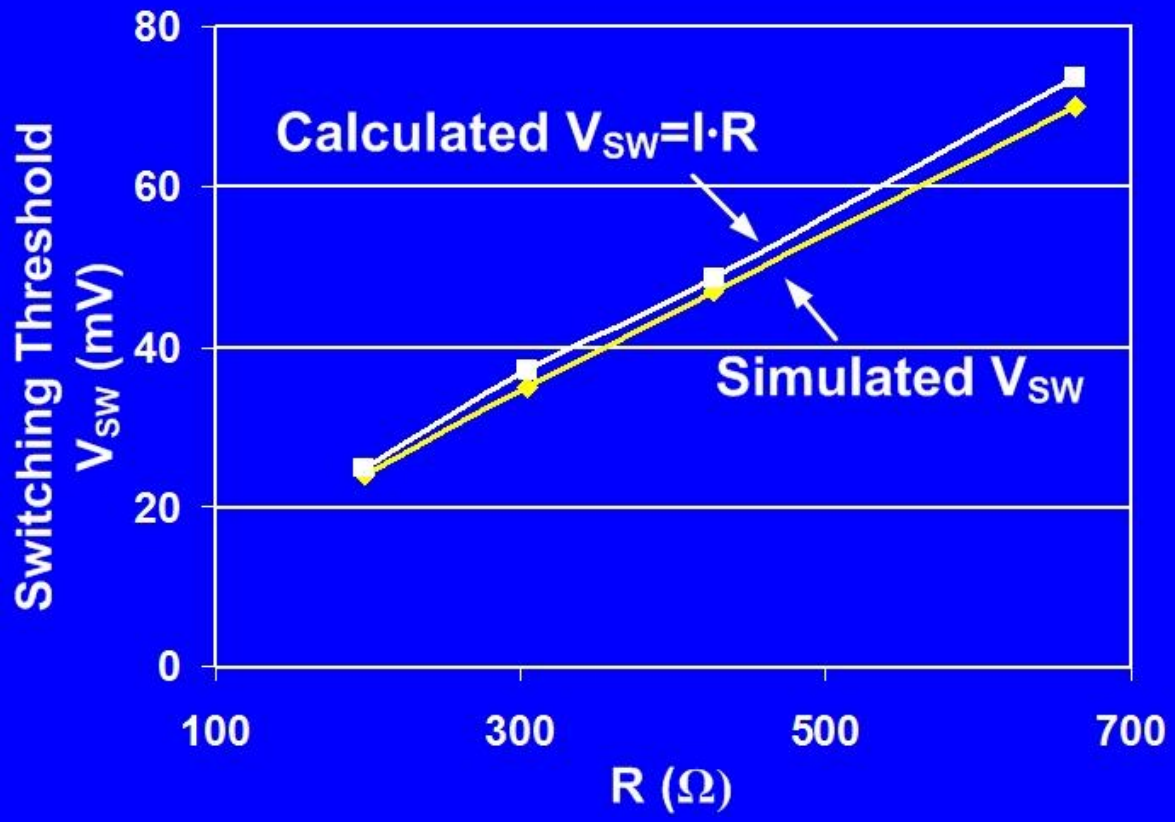
- Digital resonant detection circuit
  - Simple implementation for digital ICs
  - Low static power
- Programmable V_{SW}, PVT insensitive design

Bandpass and PVT Insensitive Design



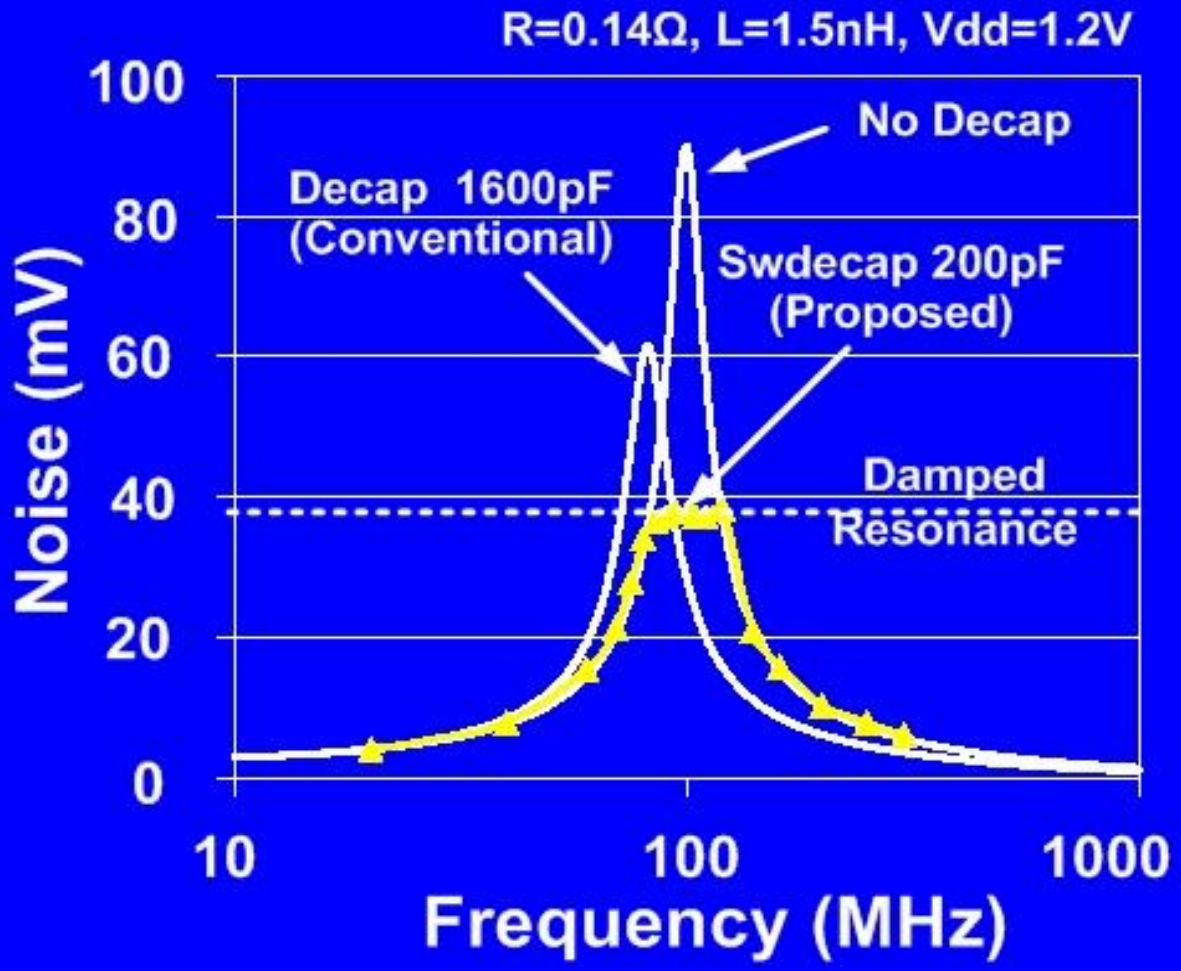
- RC circuit & delay line realize bandpass filter
- 8mV worst-case V_{sw} variation

Adjustability of Switching Threshold V_{sw}



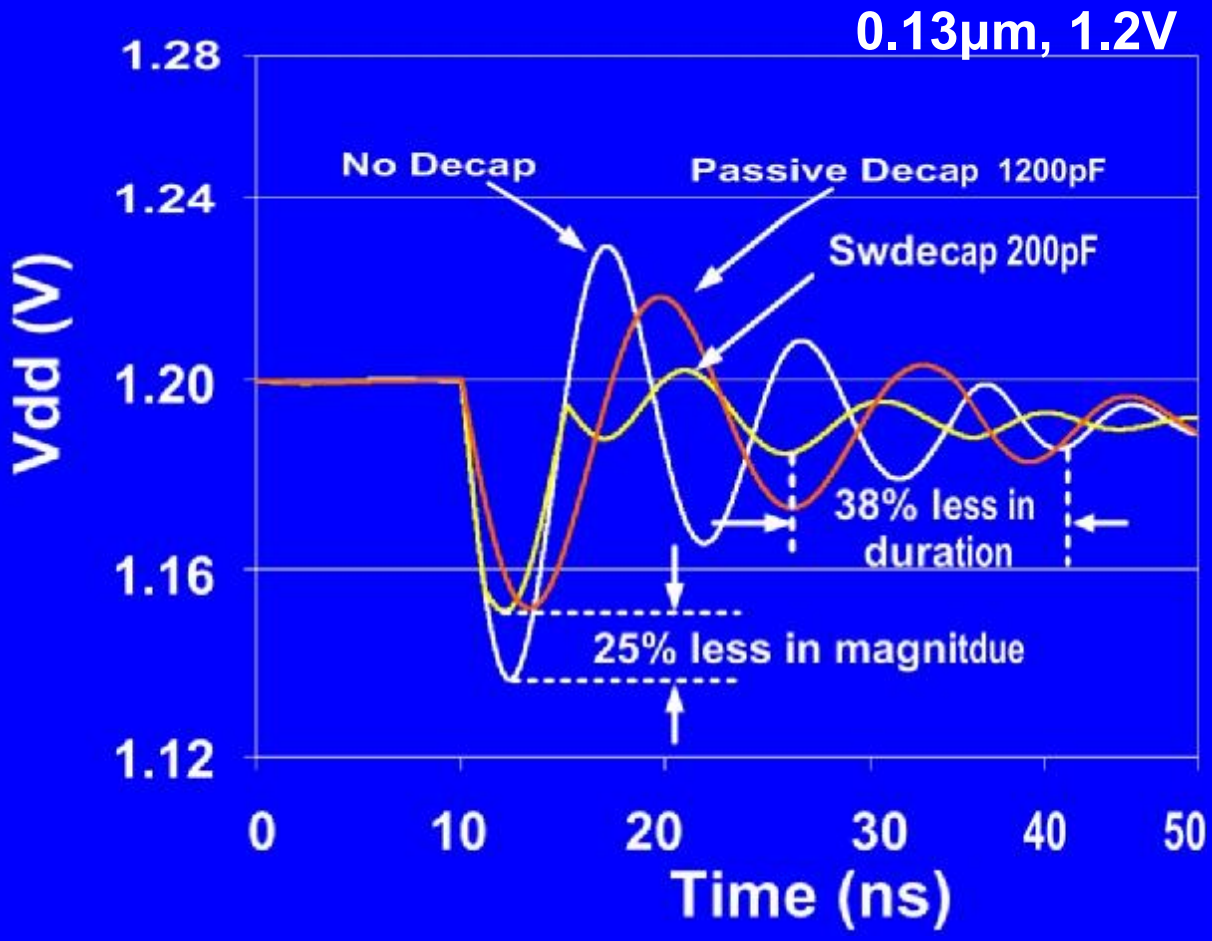
- V_{sw} can be adjusted to avoid unnecessary switching
- V_{sw} is approximately proportional to R value
- R implemented using a programmable MOSFET array

Simulated Switched Decap Performance



- Resonance is suppressed by 7dB
- More than 8X decap boost for resonant damping

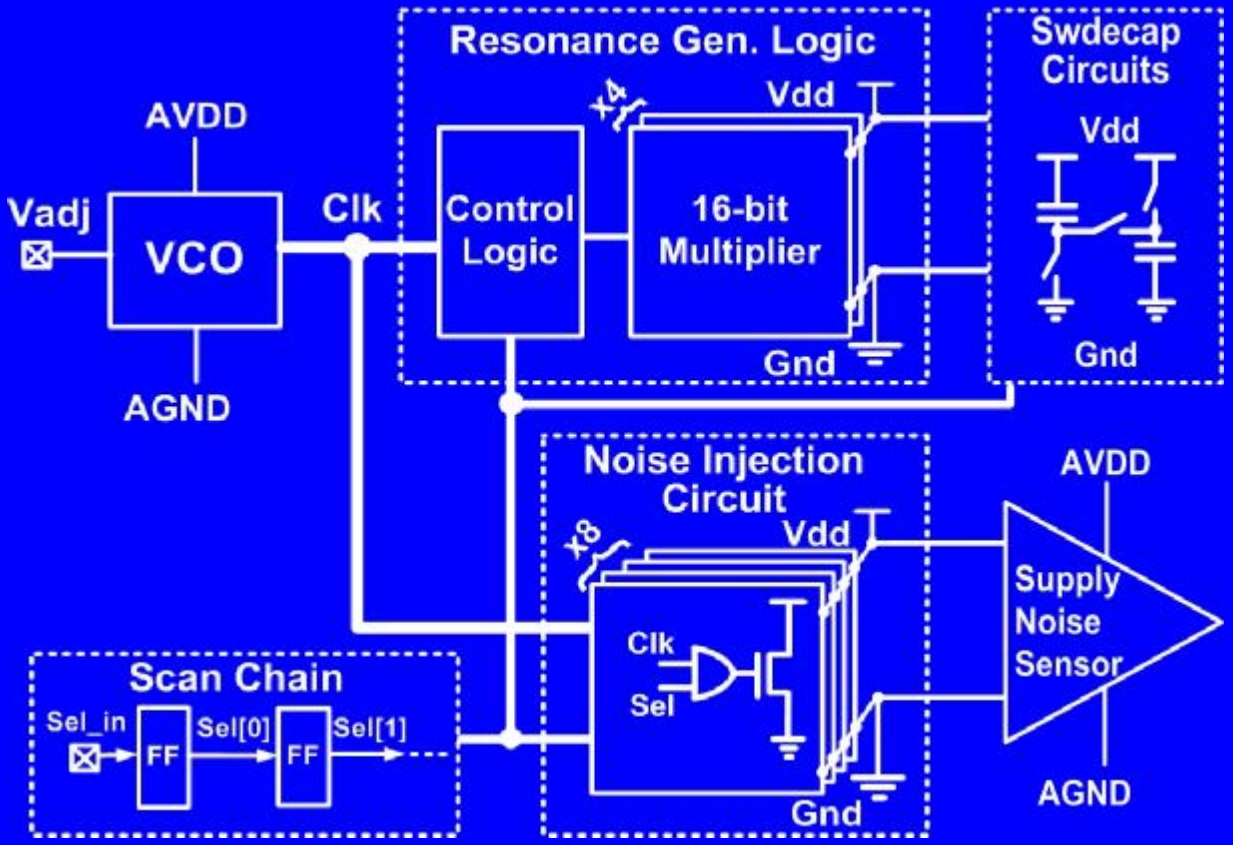
Simulated First-droop Regulation



- Both magnitude and oscillation time are reduced for first-droop noise
- 6X+ decap boost compared with passive decap

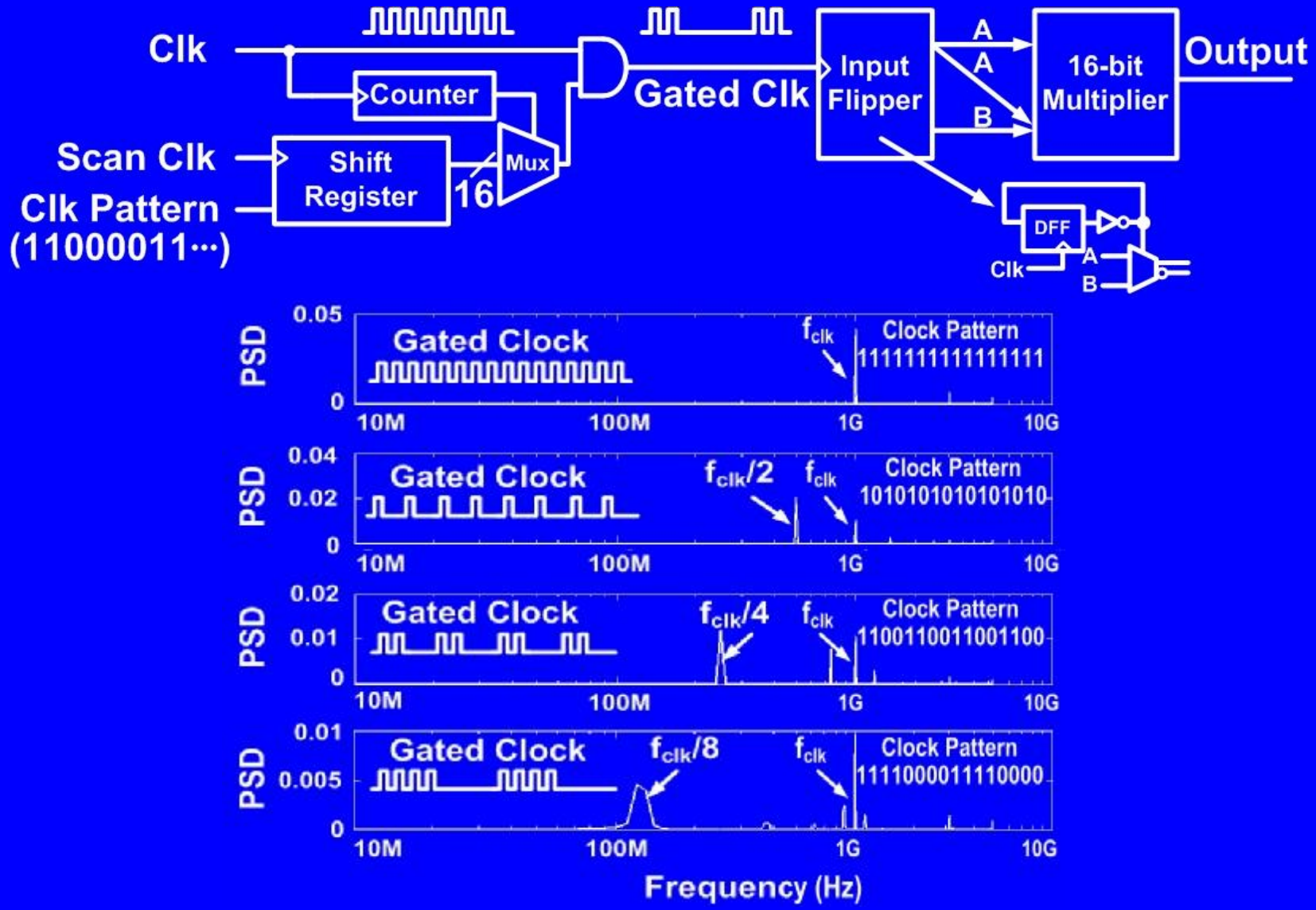
Test Chip Organization

0.13µm, 1.2V



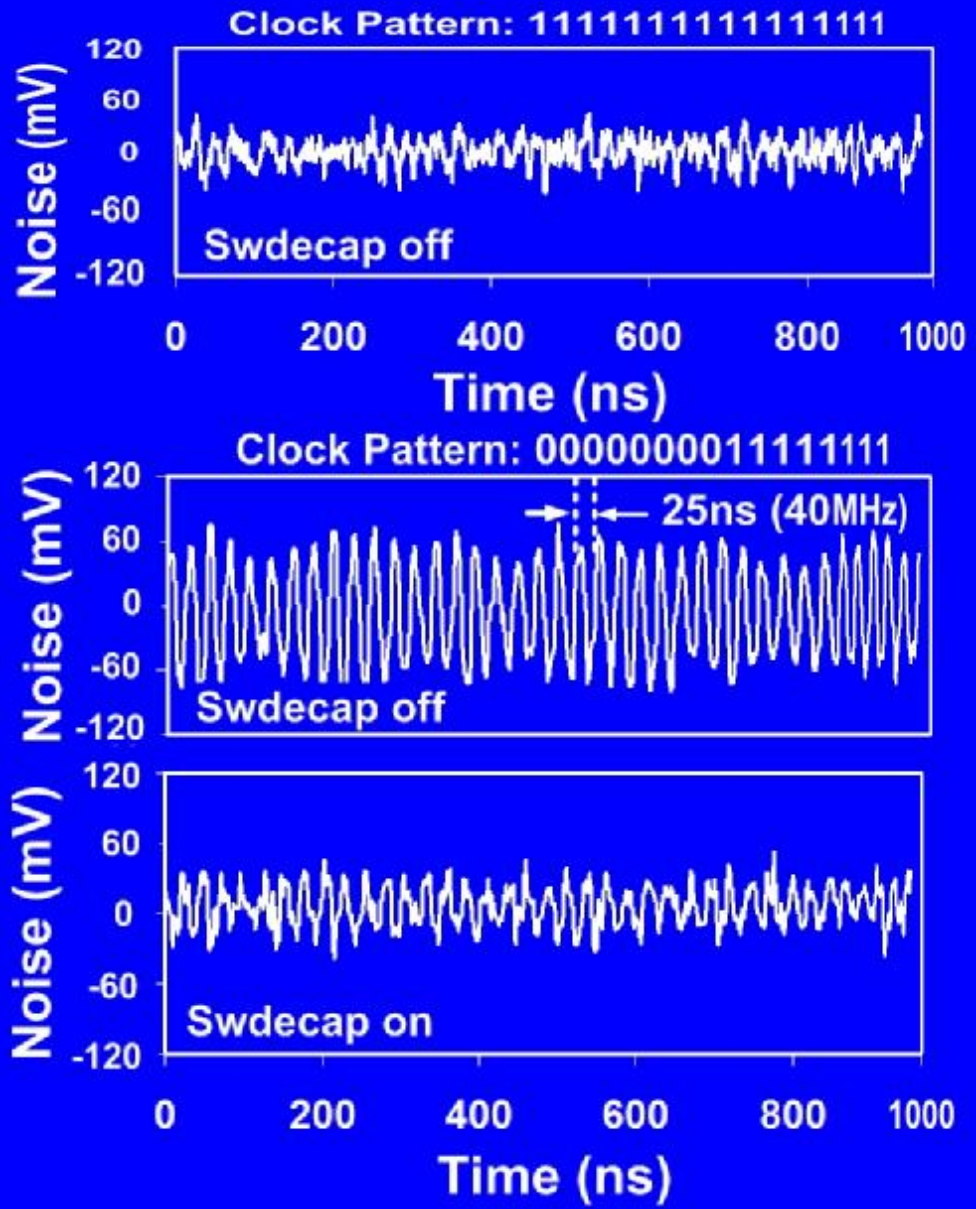
- Two types of noise generation circuits
- Selection of swdecap value: 100pF, 200pF, 300pF
- On-chip sensor to measure differential noise

Resonance Generation Logic



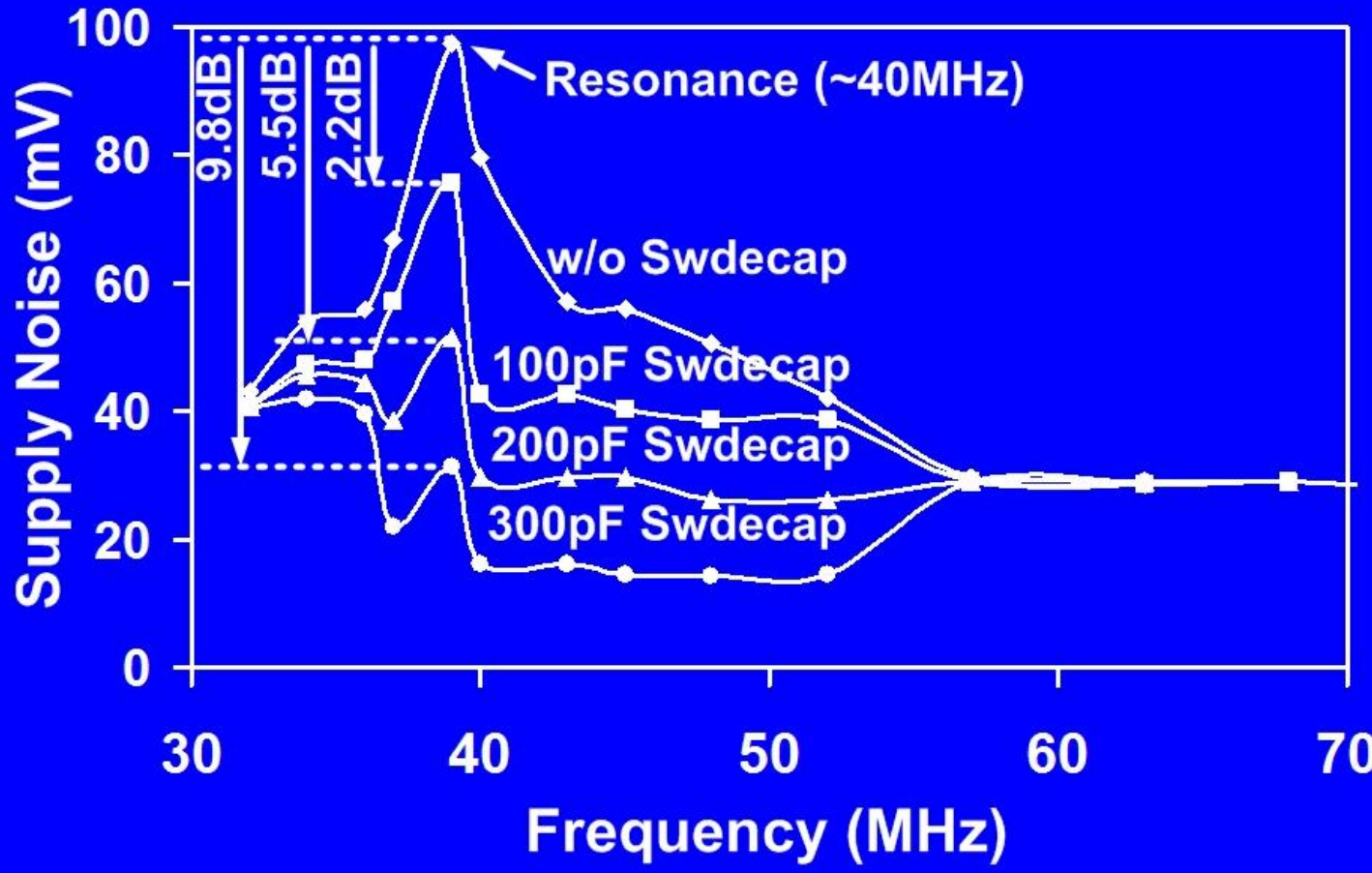
- Creates harmonics at resonant frequency

Supply Noise Measurements



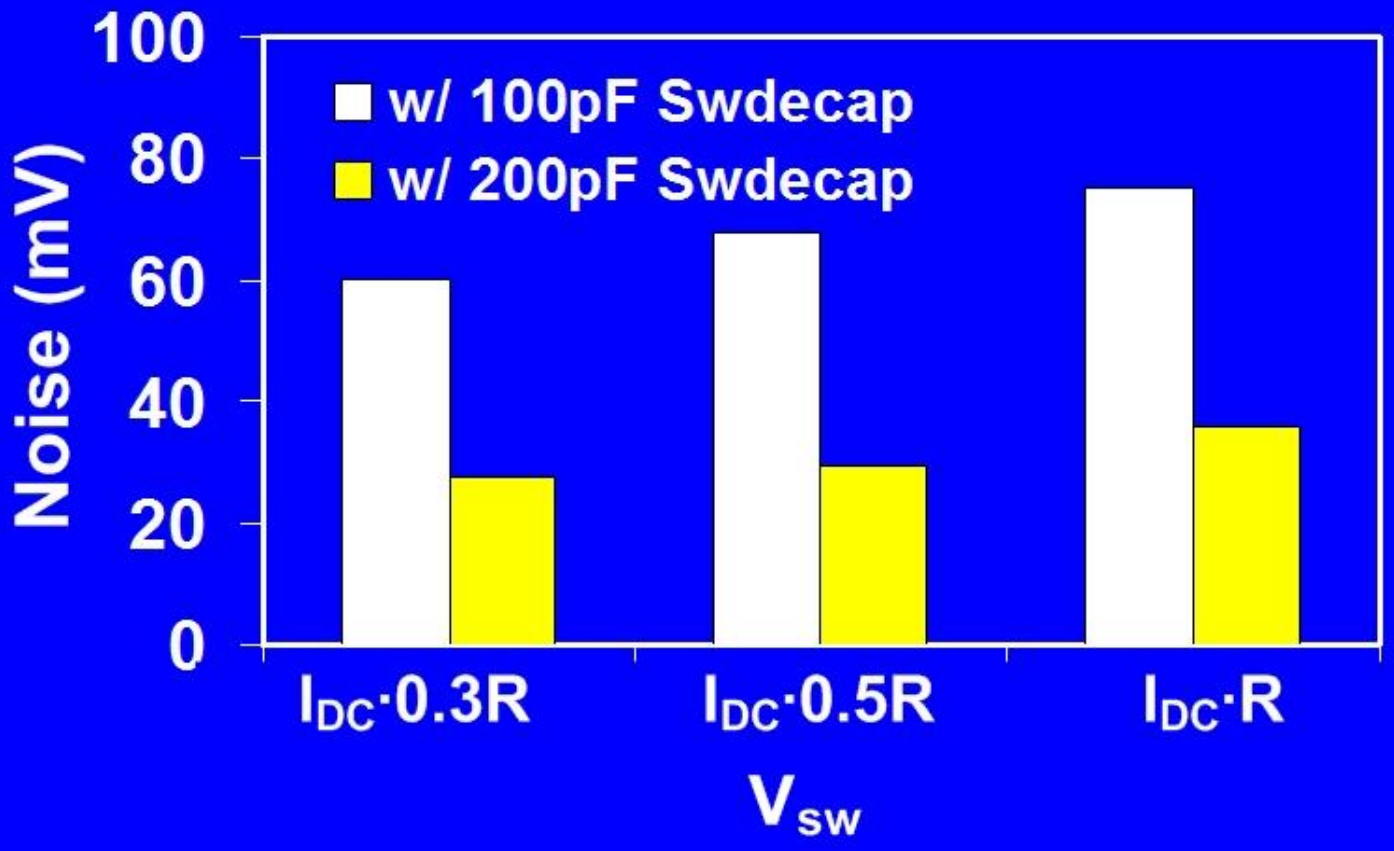
- 640MHz clock gated by 1/16
- 5.5dB noise reduction using 200pF swdecap
- f_{res} at 40MHz lower than expected due to package inductance

Frequency Domain Measurements



- 9.8dB suppression using 300pF swdecap
- No significant impact on non-resonant frequency noise

Adjusting Switching Threshold



- Noise magnitude more sensitive to swdecap value than V_{sw}

Comparison with Passive Damping

Swdecap Value	Resonant Suppression	Equiv. Passive Decap	Decap Boost	Equiv. Damp. Resistance
100pF	2.2dB	500pF	5X	0.1Ω
200pF	5.5dB	1500pF	7.5X	0.4Ω
300pF	9.8dB	3500pF	11X	1Ω

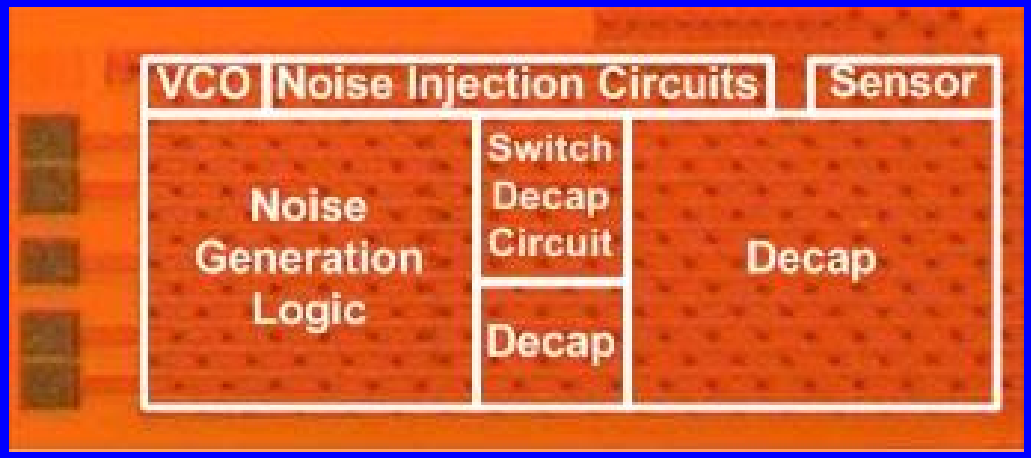
- **5−11X boost over passive decaps**
- **Equivalent to 0.1-1Ω resistive damping**
- **Passive resistor aggravates IR drop**

Performance Comparison

	Active Damping Ckt.*	This work
Technology	90nm	130nm
Static Current	2.42mA	0.54mA
Load Current suppressed	8.71mA ($3X\ I_{static}$)	33mA ($61X\ I_{static}$)
Regulator Area	$59x20\mu m^2$	$190x220\mu m^2$ (including 300pF)
First Droop Regulation	No	Yes
Analog Opamp	Yes	No

* J. Xu et al., Intel, ISSCC 2007

Die Photograph and Chip Summary



Technology	0.13μm Logic CMOS
Quiescent Current	0.54mA
Regulation Frequency	10−300MHz
Regulator Area (w/o decap)	100μmx70μm
Regulator Area (w/ 300pF decap)	190μmx220μm
Total Die Area	0.9mmx1.8mm

- **9X less static current compared with prev. swdecap design**
- **Swdecap serves as passive decap under norm. condition**
- **Up to 11X decap boost compared with passive decap**
- **Negligible power consumed for decap switching (1.2%)**

Conclusions

- Resonant supply noise impacts circuit performance and reliability
- A switched decap circuit is proposed
  - Low power resonant detection circuit
  - Digital-friendly implementation
  - Programmable and PVT insensitive switching threshold
- 0.13μm test chip implemented
  - 5−11X boost in effective decap value
  - Up to 9.8dB resonant noise suppression
  - 9X reduction in static current compared with previous switched decap design