A Process Variation Compensating Technique for Sub-90nm Dynamic Circuits

C. H. Kim, K. Roy, S. Hsu*, A. Alvandpour*,
R. K. Krishnamurthy*, S. Borkar*

Purdue University, West Lafayette, IN
**Circuit Research, Intel Labs,*
Intel Corporation, Hillsboro, OR

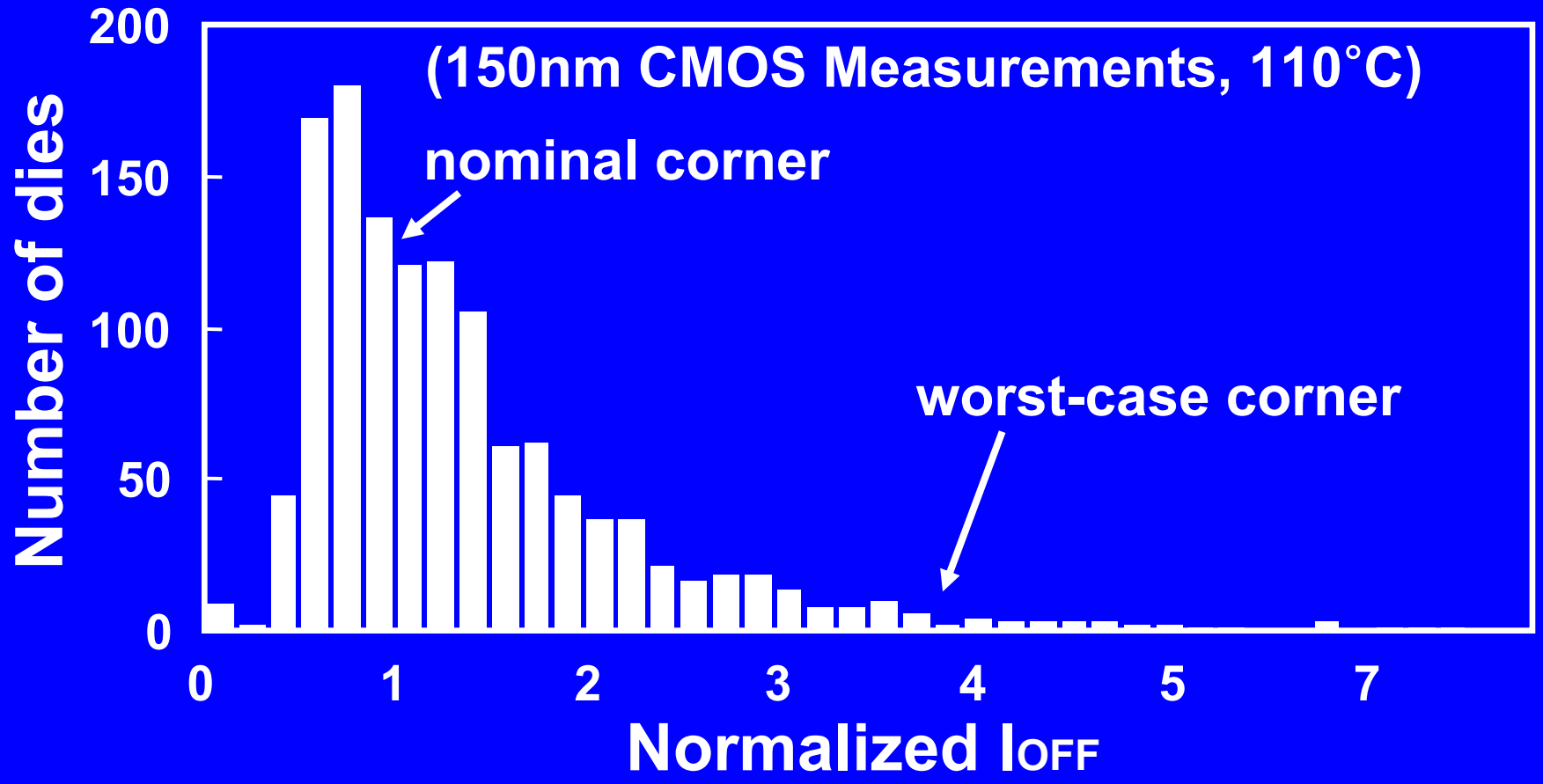
PURDUE UNIVERSITY

Intel Labs

Outline

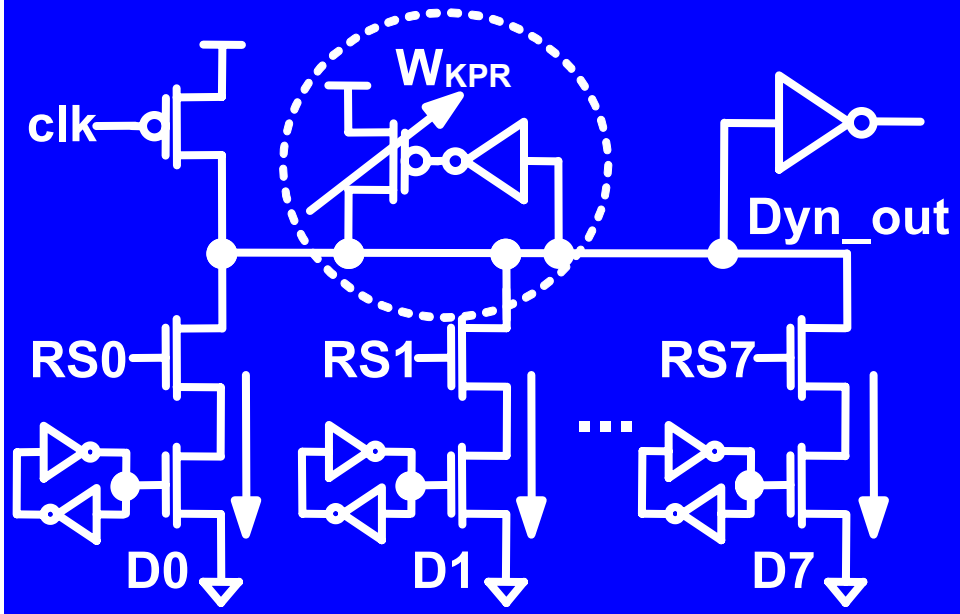
- Motivation
- Parameter Variation and Keeper Sizing
- Process Compensated Dynamic Circuit
- 90nm Delay, Robustness Squeeze
- 128x32b PCD Register File Results
- Summary

Motivation

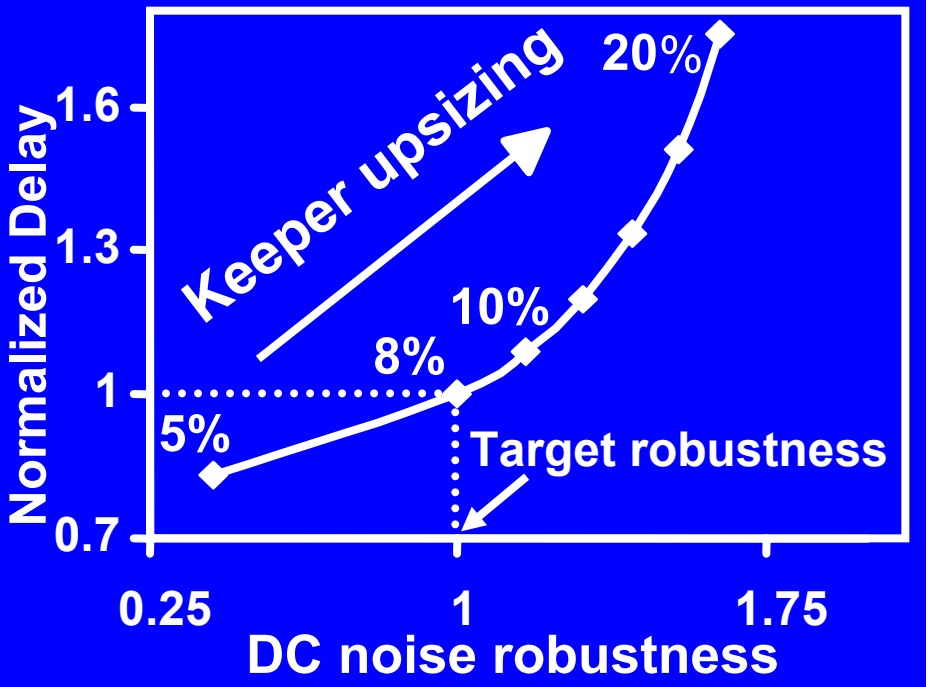


- Substantial variation in leakage across dies
- 4X variation between nominal and worst-case leakage
- Performance determined at nominal leakage
- Robustness determined at worst-case leakage

Leakage Variations Impact

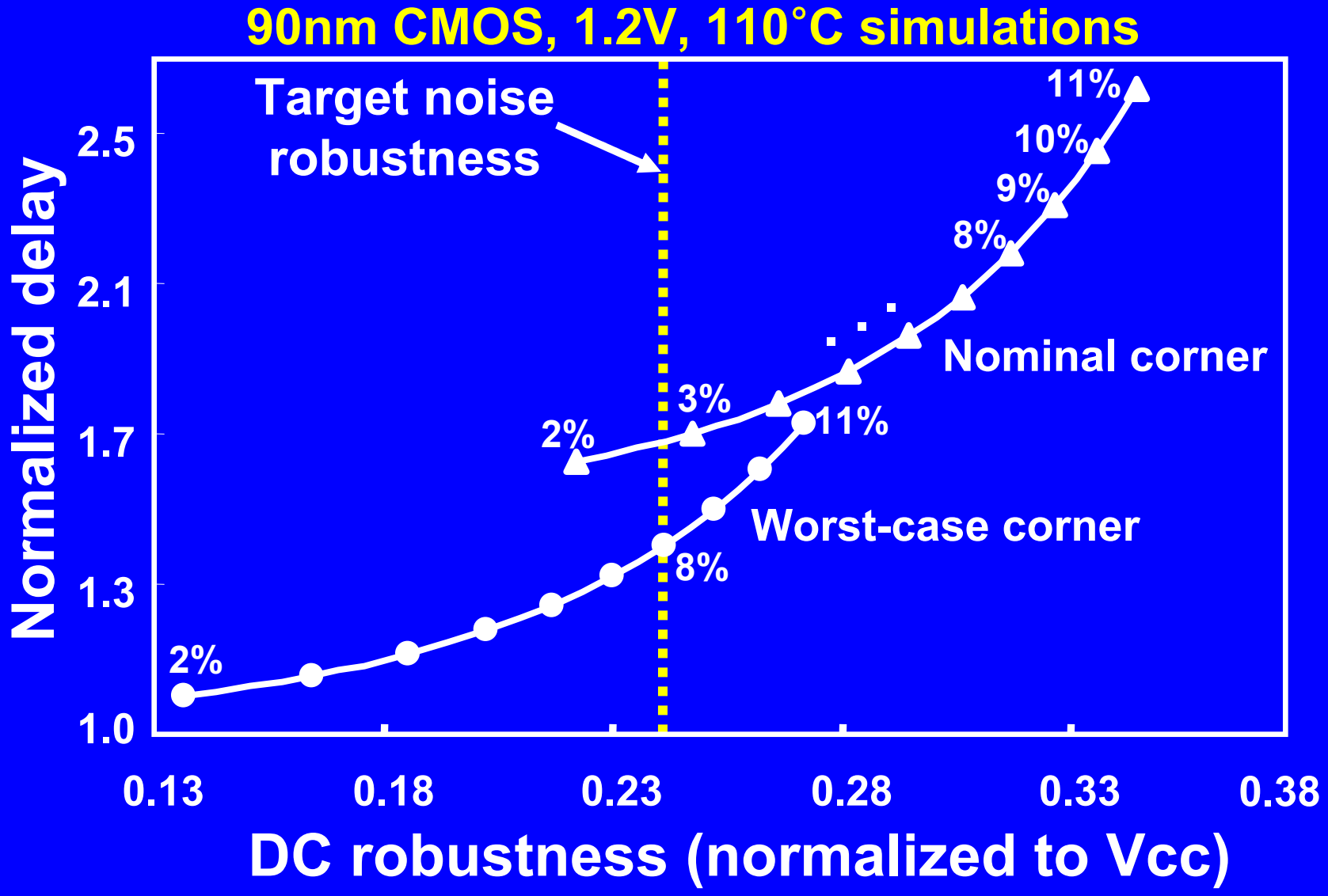


Dynamic 8-way Bitline



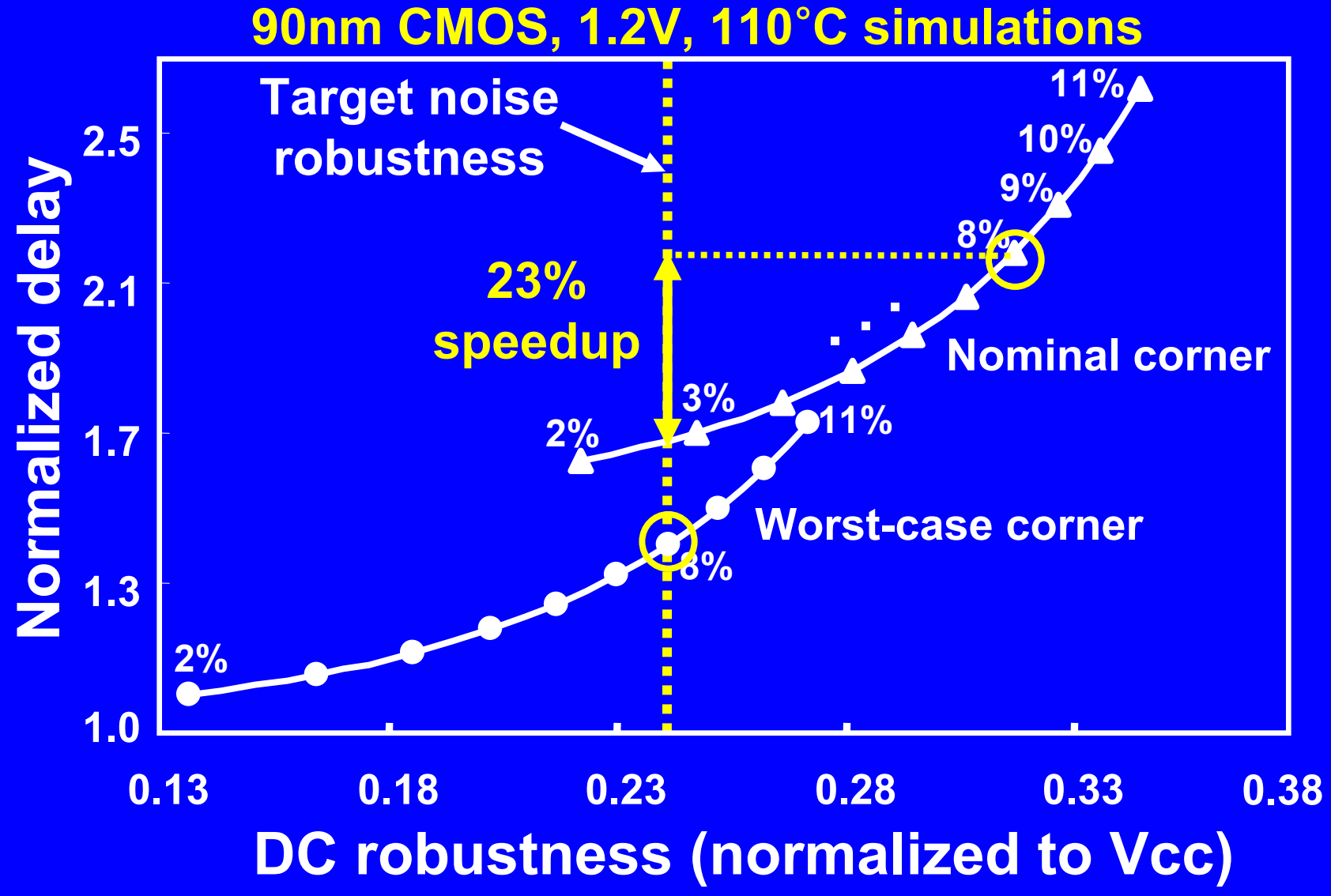
- Dynamic circuit NMOS pulldown leakage variation:
  - Keeper size determined for target robustness at worst-case leakage corner
  - Excess leakage dies: fail to meet target robustness
  - Lower leakage dies: over-designed for robustness

Delay and Robustness Spread



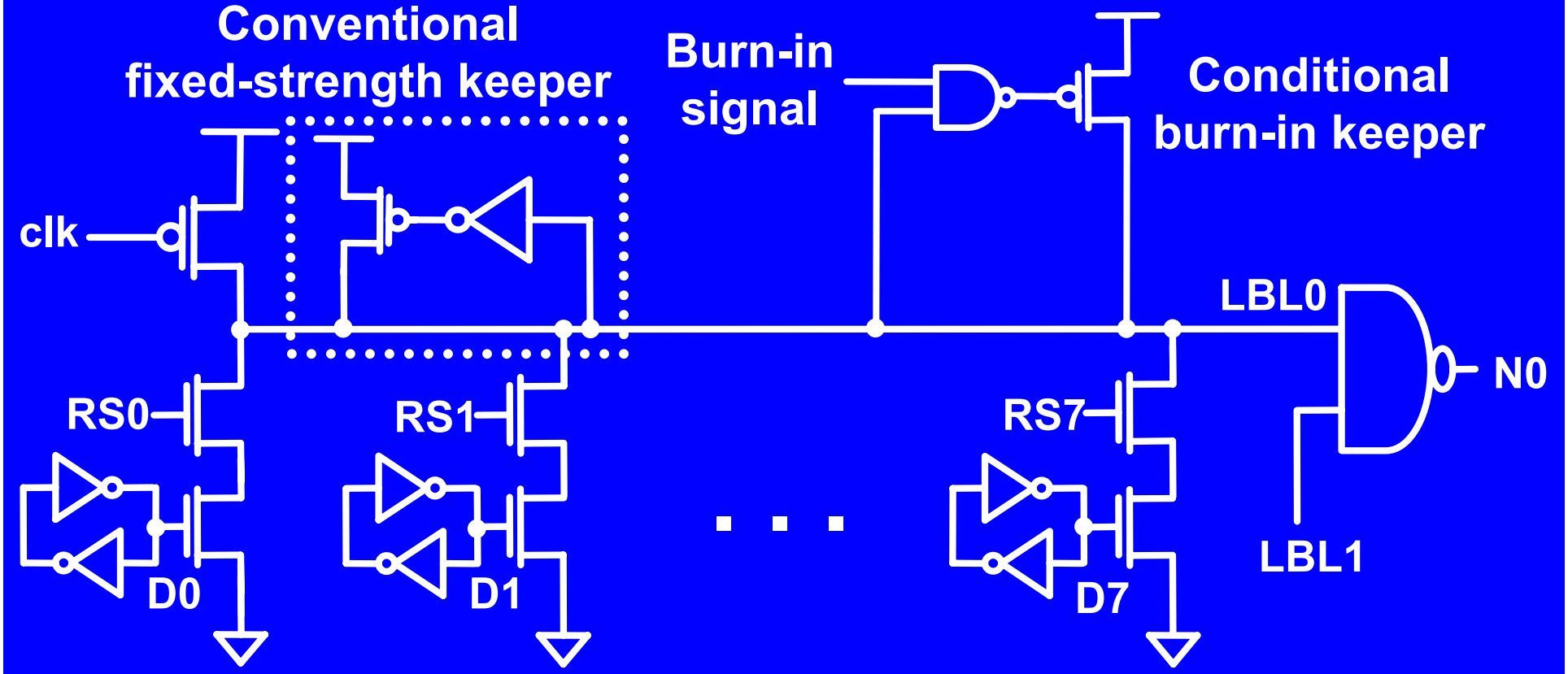
- Fast corner keeper sizing is sub-optimal for delay

Variable Strength Keeper Size



- Goal: downsize keeper on nominal leakage dies

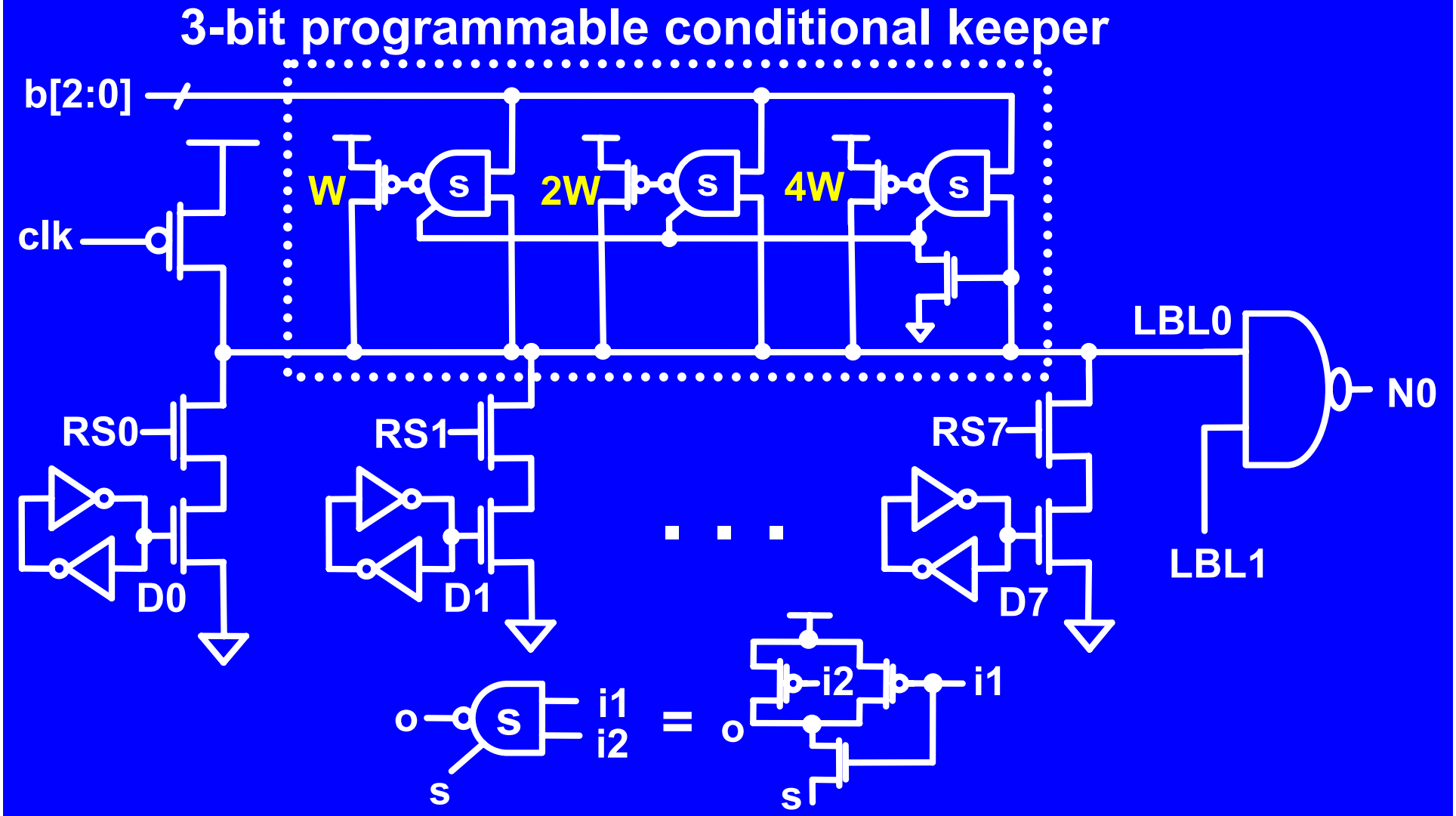
Process Compensating Dynamic Circuit Technology: Evolution



A. Alvandpour et al, CICC'02

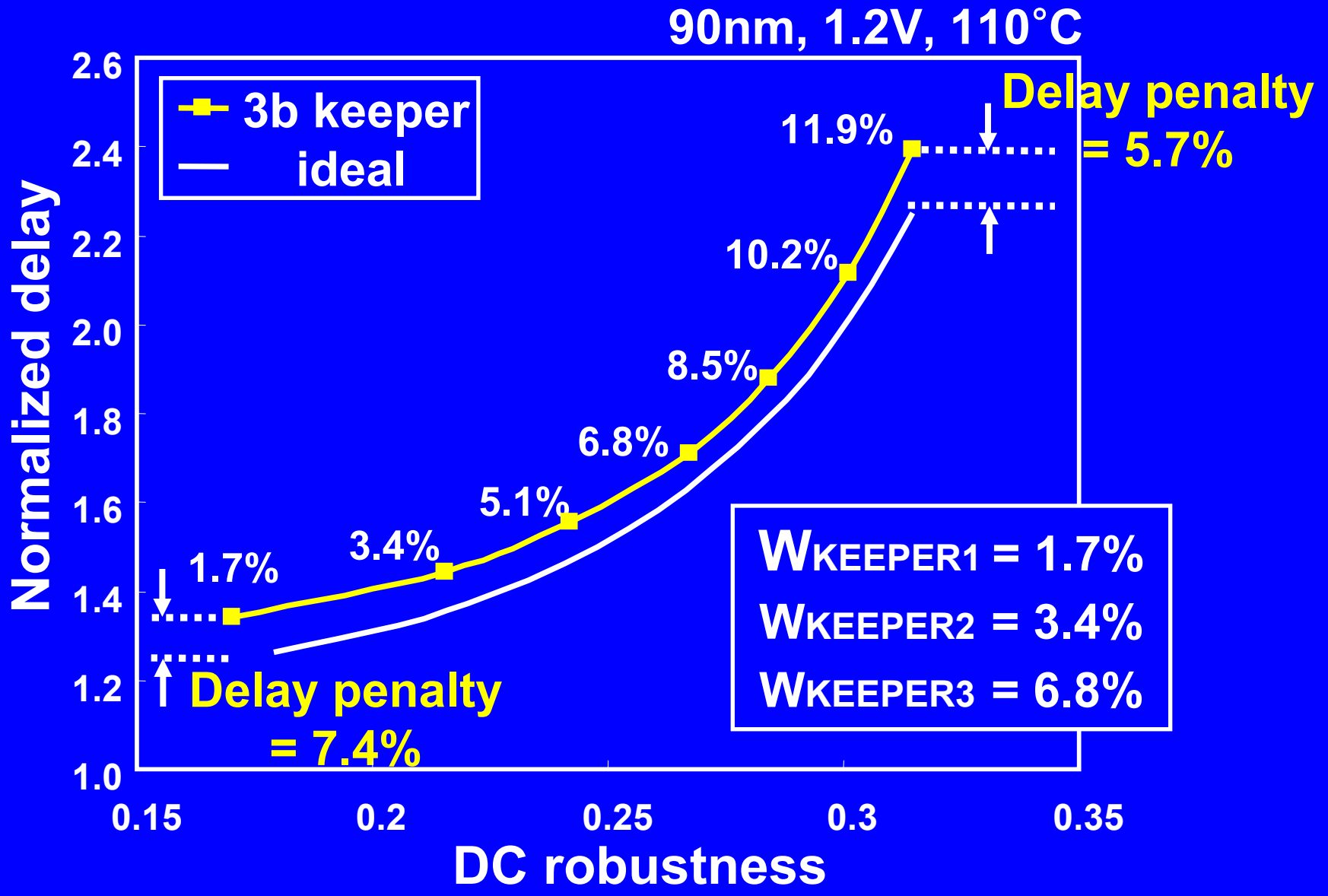
- Secondary conditional keeper activated under excessive leakage conditions
- Deactivated during nominal mode operation

Process Compensating Dynamic Circuit Technology



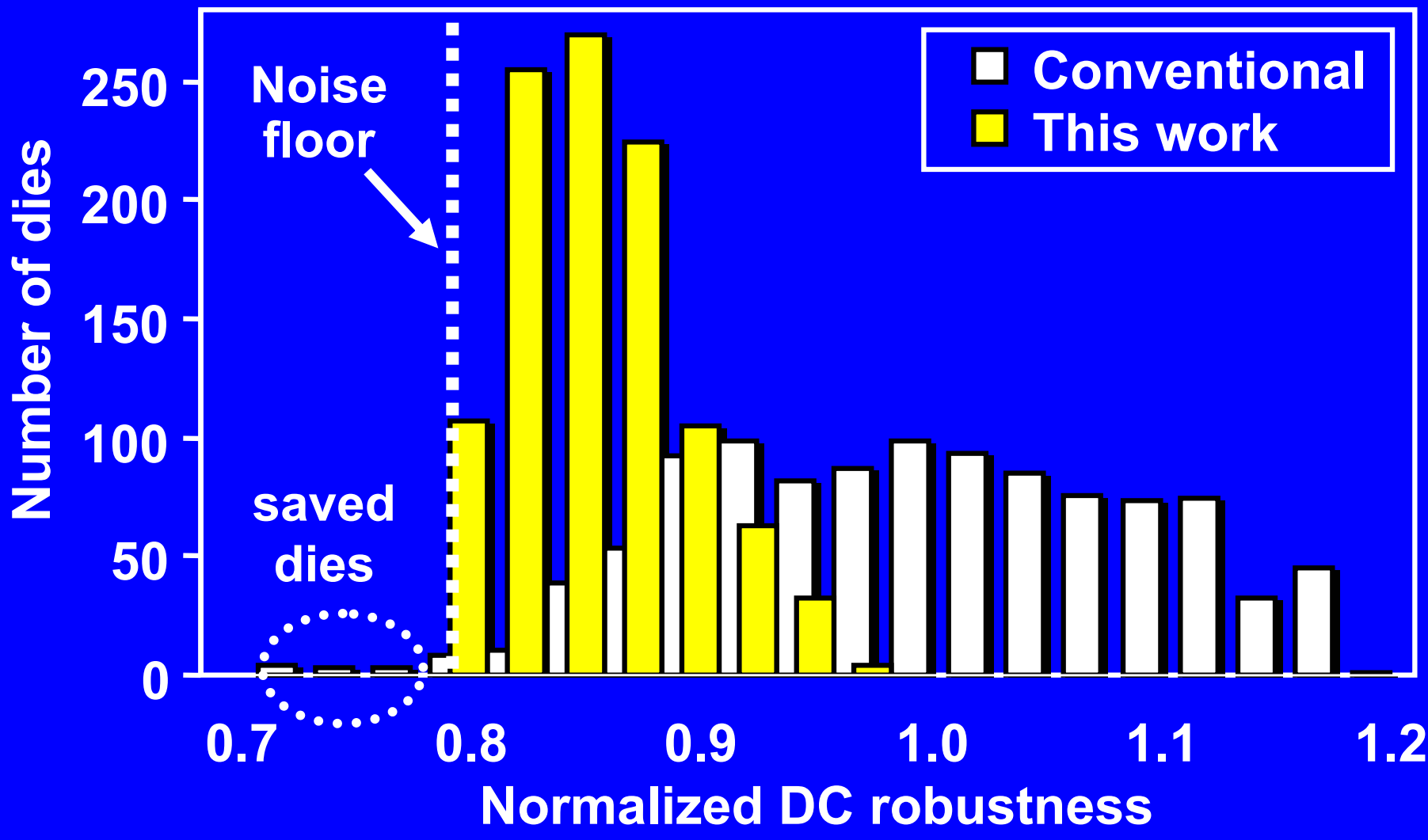
- Shared-NAND: 2 less NMOS devices, dense layout

Delay Penalty of PCD



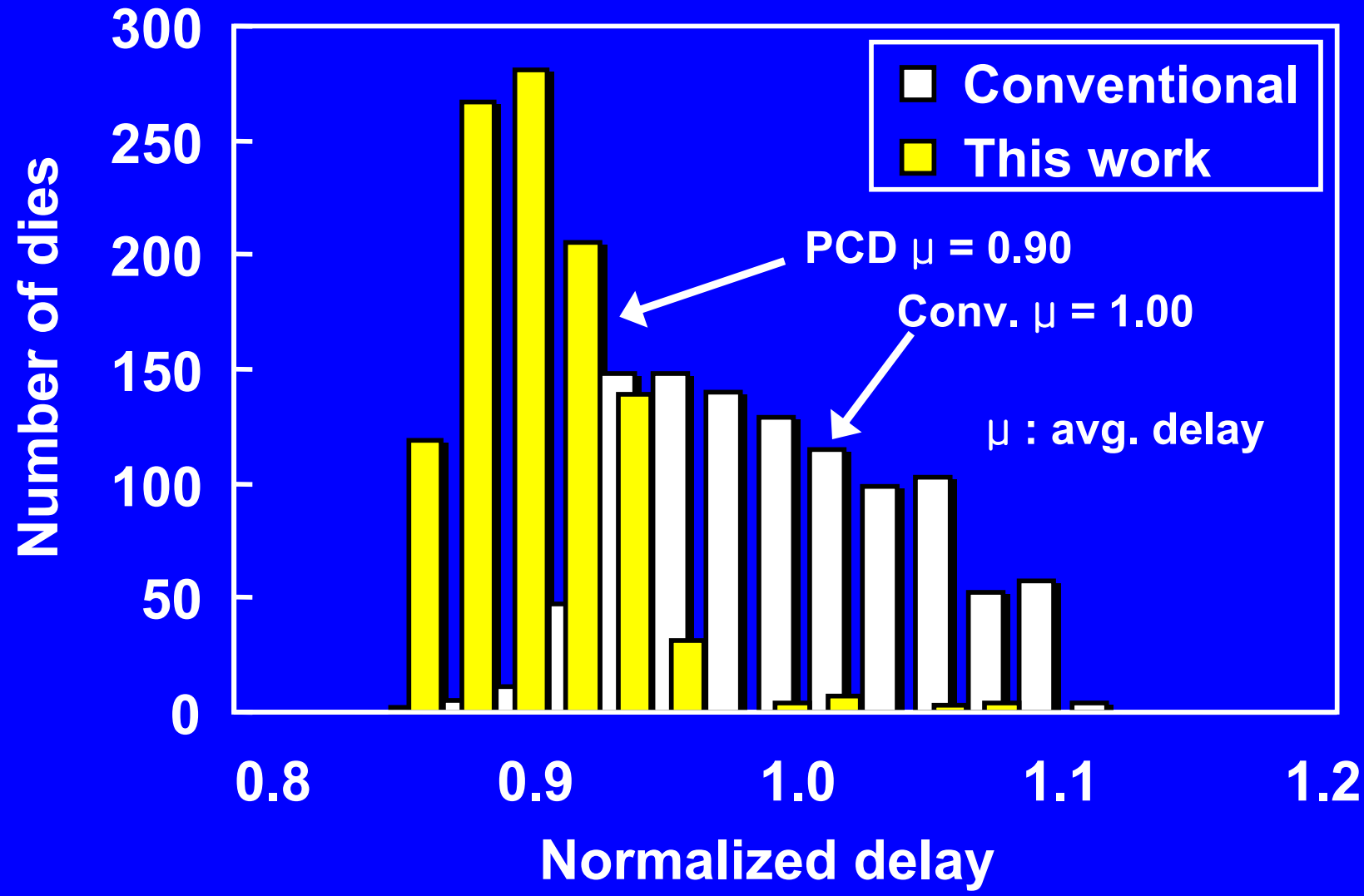
- Delay penalty is offset by opportunistic speedup

Robustness Squeeze



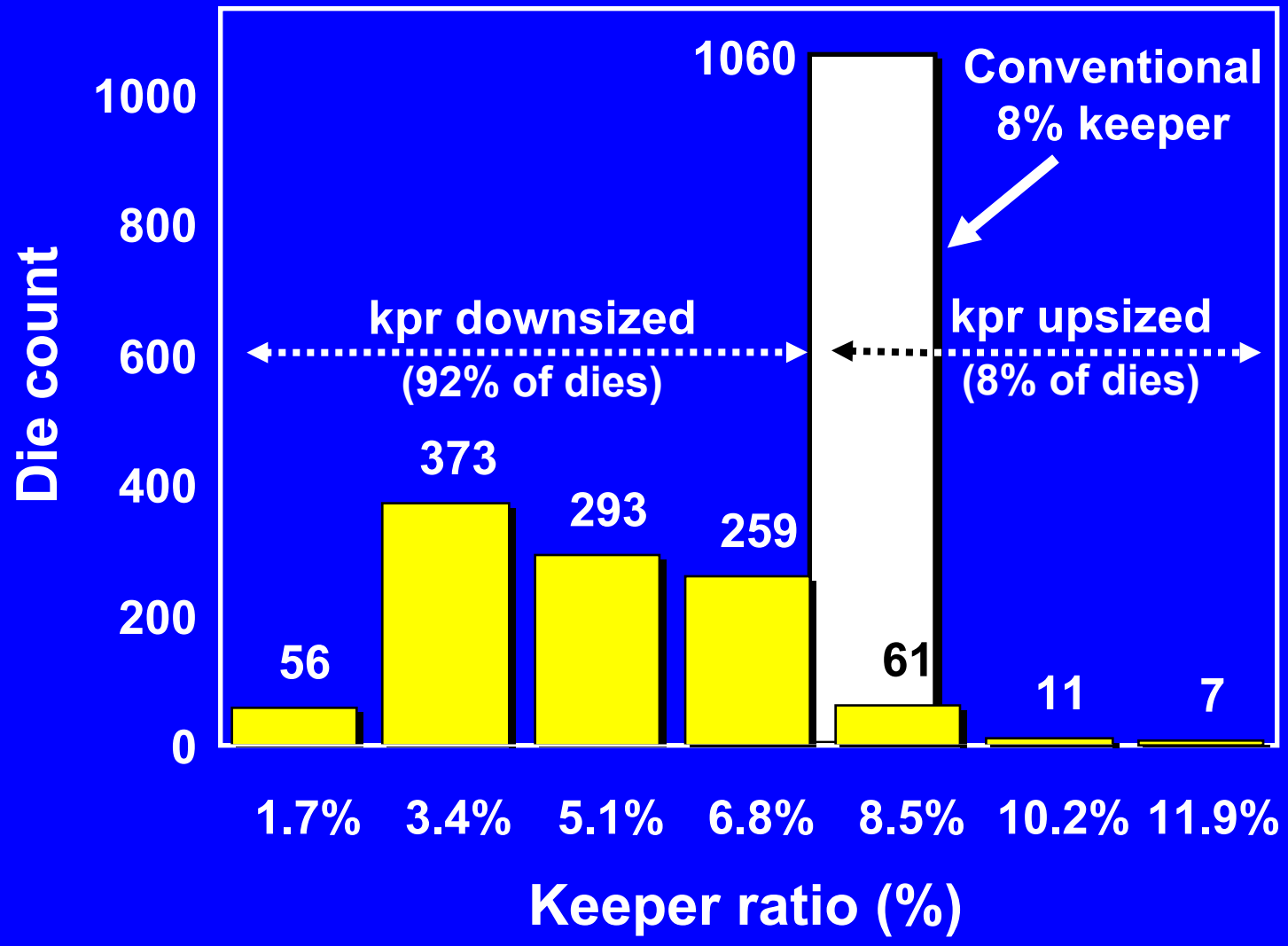
- 5X reduction in robustness failing dies

Delay Squeeze



- 10% opportunistic speedup

Keeper Ratio Distribution



- Keeper downsized in 92% of dies

Effectiveness of PCD

90nm, 1.2V, 110°C

	Robustness		Delay	
	μ	σ/μ	μ	σ/μ
Conventional	1.00	9.4 %	1.00	5.2 %
This work	0.85	4.2 %	0.90	3.4 %

	% of robustness failing dies
Conventional	1.1%
This work	0.2% (5X ▼)

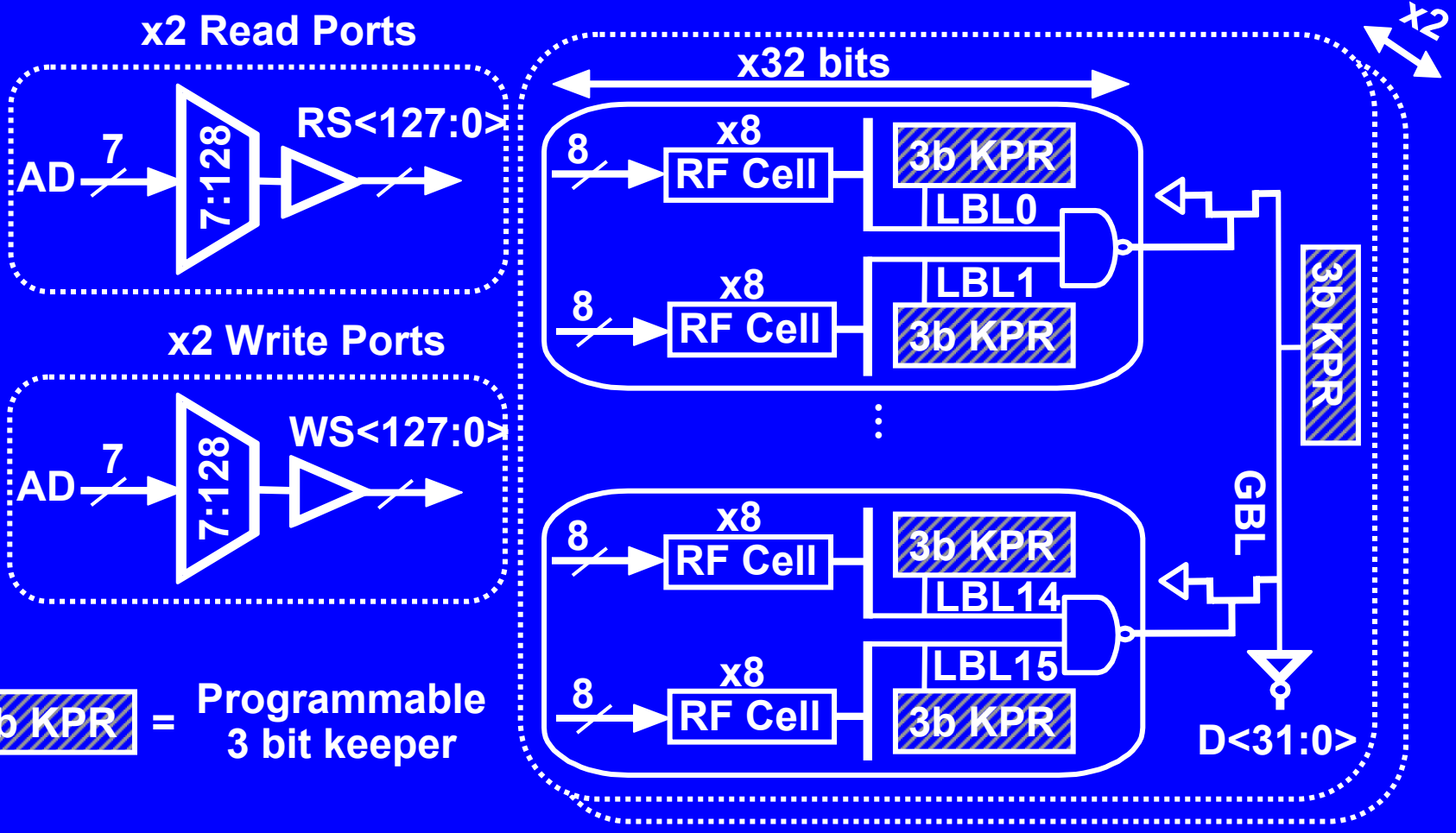
2 bit Control vs. 3 bit Control

90nm, 1.2V, 110°C

	Robustness		Delay	
	μ	σ/μ	μ	σ/μ
PCD 2 bit	0.87	5.2 %	0.89	4.5 %
PCD 3 bit	0.85	4.2 %	0.90	3.4 %

- Less squeeze in robustness and delay
  - Limited keeper range/resolution
- Lower delay penalty
  - Smaller diffusion cap. on domino node

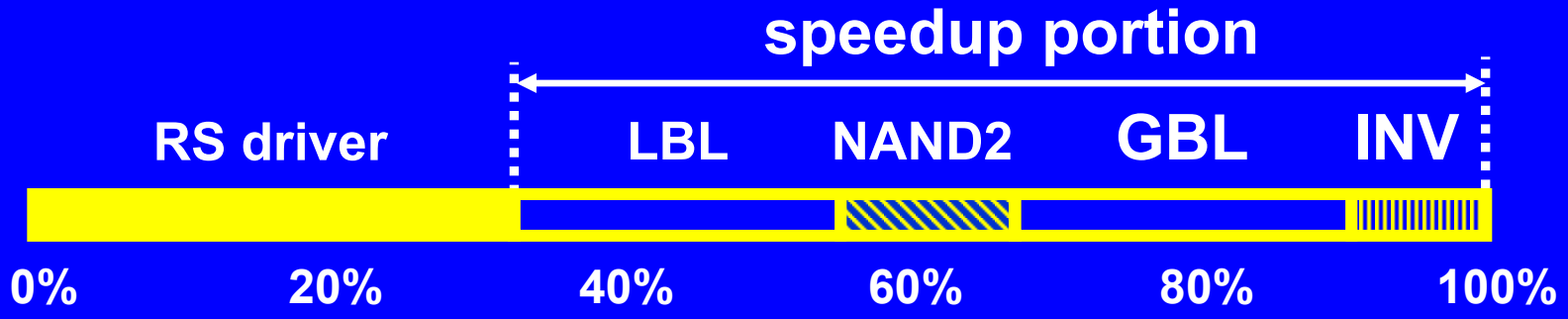
128x32b 2R2W PCD Register File



- Single-ended read, 8 bitcells/LBL, 8-way GBL
- Keeper folded into existing layout templates

PCD Register File Delay, Energy

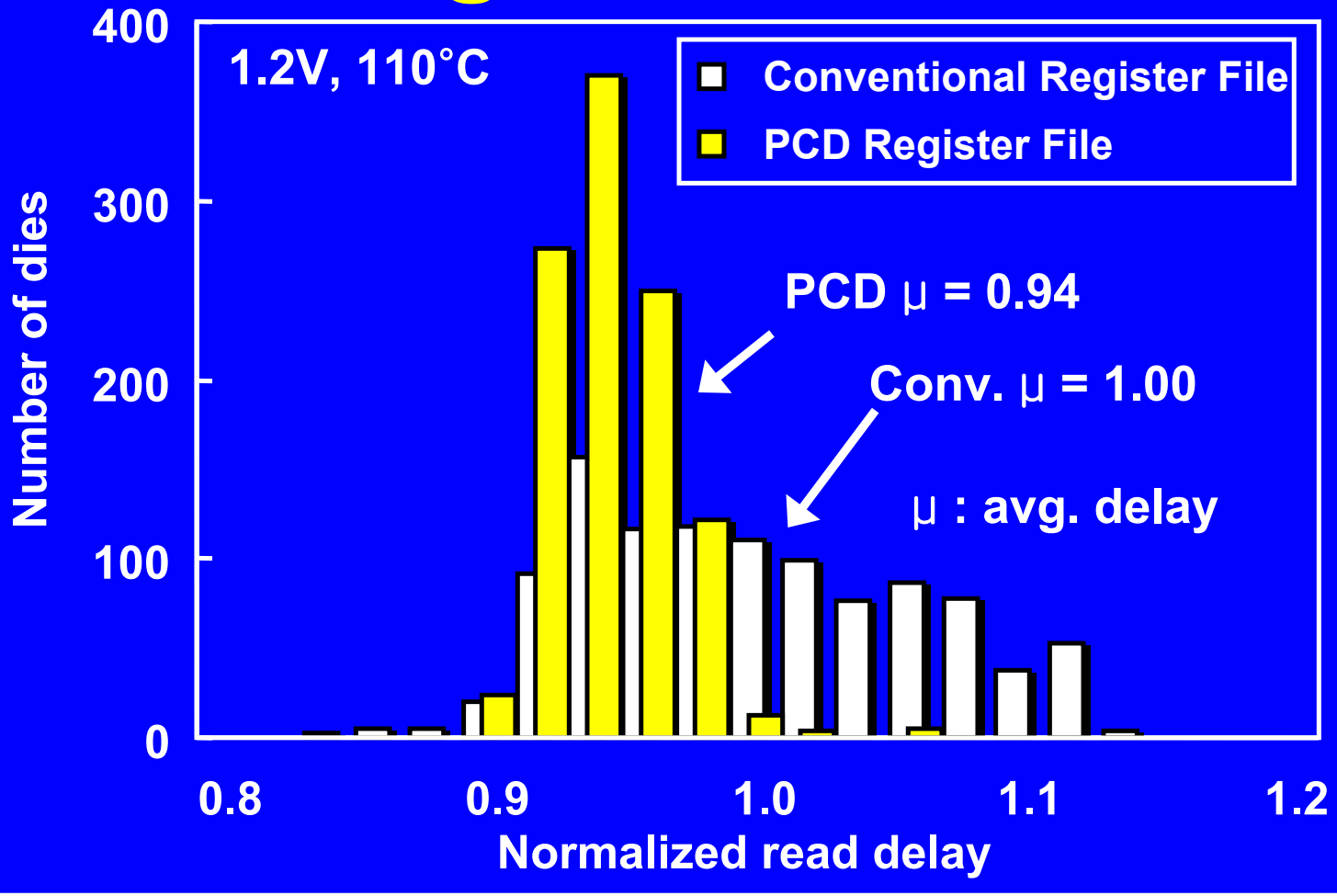
90nm, 1.2V, 110˚C



Register file delay breakdown

- Speeds up 67% of RF critical path delay
- 2% worst-case total energy overhead

PCD Register File Results



Read Delay Benefit	5.5%
Robustness Failing Dies	0.2% (5X ▼)
Read Delay Variation: σ/μ	6.1%→2.3% (2.7X ▼)

Summary

- Process Compensating Dynamic Circuit:
  - Prevents pessimistic keeper sizing
  - Digital keeper programmable based on die leakage measurements
- Delay, robustness squeeze in sub-90nm
  - 5X reduction in robustness failing dies
  - 10% opportunistic speedup
- 128x32b 2R2W PCD register file is implemented