

Emerging Memory Technology Landscape

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The charge storage based conventional memory technologies such as NAND Flash and DRAM are faced with scaling limits at dimensions smaller than 20 nm. Several flavors of new memory technologies based on alternate state variables are under active research and exploration. In addition, for cross-point architecture implementation, a suitable select device compatible with the memory element is required. This presentation will give an overview of some of the most promising candidates for memory including magnetic memories. The review will include discussion of desirable target metrics for a memory chip and some fundamental limitations in performance arising from materials complexity and device physics constraints.

Recent Progress and Future Directions in NAND Flash Scaling

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This paper discusses recent progress and future directions in NAND flash scaling. NAND cell scaling has been successful and the leader in pitch scaling. However, as technology node has reached sub-20nm and beyond, multiple scaling issues become pronounced [1-3].

Structure scaling is one of the biggest challenges for the conventional wrap floating-gate (FG) cell because of the high (>50nm) floating gate height and the inter-poly-dielectrics (IPD) wrapping FG sidewall. Cell-to-cell interference is a critical issue for Vt placement [4]. FG depletion degrades programming characteristics [3]. Increase of electrical field at FG and control gate (GC) degrades cycling reliability [5-6].

The flat planar cell has been suggested to overcome those scaling issues and various technology options were investigated [7]. Among them, the thin planar FG cell is the most successful because of the excellent program/erase characteristics (P/E window and slope) and reliability meeting multi-level-cell (MLC) requirements (Fig.1). Scaling capability to sub-20nm technology node has been demonstrated (Fig. 2) [7].

2D NAND scaling is extended significantly by introducing the thin planar FG cell. In the future, increase in cell noise due to few electron effects and high WL-WL E-field will be remaining challenges which eventually will limit the 2D NAND scaling [6]. 3D NAND is suggested to overcome those challenges owing to the large physical cell size [8-9].

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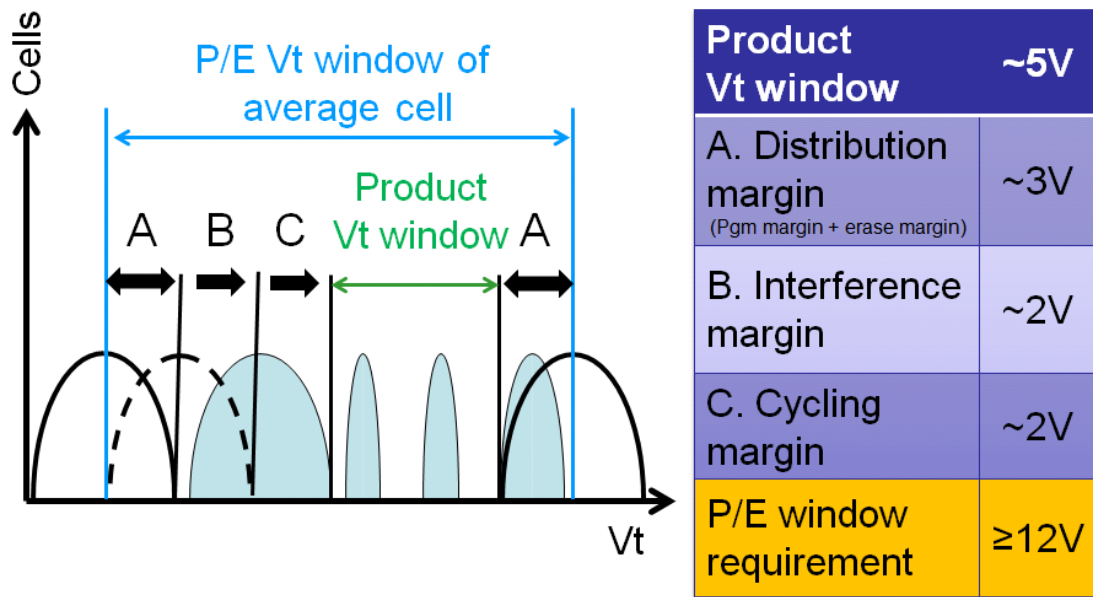


Fig. 1 Program/Erase Vt window requirement for MLC NAND [6].

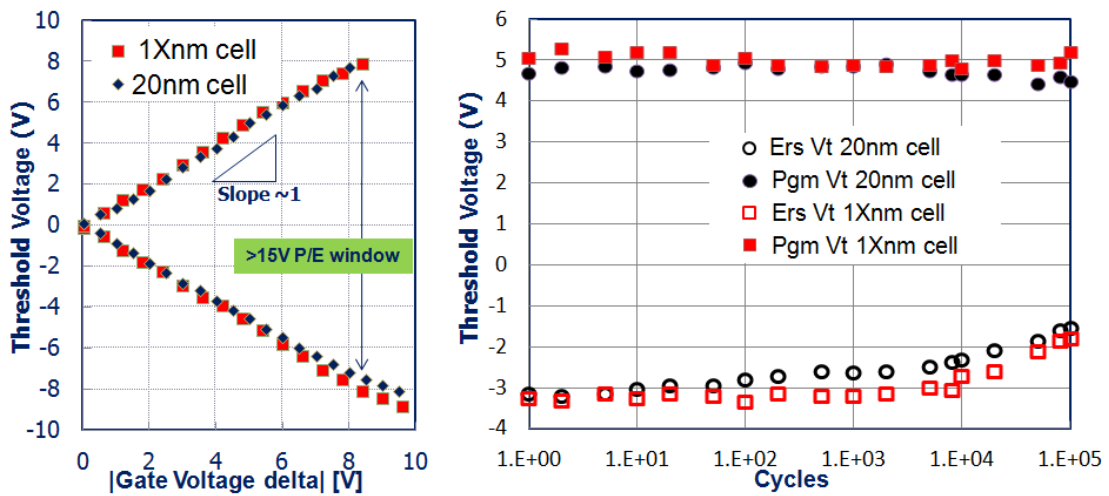


Fig.2 P/E characteristics and cycling endurance of thin planar FG cell [7].

Challenges and Opportunities of Magnetoresistive Based Memory and Logic and their Integration

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An energy efficient memory and logic device for the post-CMOS era has been the goal of a variety of research fields. The limits of scaling, which we expect to reach by the year 2025, demand that future advances in computational power will not be realized from ever-shrinking device sizes, but rather by innovative designs and new materials and physics. Magnetoresistive based devices have been a promising candidate for future integrated magnetic computation because of its unique non-volatility and functionalities [1]. The application of perpendicular magnetic anisotropy for potential STT-RAM application was demonstrated [2, 3] and later has been intensively investigated by both academia and industry groups, but there is no clear path way how scaling will work for both memory and logic applications. One of main reasons is that there is no demonstrated material stack candidate that could lead to a scaling scheme down to sub 20 nm. Another challenge for the usage of magnetoresistive based devices for logic application is its available switching speed. Although a good progress has been made to demonstrate the fast switching of a thermally stable magnetic tunnel junction (MTJ) down to 165 ps [4], it is still 4-6 times slower than its CMOS counterpart. In this talk, I will review the challenges and discuss the opportunities and some potential path ways for magnetoresistive based devices for memory [5] and logic applications and their integrations.

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Robust Low-power Multi-terminal STT-MRAM

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Design issues arising from bi-directional write current requirement, and shared read and write current paths severely limits the design space spin-transfer torque MRAM (STT-MRAM) [1]. Although failure mitigation techniques have been proposed [2]-[4], they may be insufficient for realizing the true potential of STT-MRAMs at scaled MTJ technologies due to different resistive characteristics [5], and asymmetries in MTJ characteristics as well as access transistor driving ability [6].

Multi-terminal STT-MRAM (MTSTT) structures, such as the dual-pillar STT-MRAM (DPSTT) [7] with decoupled read and write current paths, and STT-MRAM with complementary polarizers (CPSTT) [8] with differential self-referencing read operations, have been proposed to expand the STT-MRAM design space. Even though they may require more than one access transistor, the overall area of MTSTT based memory cells may be smaller than the conventional STT-MRAM memory cell due to relaxed transistor width requirements. Hence, MTSTT offers an attractive alternative in mitigating design challenges in STT-MRAM. The CPSTT based memory cell (Fig. 1) stores data in one free layer (FL) but uses two complementary polarized pinned layers (PL) instead. Write operations occur by steering current through the appropriate PL, thus avoiding bi-directional write current requirements and asymmetric transistor driving ability. The availability of complementary polarized PL's allows differential self-referencing read operations in CPSTT, enhancing its robustness against process variations while allowing fast single-cycle read operations. Furthermore, the fully-differential nature of CPSTT allows implementation of CPSTT based content-addressable memories without modifications to the CPSTT memory cell. Numerical analysis of CPSTT based memory cells (Fig. 2) show up to 25% lower write power at iso-write margin and cell area, improved sensing margins as well as read disturb failures.

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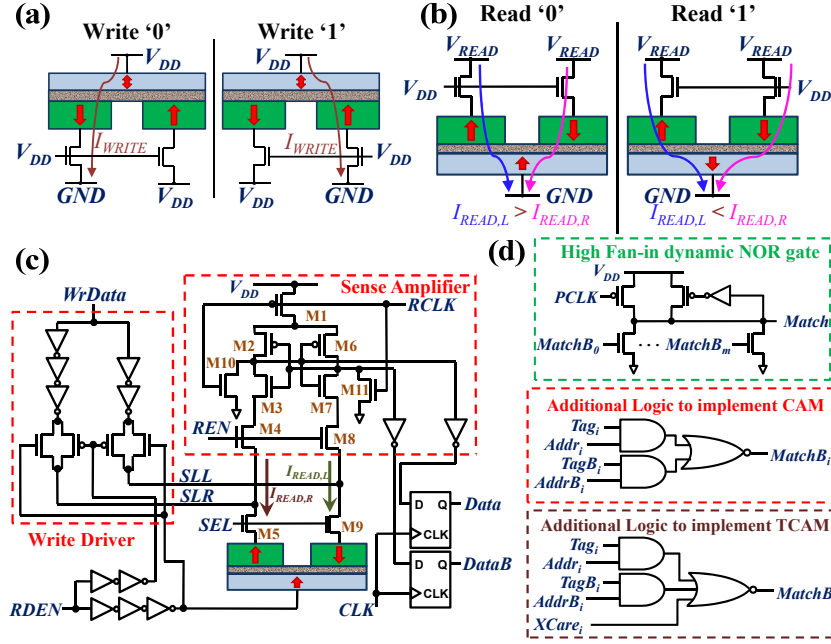


Fig. 1. (a) Write and (b) read operation principle of CPSTT memory cell and (c) the peripheral circuitry for memory array operation. (d) Content-addressable memory (CAM) implementations may be achieved using additional logic in the read sense amplifier, which is shared along a column, without modifications to the CPSTT memory cell as compared to 6T SRAM based CAM.

Barrier Height	$56k_B T$		
Write Pulse Width	2ns		
FL size (1T1MTJ)	$10 \times 10 \times 1.5 \text{ nm}^3$	$t_{MGO} \text{ (nm)}$	CPSTT Write Power (μW)
FL size (CPSTT)	$10 \times 22.5 \times 1.5 \text{ nm}^3$		1T1MTJ Write Power (μW)
1T1MTJ		0.9	9.626
$I_C('0'), I_C('1')$	9 μA , 17 μA	0.95	10.95
CPSTT		1.00	14.36
$I_C('0'), I_C('1')$	14 μA , 14 μA	1.05	17.20
TMR	$\sim 160\%$ @ $t_{MGO} = 1.15 \text{ nm}$	1.10	19.66
$R_{Ap} @ V_{MTJ} = 0 \text{ V}$	$\sim 7.5 \Omega \cdot \mu\text{m}^2$ @ $t_{MGO} = 1.15 \text{ nm}$	1.15	21.80
			22.23

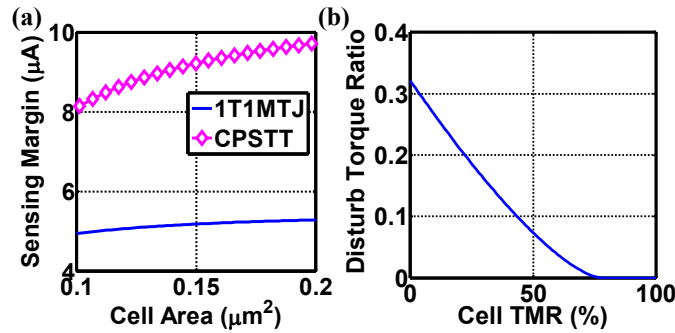


Fig. 2. Numerical analysis using the parameters shown in the top left table shows that CPSTT has better write power efficiency than 1T1MTJ STT-MRAM at iso-write margin (10%) and iso-cell area ($\sim 0.1308 \mu\text{m}^2$). (a) Sensing margin of CPSTT is about 2x that of 1T1MTJ while (b) torque per read current is also lower in CPSTT.

Thermally Assisted Switching STT MRAM

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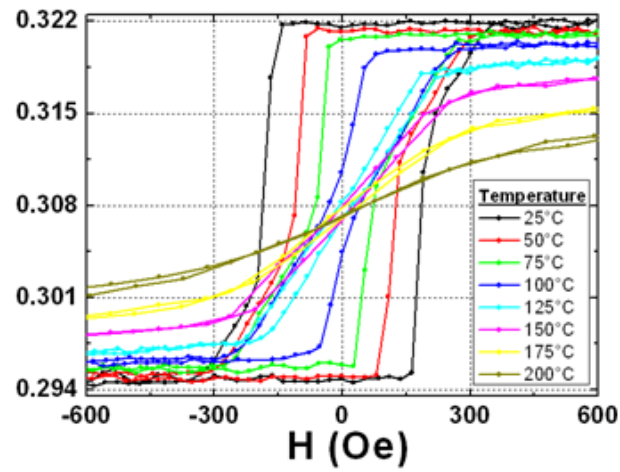
Since its inception in the late 90's and despite numerous promising announcements, MRAM has yet failed to live to its expectations. The recent advent of spin transfer torque (STT), however, has shed a new light on MRAM with the promises of much improved performances and greater scalability to very advanced technology nodes. As a result, MRAM is now viewed again as a credible solution for stand-alone and embedded applications where the combination of non-volatility, speed and endurance is key. Scaling to sub-20nm, however, remains a challenge. Whereas process teams focus on cell etching, physicists have to deal with issues such as reliability, write power and write efficiency, and, last but not least, data retention at such small sizes.

In this paper, we show how thermal assistance [1] can be a solution to ultimate scaling, in particular if implemented together with spin transfer torque (STT). Thermally Assisted Switching (TAS) is now being deployed in memories and logic devices using (magnetic) field-driven writing schemes. Combining TAS with STT writing has been initially proven in standard planar magnetization stack, with much improved thermal stability factors, yet little if no impact on total write power [2]. The same approach is now being pursued in cells with perpendicular magnetization, which is believed to be preferred route for small feature sizes.

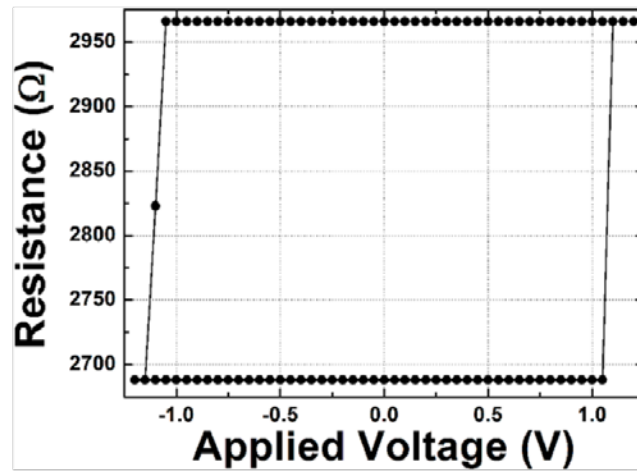
For devices less than 30nm the switching process proceeds through coherent rotation and the total current for switching by STT becomes proportional to the thermal stability factor, representing a minimum value for the STT write current. Keeping a 10 year retention on Gbit density below the 20nm node can be achieved using thermally induced anisotropy reorientation (TIAR). This proposed writing scheme uses the intrinsic heating of the cell, when current flows through the cells during STT write, to induce an anisotropy reorientation of the storage layer from perpendicular to in-plane. This results in a decreased switching power, at no cost on thermal stability, hence an increased writing efficiency, as measured by the ratio between thermal stability and critical current (Δ/I_C). TIAR is believed to be the best solution to combine minimal write power, proper reliability and scalability to sub-20nm.

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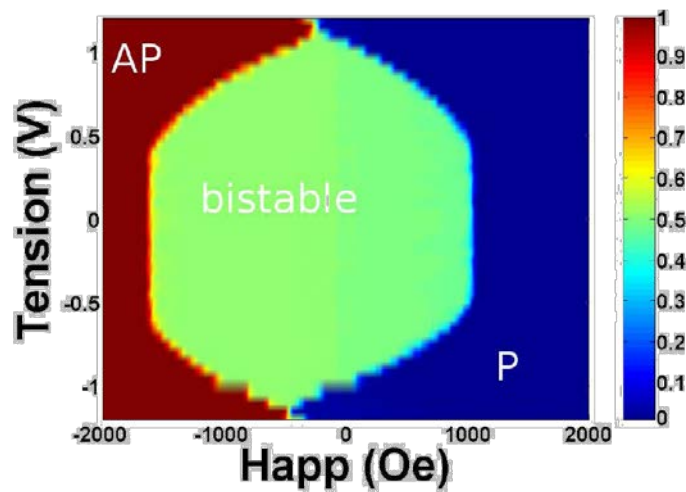
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(STT) current-induced anisotropy reorientation in perpendicular MRAM cells



STT-TIAR hysteresis loop for 110nm cells and 30ns write pulses.



STT-TIAR write phase diagram for 110nm diameter cells and 30ns write pulses.

High speed and low current STT-MRAM for Normally-off Computing

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Reduction of the power consumption of CPU is a critical requirement. In order to reduce the power consumption, the normally-off computing has been proposed[1]. The CPU energy is mainly consumed by the leak current of the cache memory. Therefore, the energy consumption is expected be reduced by shutting down the power of these cache memories during their waiting time. This is the concept of the normally-off computing. However, the CPUs with the volatile SRAM based cache memories will lose data by shutting down the power. Therefore, fast and low power non-volatile memories are required. Only the STT-MRAM has the potential for the replacement for the cache memory. However, the write speed and current of the conventional STT-MRAM are not enough for this purpose.

Toshiba has focused on the advantage of STT-MRAM with perpendicular magnetization MTJs and pioneered its development mainly for high density memory applications. Furthermore, we have clarified that Toshiba's MTJs with the perpendicular magnetization has potential of the both higher speed and lower power switching compared to other MTJs with perpendicular magnetization or MTJs with in-plane magnetization. We have successfully achieved the development of sub-30nm ϕ MTJs which can be switched by 3ns, 50uA pulse current. The simulation results show that CPU energy reduction by 80% can be achievable by implementing these MTJs as cache memories[2-4]. In this paper, more detailed of advanced perpendicular STT-MRAM technologies and their applications will be presented. This work was partly supported by the Normally-Off Computing Project and the Spintronics Non-volatile Devices Project of NEDO, Japan.

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MRAM: Magneto-resistive Random Access Memory

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MRAM (Magneto-resistive Random Access Memory) technology [1-3] is a breakthrough non-volatile memory (NVM) technology that has proceeded through research and development phases and has become a production technology that supports product offerings [4]. Honeywell has developed and placed into production a 1Mb MRAM product [5-6]; and is developing a 16Mb MRAM product [7]. The MRAM technology described in this work applies magnetic spin-dependent tunneling which is a spin-electronic, or spintronic, effect [8] to support the read process; and inductive writing for the write process. MRAM has advantages and desired traits as a non-volatile memory including excellent write and read endurance and data retention over specified product life. This paper will outline background, characteristics, and attributes of Honeywell's 1Mb MRAM product, which is shown in Figure 1, and Honeywell's 16Mb MRAM, which is shown in Figure 2.

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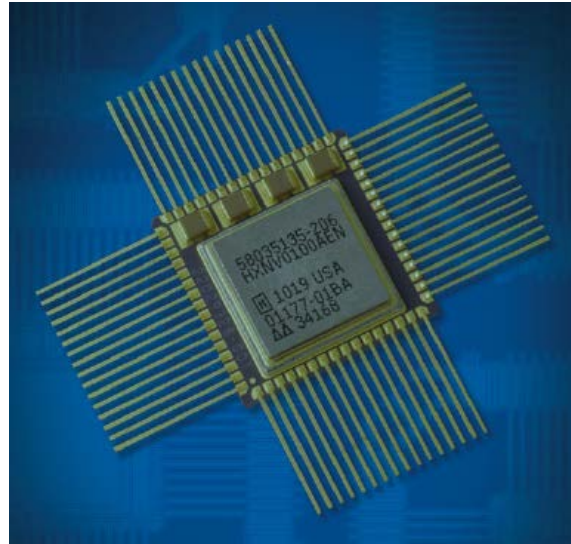


Figure 1. Honeywell's HXNV0100 1Mb MRAM product, fabricated on Silicon-On-Insulator (SOI) CMOS underlayer technology and packaged in a 64-Lead Shielded Ceramic Quad Flat Pack.

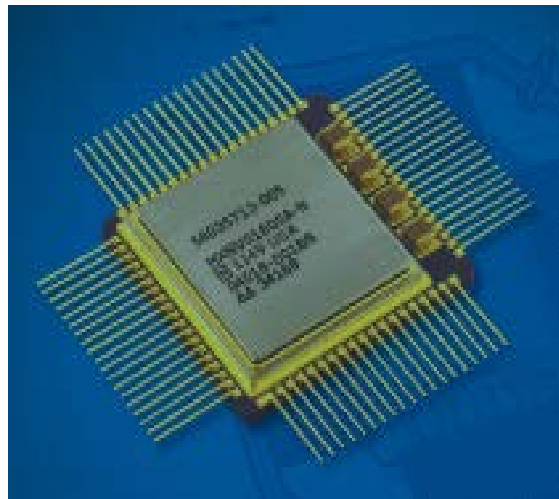


Figure 2. Honeywell's HXNV01600 16Mb MRAM, fabricated on SOI CMOS underlayer technology and packaged in a 76-Lead Shielded Ceramic Quad Flat Pack.

Selector Devices for Emerging Memory Architectures

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Many emerging nonvolatile memories (NVM) have simple two-terminal structures compatible with high-density crossbar array architectures [1]; however, large number of sneak paths in crossbar memory arrays significantly degrades reading/writing performance. Selector devices reduce the impact of sneak paths and enhance the functionality of crossbar arrays. Both asymmetry and nonlinearity in device characteristics can provide device-selection functions [2-5]. Fig. 1 lists different categories of memory selector devices. Selector devices should have large enough resistance difference in the conductive- and blocking-states, measured by *rectification ratio* of diode selectors or *nonlinearity ratio* of nonlinear selectors. They also need to provide sufficient *maximum ON current* to switch memory elements and preferably have comparable scalability as memory elements. Diode selectors reduce sneak current by blocking reverse-direction leakage; however they only work for unipolar memory elements. High rectification ratio can be achieved in diode selectors but maximum ON current is still limited (often by contact resistance). Nonlinear selectors enhance array functionality by increasing effective resistance of sneak paths and provide solutions for bipolar memory elements. Volatile switches can also work as memory selectors but voltage redistribution after switching requires balanced resistance in the selector-memory combination. Detailed analysis of these selector device options will be discussed in this presentation.

A comprehensive crossbar array model is developed to assess array performance with different types of selector devices [6]. Selectors decrease line resistance induced voltage decay by reducing array leakage (Fig. 2a), which helps to improve the current/voltage delivered to selected junctions during switching operations (Fig. 2b). However, selectors also divide junction voltage with memory elements and decrease the effective voltage available for memory operations (Fig. 2c). Sensing margin is significantly improved by selector devices without which sensing signal would be buried in sneak current noise. Compatibility between memory and selector characteristics plays a critical role in array performance. Tradeoffs often exist between selectivity and efficiency in crossbar memory arrays with selectors, which should be considered in array design and selector engineering. Memory devices with intrinsic self-rectifying or nonlinear characteristics may be utilized to design self-selecting memory arrays [5]. However, it is challenging to optimize memory devices for both switching performance and device selection functionality. Quantitative analysis of crossbar array design and selector device options will be discussed in this presentation. The potential of emerging memories for data-centric applications may eventually be constrained by the availability and property of selector devices rather than their own switching characteristics.

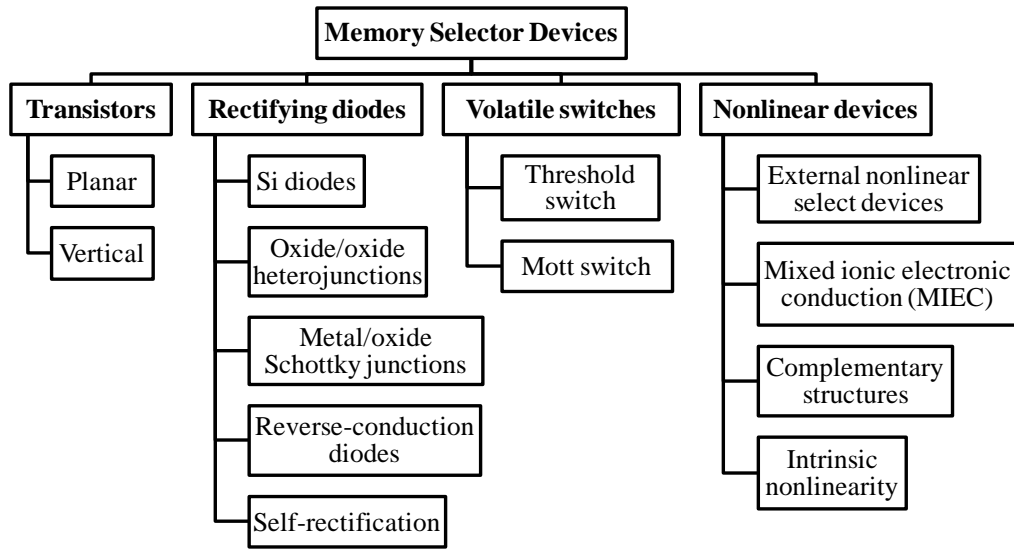


Fig. 1 Taxonomy of memory selector devices.

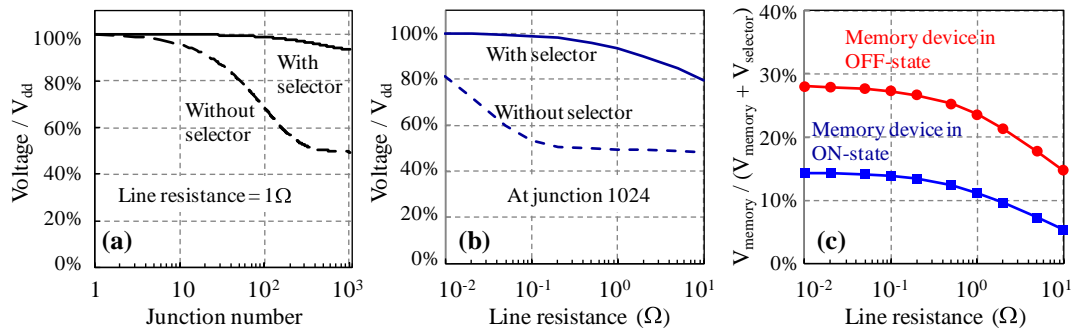


Fig. 2 (a) Line voltage decay in a crossbar array up to 1024 junctions along a line for bit-to-bit line resistance of 1Ω . Selectors significantly reduce voltage decay. (b) Voltage at junction 1024 for bit-to-bit line resistance from 0.01Ω up to 10Ω . (c) Percentage of memory voltage in a memory-selector combination for memory device in ON and OFF states. A partial bias scheme (i.e., "1/2 bias" scheme) is used in the calculation of all three figures.

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Investigation of resistive memories (RRAM) potentialities – Switching phenomena and retention performances

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Resistive memories are seen as one of the most promising candidates for Flash replacement for the future generations [1-2]. Indeed, they offer low operating voltages, low consumption, fast program erase, and can be easily integrated in the BEOL of an advanced logic circuit. They are based on the reversible formation and disruption of a conductive filament in a resistive layer. In the most studied configuration, the filament can be obtained by migration of oxygen vacancies in transition metal oxides (OxRAM) or by the dissolution of an active electrode in an oxide or chalcogenide based electrolyte (CBRAM). Nevertheless, today, a clear understanding of the involved mechanisms ruling the RRAM operation is still missing. Indeed, the origin of the filament formation and dissolution should be further clarified to allow RRAM industrialization and their pervasion in the market. In this work, we will address these issues and discuss about the potentialities of RRAM as non volatile memory technologies.

Concerning CBRAM (Fig.1), we investigated how the engineering of the electrolyte can modify the memory characteristics. In particular, we demonstrated that CBRAM based on GeS₂ electrolyte doped with Antimony (Sb) offers both ultra low-power performance and increased conductive filament thermal stability during high temperature retention [3]. We analyzed the mechanisms at the origin of the filament formation and dissolution in SET, RESET, disturb and retention regimes [4]. The impact of Sb at the atomistic and device level is analyzed by means of material and electrical measurements, empirical model [5] and 1st principle calculations.

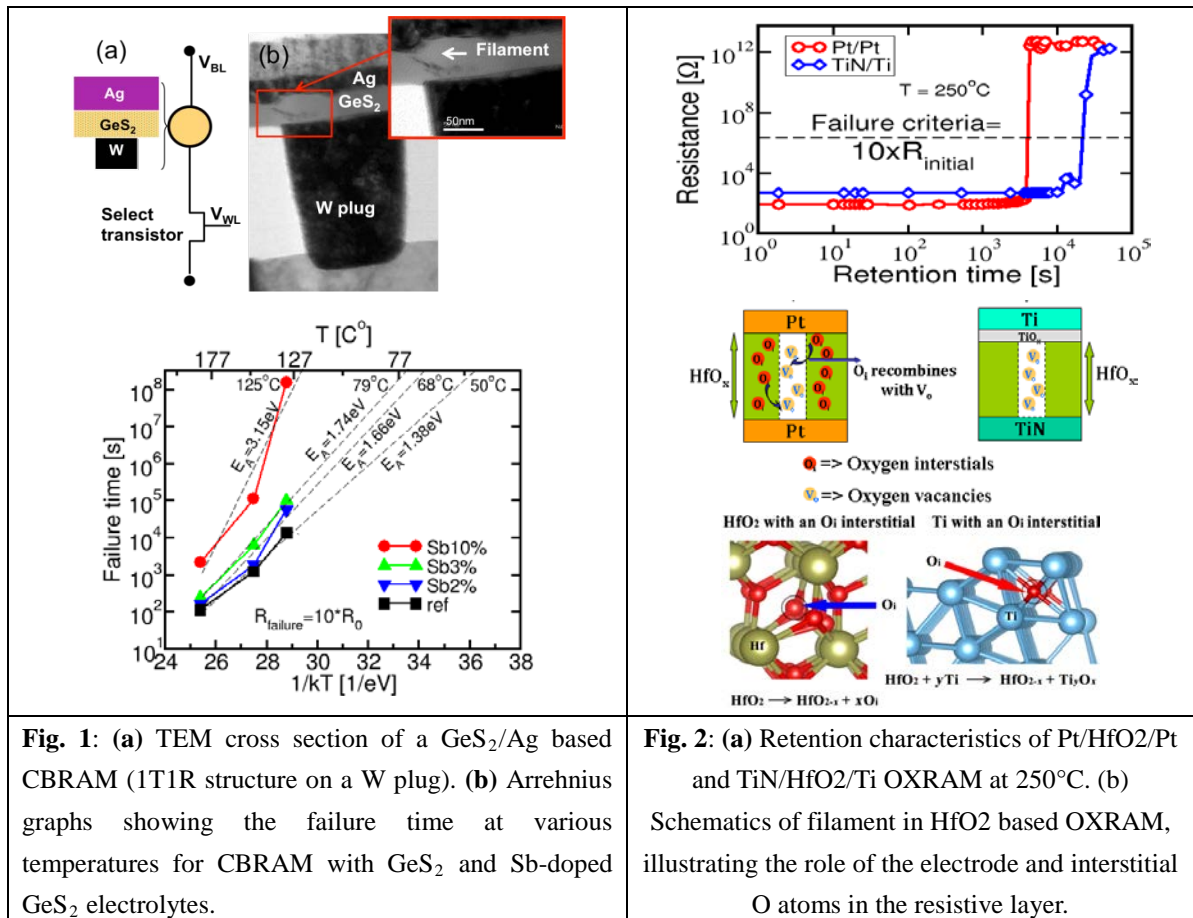
Concerning OxRAM, we will investigate the role of the electrode on the memory performances [6]. The memory behavior at high temperature (up to 200°C) will be studied to evaluate the potentialities for automotive embedded applications [7]. Starting from experimental data, we used physics-based RRAM modeling and first

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principle calculations to show that the concentration of oxygen interstitial (O_i) ions significantly depends on the metal electrodes, being much larger for RRAM devices with Pt electrodes, as Ti is easily oxidized [8]. The lower O_i concentration in HfO_x with Ti electrodes results in improved retention and thermal stability (Fig.2).

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New Insights into Redox Based Resistive Switches

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Resistive switching memories (RRAM) are considered as one of the most promising candidates to overcome the conventional FLASH technology which will reach its scaling limitations within the next years. Among other promising RRAM technologies redox based resistive switching memories (ReRAM) attracted high attention due to their scalability to almost atomic level, thus ensuring high information storage density and low power operation. In particular, ReRAMs based on the valence change mechanism (VCM) and electrochemical metallization effect (ECM) are in the scope of current research and are theoretically described as memristors or memristive systems. This talk summarizes recent research highlights on both ECM- and VCM-type resistive switches. The resistive switching effect and preceding redox reactions on the nanoscale are analyzed in detail for the case of typical prototype material systems including AgI, SiO₂ and SrTiO₃. Special attention is paid to strongly non-linear effects such as the exponential relation of switching time and switching voltage studied on a time scale of more than 12 orders of magnitude. Finally, the necessity to extend the theory of memristors and memristive systems will be addressed in the light of the recent discovery of nanobatteries inside redox based memory devices.

AlO_x/WO_x Bilayer Resistive Random Access Memory

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Resistive random access memory (RRAM) has gained significant attentions because of its promising characteristics for next-generation nonvolatile memory applications. Recent studies show that multi-layer structure exhibits better resistive switching characteristics than single layer RRAM devices. It is reported that multi-layer RRAM devices have better switching uniformity[1], higher cycling endurance[2], longer retention[3], lower operation current[4], and multilevel application[5].

In this paper, an AlO_x/WO_x bilayer RRAM cell was fabricated in a commercial foundry using 0.18μm CMOS technology with five major fabrication steps: 1) deposition and chemical mechanical polishing (CMP) to form the W-plug; 2) rapid thermal oxidation (RTO) to produce WO_x layer; 3) pattern and dry etch to clean the WO_x in via regions; 4) Al deposition to form top electrode; 5) rapid thermal annealing (RTA) to form the AlO_x layer by inter-diffusion between Al and WO_x layers.

Typical I-V sweeping curve of AlO_x/WO_x bilayer RRAM is shown in the figure 1. By applying negative RESET and positive SET sweeping voltages, bilayer RRAM switches between high resistive state (HRS) and low resistive state (LRS) with operation current at about 10 μA. The inset image in figure 1 shows that the initial resistance, LRS and HRS have significant improvement from single WO_x layer RRAM cells.

The switching mechanism of AlO_x/WO_x bilayer RRAM structures is proposed as shown in the figure 2. During the RTA treatment, an AlO_x layer was formed due to the inter-diffusion between Al and WO_x layers. Al, W, AlO_x, WO_x were found in this layer based on XPS depth analysis. When positive voltage is applied on Al TE, oxygen ions move out of WO_x or AlO_x (most probably WO_x since W-O has weaker bond strength in comparison to Al-O bond). In some preferred locations, such as grain boundaries or defect locations, conductive filaments could be formed which induces the resistance drop to low state. When negative voltage is applied on top Al electrode, the oxygen ions move back to conductive path, which break the conduction path and bring the cell back to high resistive state. Each layer undertakes different roles for this bilayer RRAM device: the lower WO_x layer provides W ions to dope the AlO_x layer. While the upper AlO_x layer is the resistive switching layer which enable oxygen ions move to form and rupture the conductive paths. Stable and excellent resistive switching characteristics could be observed from this fully CMOS compatible RRAM structure.

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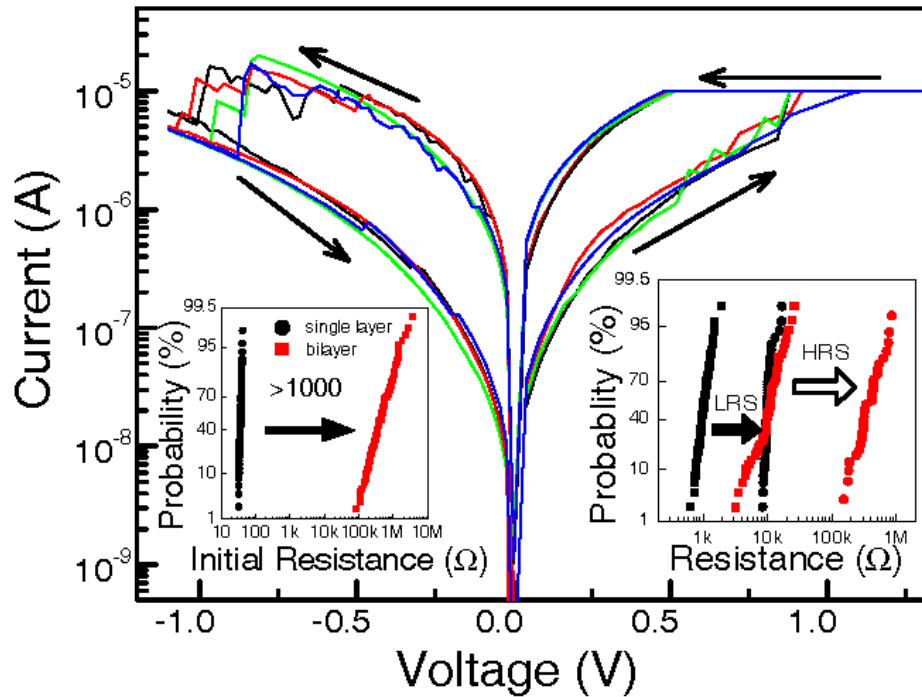


Figure 1. Typical I-V sweeping curves of AlO_x/WO_x RRAM devices and the comparison of initial resistance (left inset imagine) and HRS/LRS (right inset imagine) between single WO_x RRAM and bilayer AlO_x/WO_x RRAM.

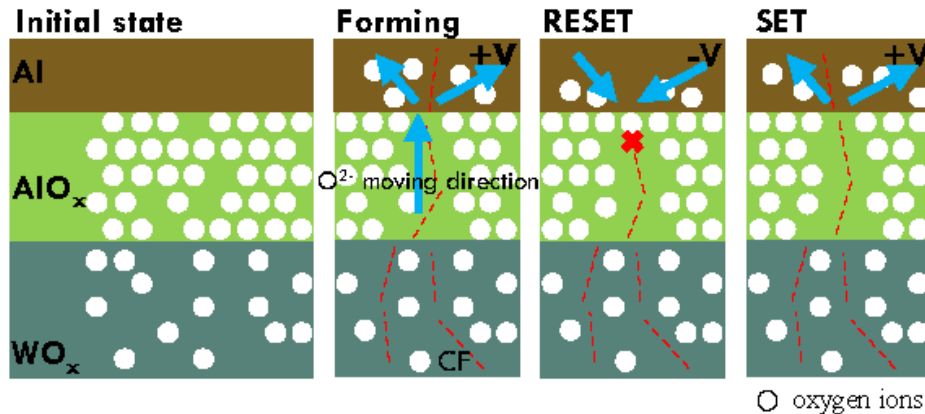


Figure 2. Schematics of resistive switching mechanism of AlO_x/WO_x RRAM devices in initial state, forming process, RESET/SET process.

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Mechanism of localized electrical conduction at the onset of electroforming in TiO₂ based resistive switching devices

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Transition metal oxide based non-volatile resistance switching devices are promising candidates for next-generation solid state memory technology. TiO₂ based devices in particular have gained significant research interest over the last several years [1,2,3]. However, despite many demonstrations of promising device performances, the understanding of the physical mechanism that drives the resistance switching process remains an open area for debate. Electroforming, a one-time initialization step, which often must be performed prior to obtaining stable resistance switching characteristics is another aspect that remains poorly understood. It has been proposed that the motion of oxygen ions (or vacancies) may lead to the physical and electrical changes observed during electroforming and resistance switching [1,4,5], and indeed we have made in situ TEM observation of defect motion during switching. However, the exact nature of this vacancy migration and its relationship (if any) to reversible and permanent changes in electrical transport requires further investigation.

In this work, a pulsed voltage method building on past work [6] has been employed to investigate the events leading up to the onset of localized current conduction during electroforming of TiO₂-based resistive switching devices. This technique uses pulsed I-V measurements as a function of stage temperature shown in Figure 1 for thermometry purposes. By collecting the I-V data before ohmic losses can cause any significant heating, a true mapping between I, V and internal device temperature is possible.

Using this thermometry technique, the temperature rise at the onset of electroforming is found to vary from 25°C – 300°C as the pulse amplitude is varied between 3 - 8 V, and the width is varied between 10 ns – 100 ms. From a tabulation of forming time vs voltage and device internal temperature, it is possible to extract an effective activation energy for forming. This effective activation energy of the forming event is found to be strongly dependent on the electric field strength and varies from 0.7 eV at 3 V to almost zero at 8 V, as shown in Figure 2. The functional form of this dependence is not in agreement with the predictions of vacancy migration theory; rather it points toward charge trapping as the mechanism for onset of localized conduction prior to electroforming. This interpretation is supported by modeling of the measured preforming temperatures that cannot be explained without invoking reversible current constrictions events that occur prior to forming.

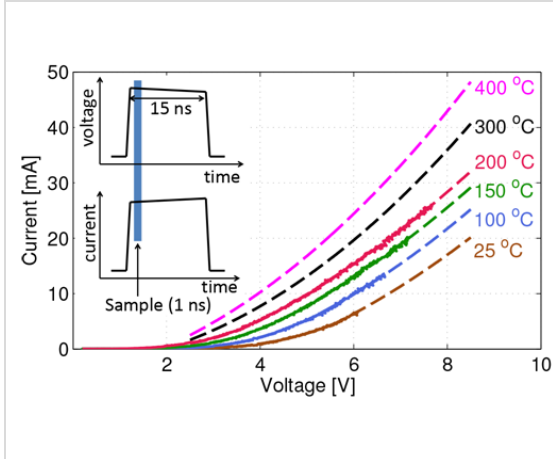


Figure 1: Pulsed I-V data collected at four different ambient temperatures on a pristine device (prior to electroforming) by sampling the current and voltage during the first 1 ns of the pulse (schematically shown in inset). Solid lines are measured data. Dotted lines are extrapolations based of measured results.

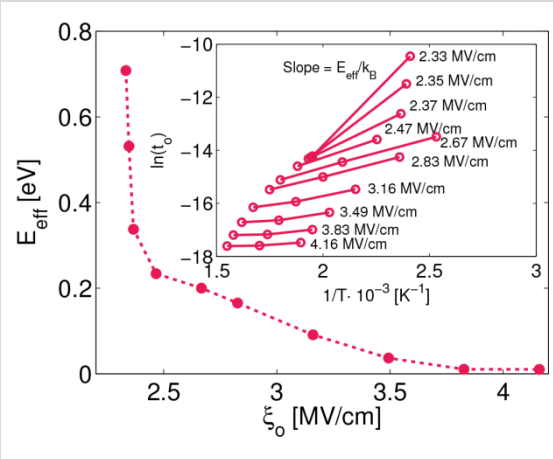


Figure 2: Effective activation energy, E_{eff} vs. electric field ξ_o at the onset of electroforming as extracted from data of forming time, t_0 , vs voltage at different device temperatures. Each point in this plot is derived from the slope of the Arrhenius plots shown in the inset.

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SiO_x resistive memory device: invisible memory and 1D-1R

1 kbit integration application

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Conventional Si-based complementary metal-oxide-semiconductor (CMOS) transistors have been the mainstay for electronic memory. However, future CMOS transistor technology faces significant challenges with respect to its fundamental scaling limitations and high energy consumption requirements [1]. Here, we make an entire 1-kilobit crossbar devices based upon SiO_x resistive memories with the integrated diodes, thereby truly demonstrating the scalable efficacy of this approach [2]. The diode-resistor (1D–1R) device in the present study exhibits high ON/OFF ratios (up to $\sim 5 \times 10^5$), low ON-power ($\sim 1.2 \times 10^{-5}$ W/bit), and low energy consumption ($\sim 6 \times 10^{-3}$ J/Gigabit) as well as excellent operational retention ($> 10^4$ s) and endurance. Furthermore, we have demonstrated that these devices enable the operation of multi-bit switching by different reset voltages, which permits higher density information storage than conventional two-state memory systems.

For invisible memory application, we fabricated highly transparent memory using SiO_x as the active material and indium tin oxide or graphene as the electrodes [3]. The two-terminal, nonvolatile resistive memory can also be configured in crossbar arrays on glass or flexible transparent platforms. As glass is becoming one of the mainstays of building construction materials, and conductive displays are essential in modern handheld devices, to have increased functionality in form-fitting packages is advantageous.

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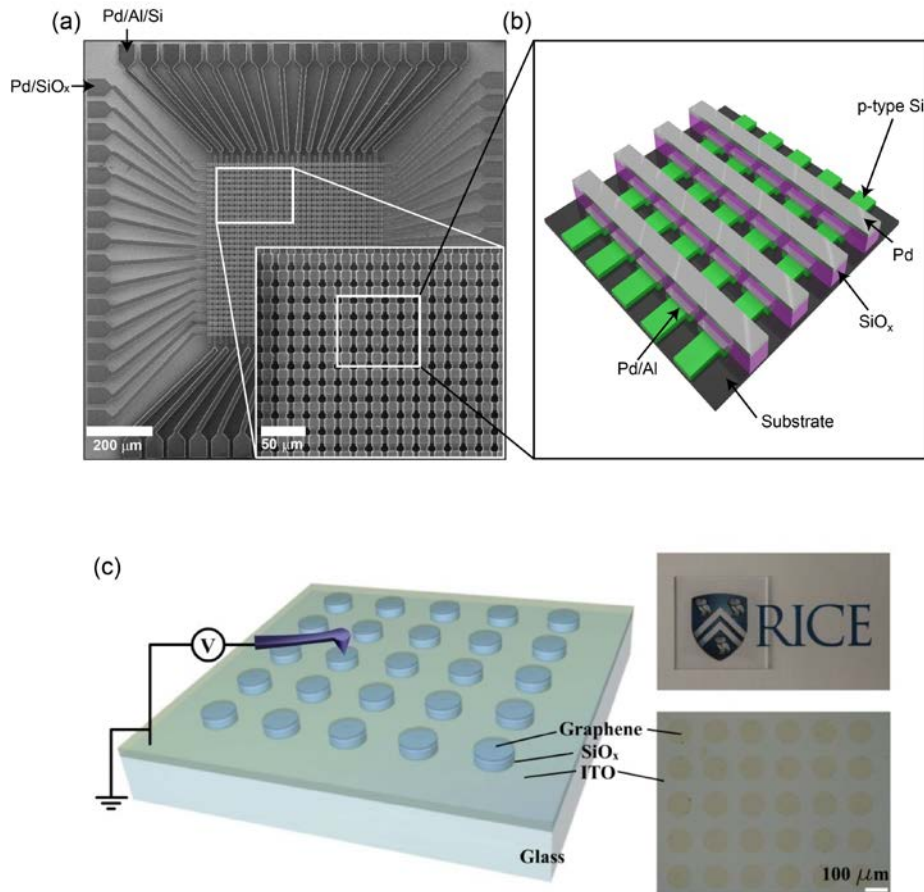


Figure. (a) SEM image of the 1 kbit 1D-1R device. The line width of junction is 10 μm . The inset shows the cells in the 1D-1R device. (b) Schematic illustration of the cells in the 1D-1R device. (c) Left panel; schematic of the G/SiO_x/ITO device arrays on a glass substrate and the setup for electrical characterization. The top right panel shows the G/SiO_x/ITO layered structure on a glass substrate and the bottom right panel shows the optical images of the G/SiO_x/ITO devices; scale bar, 100 μm .

Resistive Switching Memory Effect in a BiFeO₃ Ferroelectric Diode

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Ferroelectrics have attracted considerable attention for their nonvolatile memory applications over the past decades, and ferroelectric random access memory (FeRAM) is put to practical use. Recent studies on the resistive switching based on polarization reversal in ferroelectric tunneling junctions [1,2] and ferroelectric diodes [3,4] offer new non-charge-based memories which may have an advantage over conventional FeRAM and semiconductor charge-based memories such as flash memory.

In this study, we have developed a ferroelectric resistive switching device consisting of a multiferroic BiFeO₃ (BFO) [5]. Pt/BFO/SrRuO₃ capacitor structures showed rectifying and hysteretic current-voltage (*I-V*) characteristics, i.e., a resistive switching phenomenon. Moreover, in *I-V* characteristics measured at a voltage-sweep frequency of 1 kHz, positive and negative current peaks originating from ferroelectric displacement current were observed under forward and reverse bias prior to set and reset switching processes, respectively. This result suggests that polarization reversal is involved in the resistive switching effect. The detailed study on resistive switching properties of the device suggested that a dielectric dead layer formed at the Pt/BiFeO₃ interface plays a crucial role in the emergence of the ferroelectric resistive switching. We also confirmed that the resistive switching can be induced by applying voltage pulses with a duration time of 100 ns. The devices showed endurance of >10⁵ cycles and data retention of >10⁵ s. Moreover, unlike conventional resistive switching devices made of metal oxides, no forming process is needed to obtain a stable resistive switching effect in our ferroelectric resistive switching devices.

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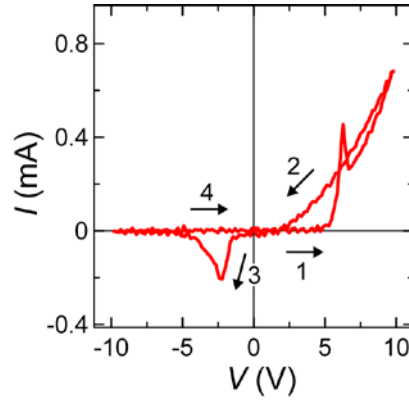


Fig. 1. I - V characteristics of a Pt/BiFeO₃/SrRuO₃ ferroelectric resistive switching device measured at a voltage-sweeping frequency of 1 kHz. Arrows and numbers indicate the sequence of the hysteric current loop. Positive and negative current peaks originating from ferroelectric displacement current were observed at $V = +6.3$ V and -2.3 V, respectively.

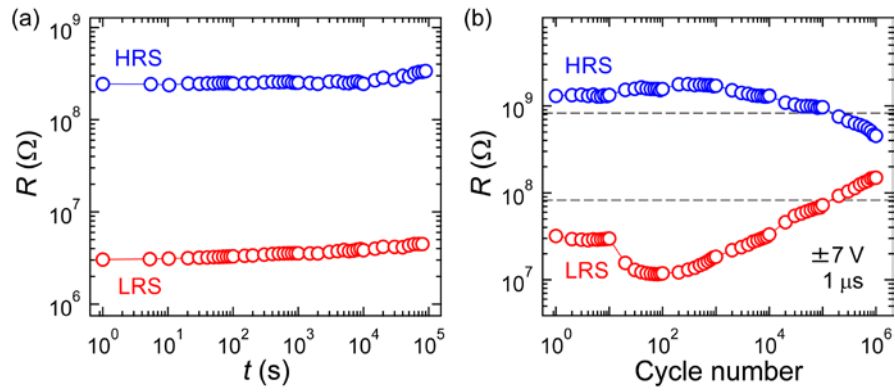


Fig. 2. a) Data retention and b) endurance characteristics of a Pt/BiFeO₃/SrRuO₃ ferroelectric resistive switching device. Broken lines in b) represent a memory window of $R_H/R_L = 10$.

Ferroelectric Memories based on Resistive Switching

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Ferroelectrics comprise a class of polar materials with an electrically switchable spontaneous polarization allowing their use as binary data storage media in nonvolatile ferroelectric random access memories (FeRAMs). Currently available FeRAMs utilize a destructive read process of stored information, which requires the memory cells to be re-written by a relatively high voltage, increases the read time and limits the scalability. An alternative approach to read operation is based on the polarization-driven resistive switching, known as the tunneling electroresistance (TER) effect. If the ferroelectric film is sufficiently thin (of the order of a few nanometers), conduction electrons can quantum-mechanically tunnel through the ferroelectric barrier. By flipping the polarization of the ferroelectric barrier it is possible to change an internal electronic potential profile and, hence, alter the transmission probability and produce the TER effect. Using this effect, reading of the polarization state can be performed in a non-destructive manner by measuring the resistance of the memory cell to a relatively low voltage. Since TER does not depend on the amount of the stored charge it allows a much better scalability. In addition to being highly relevant to technological applications, the TER effect concerns the fundamental issues of the critical behavior and switching dynamics in ultrathin ferroelectric films, role of structural defects and interfacial properties in the transport behavior. Maintaining a stable polarization in ultrathin ferroelectric films is essential for exploiting the functionality of these materials in nonvolatile memory applications. This talk will focus on investigation of the fundamental relationship between retention of ferroelectric polarization and related electronic transport behavior in high-quality single-crystalline BaTiO_3 tunnel junctions by means of piezoresponse force microscopy (PFM) and pulsed switching current measurements (PUND) [1]. It is shown that although polarization is stable in ultrathin BaTiO_3 films with no top electrodes, deposition of top electrodes (SrRuO_3) results in severe polarization relaxation. This effect is a consequence of strong effective depolarizing fields due to unfavorable interface terminations with the deposited electrodes, as opposed to more complete screening in the films by adsorbed charges on the free surface. Several approaches to enhance polarization retention in the case of a deposited electrode, including strain engineering and control of electrically boundary conditions, were explored. In particular, first-principle calculations based on density functional theory show that engineering of the atomic termination at the electrode interface by insertion of ultrathin dielectric layers can alleviate stability issues in the case of SrRuO_3 electrodes [2].

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Ferroelectric Memories

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The field-polarization hysteresis in ferroelectric materials has been applied to nonvolatile memory for many years with only partial success [1, 2]. Unlike ferromagnetic materials, the operation of ferroelectric switching is often entirely CMOS compatible [1]. The ferroelectric capacitor has a metal-ferroelectric-metal (MFM) structure can have a long retention time as the retention state in either polarization does not have a depolarization field, as the polarization charge is directly screened out by the image charges in the neighboring metal. However, read can only be done by the direct displacement current difference, which severely limits its area scaling. The FeFET has a metal-ferroelectric-insulator-semiconductor (MFIS) gate structure and can use the channel current to read nondestructively the polarization state, and can have much more aggressive area scaling [1]. However, the polarization charge cannot be fully compensated, which gives a sizable depolarization field that limits the retention time to a few minutes [2].

We will present a new FeFET structure in Fig. 1 where the nonvolatile charge can be injected to specific places to decrease the depolarization field and hence retention can be significantly enhanced [3, 4]. During program/erase operations in Fig. 2, the polarization switching and charge injection help each other in a distinct two-step process [5]: 1) a fast (10–100 ns) DRAM mode with $\sim 10^3$ seconds of retention, associated with ferroelectric switching, and 2) a slower (0.1–1 ms) Flash mode with long retention time, from charge tunneling into the floating nodes. The complementary characteristics of ferroelectric switching and gate charge-injection enable low-voltage program/erase (± 8 V), reasonable memory window (0.8 V) and long retention time. Devices were fabricated with the lead zirconium titanate (PZT) thin film as the ferroelectric layer and Au nanocrystals for gate-injected electron storage. Pulsed programming measurements were also performed to distinguish the memory window obtained from the two mechanisms in hybrid DRAM and Flash operations. We will finally present the device design theory and the choices of the ferroelectric material for optimal performance.

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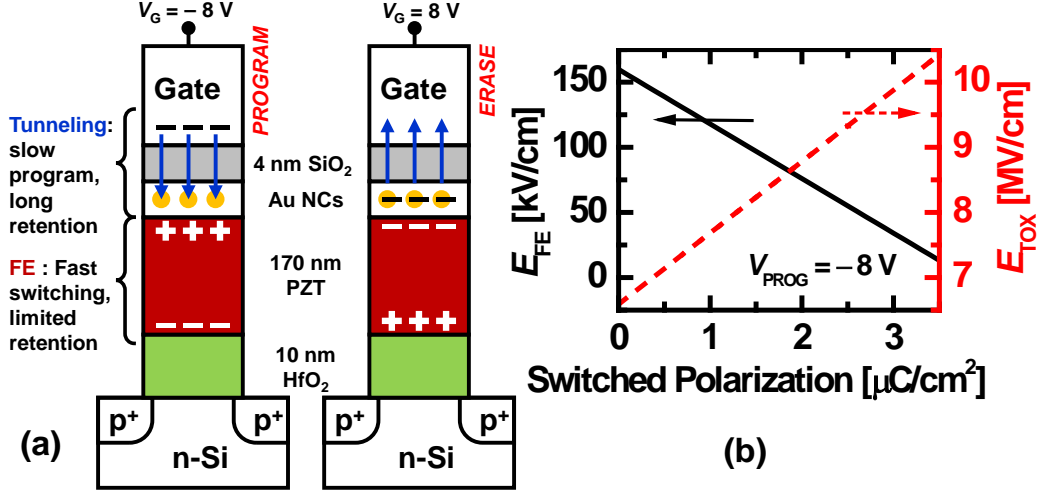


Fig. 1. (a) Schematic of ferroelectric-assisted DRAM-Flash hybrid memory. (b) Dependence of electric field in the ferroelectric (E_{FE}) and tunnel oxide (E_{TOX}) with switched polarization (P) during program operation.

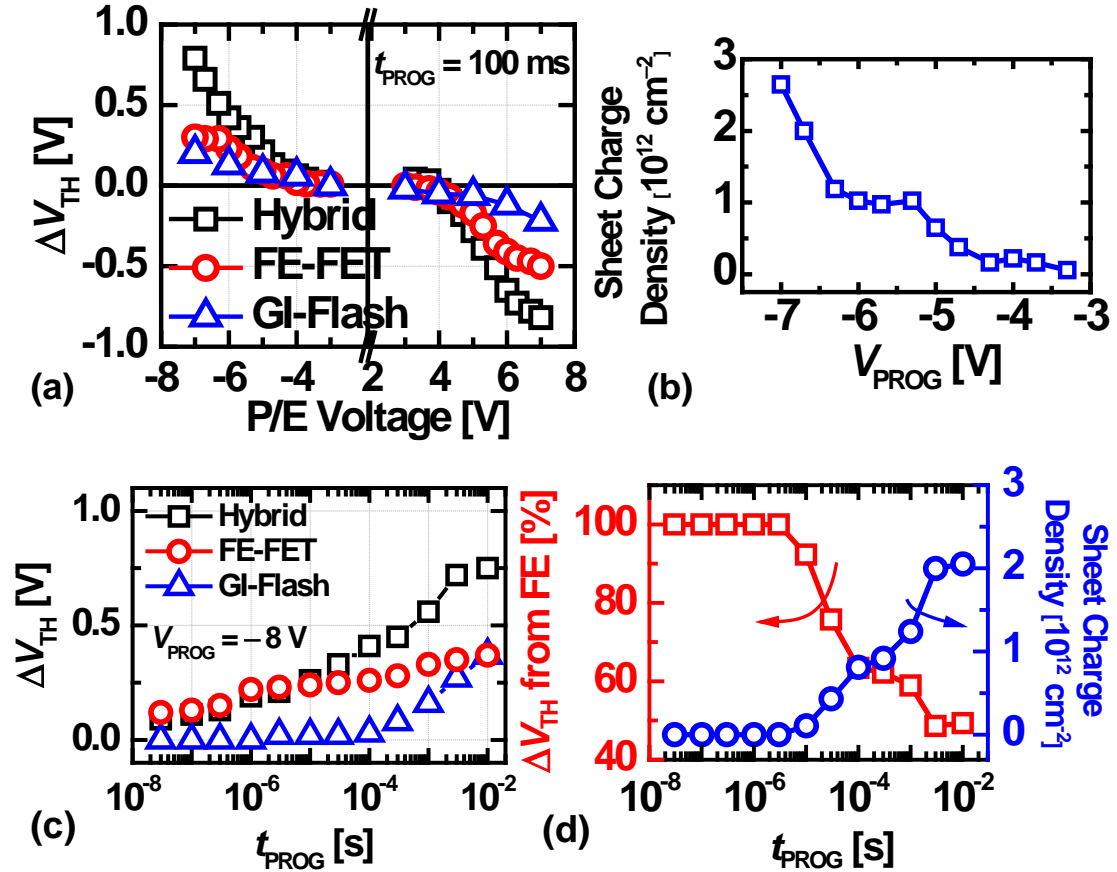


Fig. 2. (a) Summary of program and erase ΔV_{TH} measurements for hybrid, MFIS FE-FET and gate-injection (GI)-Flash device. (b) Estimated sheet charge density of electrons stored in the Au NC layer as a function of V_{PROG} in the hybrid device. (c) Pulsed program measurements for hybrid, FE-FET and GI-Flash devices at $V_{PROG} = -8$ V. (d) Estimated contribution of ferroelectric polarization to total ΔV_{TH} and sheet charge density as a function of t_{PROG} .

A Dual-Channel Ferroelectric-Gate Field-Effect Transistor

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A ferroelectric-gate field-effect transistor (FeFET) that uses ferroelectric material as a dielectric layer for a metal oxide semiconductor FET (MOSFET) is of great interest for nonvolatile memory applications, since its channel conductance can be switched and memorized with low power consumption at high speed. Recently, the material which has process compatibility with CMOS circuit, such as a ferroelectric HfO_2 , has been developed [1]. However, it is difficult to fabricate a FeFET which has a good retention property due to the reaction between the ferroelectric and Si, when a ferroelectric is deposited directly on a Si substrate. We have focused on carrier conduction in the oxide heterostructure which can eliminate undesirable reaction layer. We chose an inverted staggered (bottom-gate) thin-film transistor structure as a novel FeFET. We fabricated a FeFET consisting of a oxide semiconductor of ZnO and a ferroelectric $\text{Pb}(\text{Zr,Ti})\text{O}_3$ (PZT), which gave rise to a very sharp ZnO/PZT interface. The fabricated FeFET showed electron gas accumulation and complete depletion switching due to the ferroelectric polarization reversal. As a result, it showed not only the continuous conductance modulation with wide range but also a very long retention time that exceeded 3.5 months [2], [3].

To realize highly integrated memory chips based on an FeFET, NAND cells have been investigated [4]. However, unlike a floating-gate flash memory, an FeFET is easily disturbed by reading voltage, since ferroelectric polarization can be switched at low voltages. To realize disturb-free reading, we have also developed an oxide memory (OxiM) transistor, which is that two types of FET, such as a top gate-type TFT (top-TFT) and a bottom gate-type FeFET (bottom-FeFET), are stacked with a conduction layer of thin ZnO film in common (Fig. 1). By using top-TFT, we can readout the data from FeFET without applying a read voltage to the FeFET in NAND architecture. Fig. 2(a) shows the drain current-bottom gate voltage ($I_{DS}-V_{GSb}$) characteristics of the OxiM transistor for various top gate voltages (V_{GSr}). When the V_{GSr} is +10 V, the drain current maintains almost the same value, regardless of bottom gate voltage. When V_{GSr} is -10 V, hysteresis in the $I_{DS}-V_{GSb}$ curve caused by the polarization of the ferroelectric layer is observed. The channel conductance of the top-TFT and the bottom-FeFET can be controlled independently by the top gate and the bottom gate, respectively. Therefore, the top-TFT can operate as a select-transistor regardless of the polarization of the memorized FeFET. As shown in Fig. 2(b), we are able to read the data from the selected cell in the NAND-type OxiM by applying a voltage to the top gate while reading. Disturb-free reading has been achieved, since no voltage is applied to the unselected ferroelectric gates.

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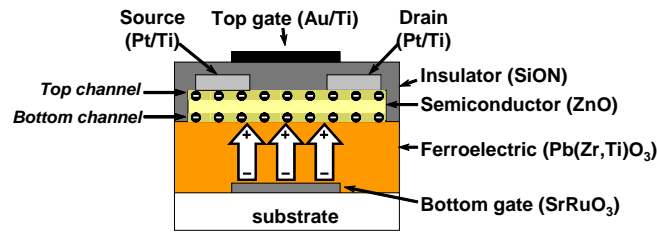


Fig. 1. A schematic image of an oxide memory (OxiM) transistor consisting of a top-TFT and a bottom-FeFET.

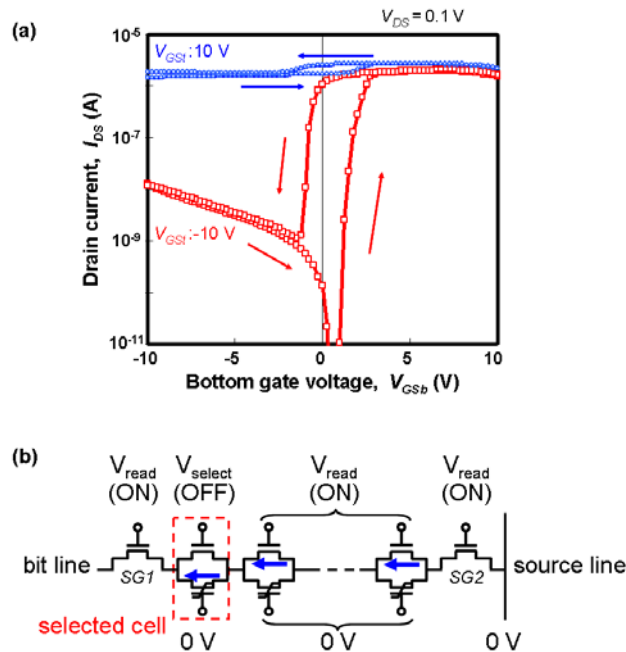


Fig. 2. (a) Drain current-bottom gate voltage (I_{DS} - V_{GSb}) characteristics of an OxiM transistor, when the top-TFT is ON ($V_{GSr} + 10$ V) and OFF ($V_{GSr} - 10$ V). (b) A schematic circuit diagram and the sequence of detecting the conductance for a NAND Oxim transistor cell, which consists of the serially connected OxiM transistors.

Evolution of PRAM application with challenging technologies

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Recently, PRAM(Phase change Random Access Memory) has been commercialized for mobile application. PRAM has been paid attention due to its fantastic characteristics, such as shrinkability, endurance, retention and so on.

At first stage, PRAM has been adapted to replace NOR flash by using conventional PRAM having moderate endurance and speed. Nowadays, advanced materials and technologies make PRAM possess better reliability and performance, leading to the evolution of PRAM application from NOR replacement to newly applications such as effective interface, innovative system and brain-inspired computation.

Effective Interface: PRAM can be operated by bit alternatively and at low voltage compared to conventional Flash memories. These advantages make DRAM-interface PRAM possible, which makes chipset simplified and effective. This application has been already applied to IT systems. Furthermore, many researchers pay attention to the new application utilizing the advantage of PRAM characteristics such as fast latency and better reliability for innovative system.[1]

Innovative System: The architecture of computing system consists of CPU, memory(DRAM) and storage(NAND/HDD). Inconveniently, there is a big latency gap between memory(<100ns) and storage(~100us), which can make the system complicated and inefficient. This latency gap problem can be resolved by taking advantage of PRAM unique properties, if some characteristics of conventional PRAM is improved. Nowadays, advanced materials and technologies are developed to have sufficient speed and endurance for this application, so called memorage (memory+storage). Besides, MLC and stack technology will be discussed for increasing PRAM density. Advanced PRAM technologies make computing system cost effective, energy saving and higher performance innovatively.

Brain Inspired Computation: Moreover, PRAM has started to study new application for brain inspired computing, which can generate paradigm shift of computation structure from Neuman to Cognitive type[2]. In this study, we demonstrate that a phase change memory cell array is able to emulate the neuron spiking as well as synaptic functions by introducing novel core algorithms, which enables PRAM to be a strong candidate for neuromorphic applications.

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Manipulating Material Interfaces for Low Current PCRAM

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PCRAM's near ideal non-volatile memory characteristics have provided increasing attractions to be used for electronic systems. However, the high RESET current requirement is still one of the most challenging issues for PCRAM to achieve high density memory. To increase the density, many methods have been pursued to minimize the physical size. Besides the size scaling, researchers have also put a lot of efforts beyond scaling and process innovation to include novel cell structures to enhance the joule heating in the RESET process. The reported structures include approaches to reduce the heat loss and to increase the heating efficiency [1-3]. The interfaces between phase change materials and surrounding materials, and their electrical and thermal properties are critical factors for power consumption [4]. In this talk, the high current issue will be discussed and tackled through the material interface engineering with two complementary approaches. Artificial layer structures were implemented to manipulate the materials' properties to minimize the heat loss from the surrounding dielectric and contact electrodes. Meanwhile, the carrier transport across material interfaces were evaluated and significantly enhanced through a new carrier injection mechanism. More details will be presented at the conference.

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Chalcogenide Memristors for Electronic Synapses

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Neuromorphic computing is an attractive approach to overcome the Von Neumann bottleneck in traditional computing architecture, which refers to the limited data transfer rate between the CPU and the memory units and severely impedes the enhancement of the computing capacity [1]. Memristors or memristive devices with gradual resistance/conductance tuning properties have been proposed to act as electronic synapses with plastic synaptic weight. Based on these devices, some representative synaptic functions have been implemented, such as spike timing dependent plasticity (STDP) and memory consolidation [2,3]. Moreover, STDP, a basic rule for memory and learning in brain, was successfully demonstrated in chalcogenide-based phase change memories utilizing the multilevel resistance states due to partial crystallization/amorphization properties [4,5].

In this talk, we will present $\text{Ge}_2\text{Sb}_2\text{Te}_5$ and AgInSbTe based memristors and describe work on synaptic plasticity modification in these devices [6,7]. The memristance of chalcogenide memristors could be classified as two types: intrinsic and extrinsic memristance. The former originates from the charge trapping and detrapping in the material defects, whereas the latter stems from the electrochemical metallization effect of the active electrode (Ag, for instance). Both mechanisms facilitate us to modify the device conductance in an analog way, therefore enable plastic synapse emulating. By applying designed pre- and postsynaptic spikes to the two terminals of the memristors, STDP functions could be realized.

We are going to demonstrate higher cognitive functions base on above results. Our work may pave a fresh way to combine data storage and processing together, similar to brain function, promoting the development of memory devices from the dimension of efficiency, rather than speed and size.

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DFT simulations of the crystallization of the phase-change material $\text{Ge}_2\text{Sb}_2\text{Te}_5$: Insights on nucleation and percolation

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Phase change materials (PCM) function in commercial rewriteable optical disks (DVDs, Blu-ray Disc) and nonvolatile computer memory (PC-RAM) because the amorphous-crystalline transition is rapid, reversible, and accompanied by changes in the optical and electrical properties. The amorphous structures of PCMs are difficult to determine, and the nature of the ultra-fast crystallization mechanism remains the subject of much study and speculation [1]. We have performed two large scale density functional simulations (several hundred atoms over hundreds of picoseconds) of crystallization in the prototype "nucleation dominated" phase change material $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST-225) and can provide details of the changes in order as crystallization proceeds.

Our first DF/MD simulations [2] were on a 460-atom sample at 500, 600, and 700 K for up to 600 picoseconds, where crystallization was promoted by fixing the structure of a crystalline "seed" (58 atoms, 10% vacancies, see Figure 1). The second simulations were also on a 460-atom sample at 600 K, but with no constraints on the geometry. The density was adjusted during the simulation to allow for the difference between the amorphous and crystalline forms. Crystallization occurs in stages and was complete within 0.3-1.1 ns, depending on the simulation parameters (constraints, temperature). The structural changes were monitored by calculating the pair distribution functions, appropriate order parameters, the number of "wrong bonds" (bond pairs that do not occur in the ordered form), the variation in the cavities, and the electronic density of states. The simulations reveal the course of the crystallization process at the atomistic level, and the important stages include pre-structuring, nucleation, percolation, and final (rapid) collapse to the crystalline state. Interestingly, the behavior of the individual elements (Ge, Sb, Te) is temperature-dependent.

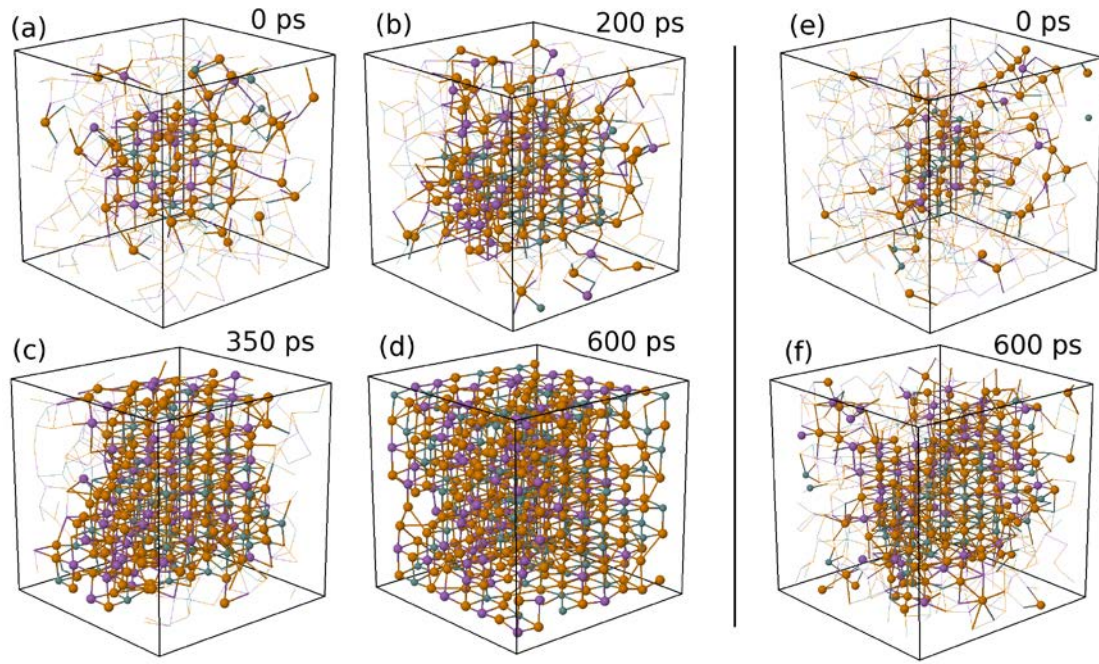


Figure 1. Visualization of (a–d) the 460-atom and (e, f) 648-atom system at different stages of crystallization at 600 K. The atoms with crystalline local environment are highlighted (ball- and stick), and the fixed cubic seed is visible in the center of (a) and (e). Green: Ge, purple: Sb, and orange: Te.

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Heat Dissipation Mechanisms in Resistive Switching Devices

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The resistive switching effect due to the formation and rupture of conductive filaments in metal oxides is a leading candidate for future non-volatile memory technology [1]. It was recently shown that the local temperature plays a key role in the switching effect [2]. We have previously presented a method to experimentally evaluate the filament temperature using HfO₂ metal-insulator-semiconductor bipolar transistor structure [3]. In light of the experimental results (Fig. 1), we discuss here the various possible heat dissipation mechanisms, and compare thermal simulations to the measured temperatures.

Several heat dissipation mechanisms are considered, which are relevant for our experiment, as well as for conventional MIM structures. The obvious heat dissipation mechanism is Joule heating of the filament. In addition, energy can be dissipated at the gap between the filament and the electrode [4]. However, if the current is injected through the gap by tunneling [5,6] the energy is not dissipated inside the gap, but at the filament tip and/or the electrode. Thermal simulations of the different possible mechanisms for the MIS structure used in [3] are shown in Fig. 2.

In the device we have studied, relatively low current levels of a few microamperes resulted in temperatures as high as 1000 K. Our devices could support 10 times larger current levels, for which our temperature measurement technique is not applicable anymore. Nevertheless, we conclude that Joule heating of the filament is not plausible in our case because a x10 increase in current is required leading to a x100 larger heat dissipation in the filament that would have resulted in unphysical elevated temperatures. We have therefore concluded that in our device heat dissipation is mainly at the electrode or filament tip.

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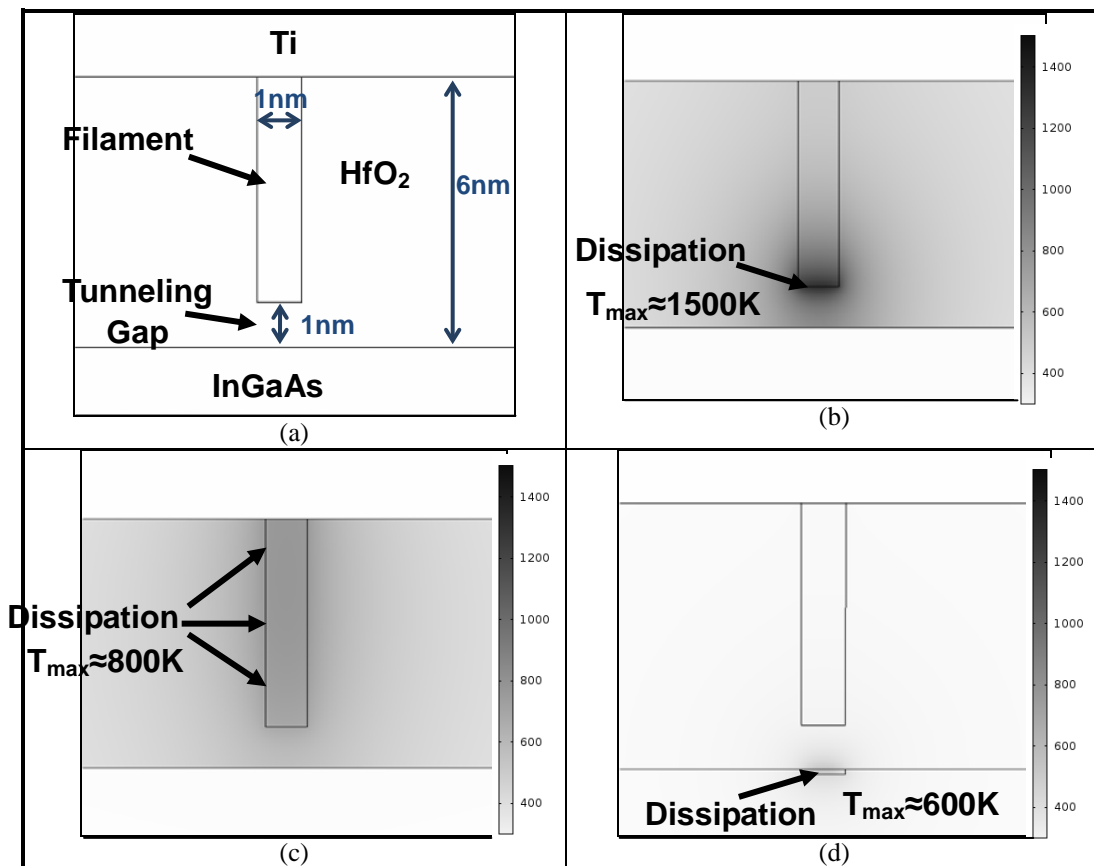
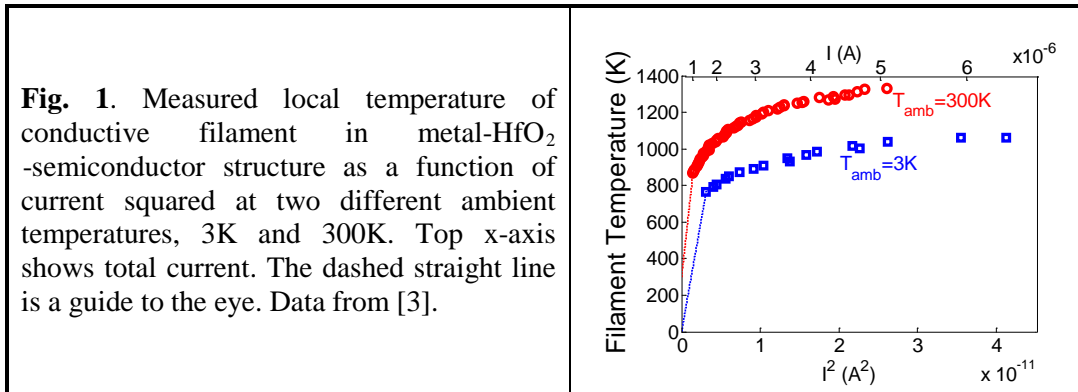


Fig. 2. Thermal simulation for the case of a cylindrical filament injecting the current through a tunneling gap. Total power dissipation is 2 μW , and the ambient temperature is 300K. Device geometry and materials are given in (a). Heat dissipation at the filament-gap interface (b), Joule heating of the filament (c), dissipation at bottom electrode (d). The maximal local temperature is indicated for each case.

CMOS-Compatible Nanometallic RRAM Devices

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Nanometallic Metal-Insulator Transition(MIT): An electron in random materials does not propagate as plane wave; instead it is repeatedly scattered and redirected to random directions in a way akin to random walk, termed *diffusion* by P. W. Anderson (1958). Along the way, the amplitude of the random-walk wave function may decay: such decay signifies electron localization and the decay distance ζ defines the localization length. A conventional random insulator has a finite ζ , whereas a conventional random metal has an infinite ζ . But if the sample size δ falls below ζ , then even a bulk-insulating sample is effectively metallic. Surprisingly, this simple idea of size-defined MIT in random materials was not revealed until our recent work [1-3] on Si(O,N)-based glassy films and ABO₃-based epitaxial films: by randomly inserting atomically dispersed conducting components into an insulating matrix (e.g., Pt to SiO₂, and SrRuO₃ to CaZrO₃), we raised ζ above δ (5-30 nm, the film thickness) and demonstrated the size-defined MIT. Moreover, a sudden decrease of ζ can be rendered at a critical voltage V_c due to injected charge that alters the landscape of Coulomb repulsion, which curtails electron “diffusion”. After voltage removal, trapped charge still remains indefinitely, and it can only be released by UV irradiation or by an opposite critical voltage. Such voltage-triggered MIT forms the basis of a new type of nonvolatile RRAM.

This Work: The present work seeks to extend the above concept to CMOS- compatible compositions. Specifically, we have verified Si₃N₄-based nanometallic materials with embedded metals ranging from main group (Al) to transition metals (Cr, Cu, Ta, Pt) all behave similarly, lending support to the universal nature of the underlying physics.[1-7] RRAM from these materials have superior statistical uniformity of their switching parameters that sets them apart from typical metal-oxide RRAM devices reported in the literature. Since the high resistance state (HRS) falls into the localization regime, its resistance exponentially increases with thickness (**Fig. 1**) in agreement with the random-walk quantum physics but in gross violation of Ohm’s law. Such thickness-sensitivity offers a new degree of freedom to engineer cell resistance. The resistance states are tunable throughout the continuum between the fully metallic state (hence the lowest resistance state, LRS) and the fully insulating state (hence the highest HRS) within a narrow range of a critical switching voltage. Yet through load resistance design, tuning can be readily performed over a wide range of device voltage. Remarkably, the critical switching voltage is independent of the film thickness (5-20 nm), cell size (down to 100 nm) and switching temperature (down to 2K), owing to the electronic nature of the trapping/detrapping mechanism. Based on scaling analysis and RC response (**Fig. 2**), we have also demonstrated that the same critical switching voltage suffices as long as the excitation pulse is not distorted by the RC delay, and that the device is switchable down to 0.1 ps speed.

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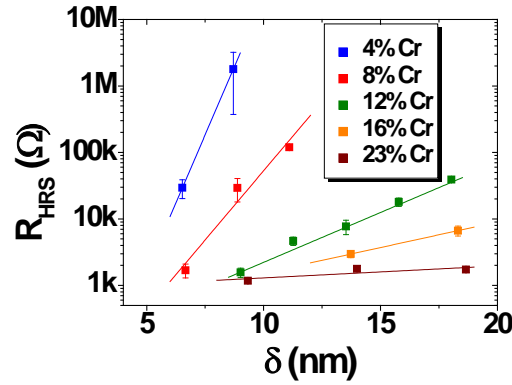


Fig. 1 High resistance values of HRS vs. thickness for different metal dopant concentrations ($\text{Si}_3\text{N}_4\text{:Cr}$ device). Exponential thickness dependence, which disobeys conventional Ohm's law, is predicted by Anderson's localization theory for random materials.

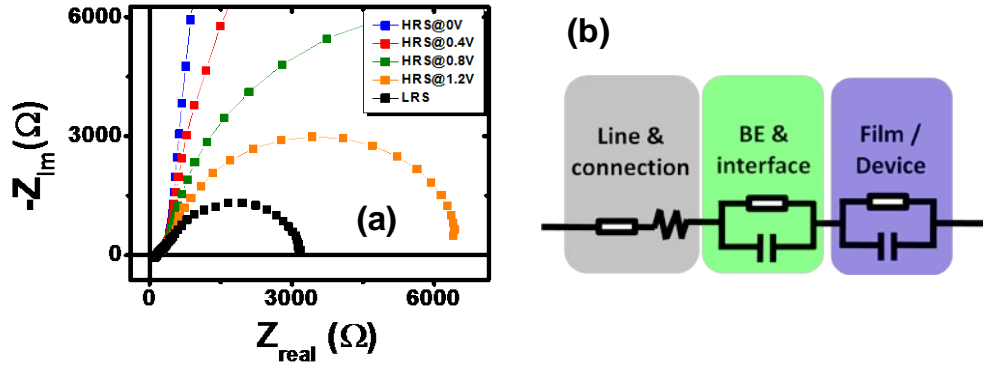


Fig. 2 (a) Cole-Cole plot for HRS at several bias voltages and LRS at 0V. (b) Schematic of equivalent circuit. In (a), the highest frequency corresponds to the point closest to the origin; as the frequency decreases, the point progresses toward the outer edge of the arc. Nanometallic film/device (see (b)) is mainly responsible for the large semicircle (incomplete ones appearing when film resistance is too high), while interface (see (b)) contributes to a small arc at high frequencies, as indicated by the apparent "distortion" of the larger semicircle near the origin. The line resistance contribution is the (Z_{real}) segment between the origin and the high frequency end of the arc near the origin.

Resistive Switching Behavior in Two-Dimensional Highly Crystalline Layered Dielectric

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We observed resistive switching behavior in highly crystalline layered insulator hexagonal boron nitride (h-BN) under high electric field. Two distinct resistive states, i.e., high-resistance state (HRS) and low-resistance state (LRS), were observed with non-volatile characteristics. Further analysis using electrical characterization confirms h-BN multilayer as the active switching material in the nano-device configuration. The resistive switching could be attributed to substitutional doping in the h-BN crystalline lattice under appropriate electric field present in the active device region, possibly resulting in formation of B-N-C complex in which electrical conductivity depends on the amount of carbon substituted in the material. Since switching is independent of the polarity of electric field, it is unipolar in nature. The observed resistive switch phenomenon in layered insulator may be potentially used in the form of either NVM or memristor, providing a possible direction to implement information storage or reconfigurable applications based on a new material system.

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Resistive Switching in Organic Memory Devices for Extended Flexible Applications

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The organic resistive memories (RRAMs) exhibit high flexibility and simple process for extended inexpensive, lightweight and transparent non-volatile memory applications. The main challenges of the organic resistive memory device and integration scheme will be discussed, as well as some typical improvements.

The resistive switching behavior of a kind of single-component polymer resistive memory device based on poly-chloro-para-xylylene (parylene-C) will be focused. With excellent chemical stability and high CMOS process compatibility, the fabricated devices exhibit excellent performance with 10^7 on/off current ratio, nano-seconds set/reset speed and low switching voltages (as shown in Fig.1), as well as good retention and cycling endurance behaviors. The related switching mechanism is studied through the electrode design and temperature dependence testing. Further improvement for low power design based on double-layer parylene-C is given, which shows extremely low reset current of sub-20nA and set current of 0.15 μ A in the area of organic RRAM, almost 10^5 times lower than the above-mentioned single-layer parylene-C cells (as shown in Fig.2). Possible mechanism for the ultra-low operating current of the double-layer organic memory device is investigated. Finally the technology tendency and possible hetero-integration of flexible memories is discussed.

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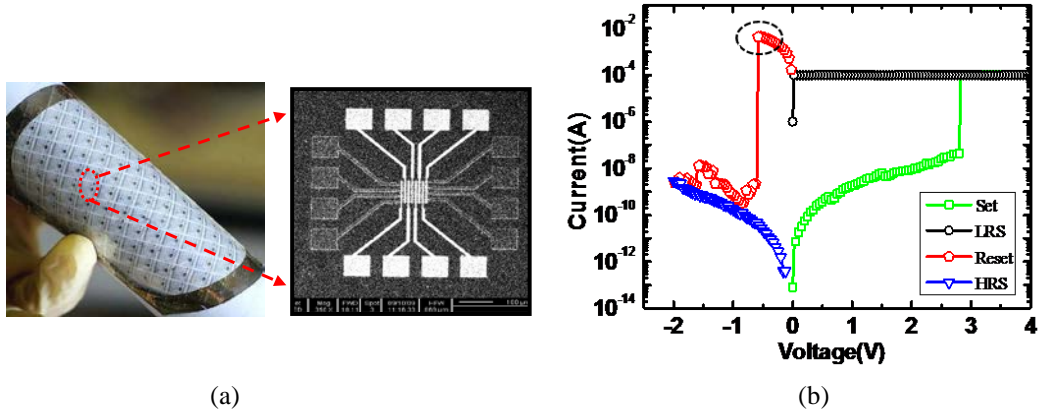


Fig.1 (a) The picture of the fabricated flexible memory devices and the SEM image of fabricated 8x8 crossbar structure of the device (b) Measured typical I-V curves of Al/parylene-C/W device in a semi-logarithmic current scale

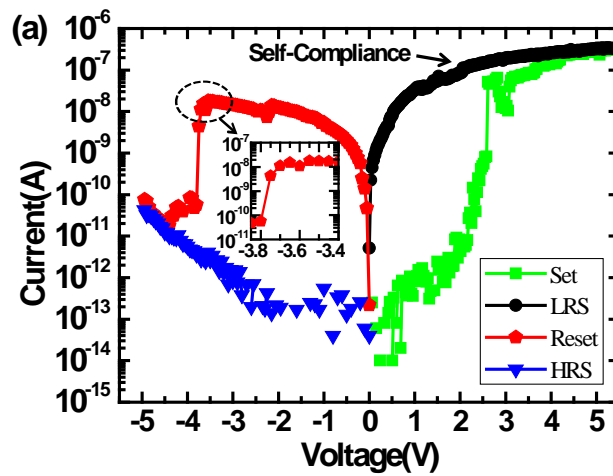


Fig.2 Measured typical I-V characteristics of Al/parylene-C/parylene-C/W double layer memory cell with extremely low operation current

Simulation and Benchmarking of Spintronic Memory and Logic

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Spintronic memory is approaching commercialization, while spintronic logic still has a long way to it. For both applications, simulations are essential to help research and development. Both require addressing two aspects: magnetization dynamics and spin transport to drive it. The talk covers the Extended Huckel theory method [1] for simulating spin transport in various materials. The magnetization dynamics is addressed by well-established micromagnetic simulators. The talk covers the results of such simulations to determine the limitations of spin torque memory and future progress via spin Hall effect switching [2]. Further, simulations of more complex logic devices, spin majority gates [3] is examined in detail. For even larger circuits, a method for simulating spin circuits [4] is outlined. Finally, performance of a wide class of spintronic devices and circuits is estimated and benchmarked against CMOS logic [5].

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Towards a Nonvolatile VLSI Processor Using MTJ/MOS-Hybrid Logic-in-Memory Architecture

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Rapid progress in recent deep submicron regime has led to the capability to realize giga-scaled embedded systems on a chip, while the communication bottleneck between memory and logic modules has increasingly become a serious problem. In addition, power dissipation and device-characteristic variation have been also the emerging problems in the recent VLSI chip.

In this paper, I present a new logic-VLSI architecture called “nonvolatile logic-in-memory architecture” as a solution to implement “ultra-low-power VLSI chips. In the nonvolatile logic-in-memory architecture, nonvolatile storage elements are distributed over a logic-circuit plane, so that it is expected to achieve both ultra-low power dissipation and shorter interconnection delay because of great reduction of global interconnection counts and volatile storage-element counts, respectively. Actually, I discuss novel nonvolatile logic circuits based on nonvolatile logic-in-memory structure using magnetic tunnel junction (MTJ) devices in combination with MOS transistors. Since the MTJ device with a spin-injection write capability is only one device that has all the following superior features as large resistance ratio, virtually unlimited endurance, fast read/write accessibility, scalability, complementary MOS (CMOS)-process compatibility, and no volatility, it is suited to implement the MOS/MTJ-hybrid logic circuit with logic-in-memory architecture. Moreover, it is also important to support VLSI CAD tools specialized in the MTJ-based nonvolatile logic-in-memory circuit because of establishing its design-evaluation environment. As typical examples of the proposed nonvolatile logic-in-memory circuitry, an MTJ-based nonvolatile look-up table circuit for an instant power-ON/OFF Field Programmable Gate Array [1], an MTJ-based bit-parallel nonvolatile Ternary Content-Addressable Memory (Fig. 1) [2], [3], and an MTJ-based special-purpose VLSI processor for real-time motion- vector extraction (Fig. 2) [4] are also demonstrated together with the fabricated test-chip results.

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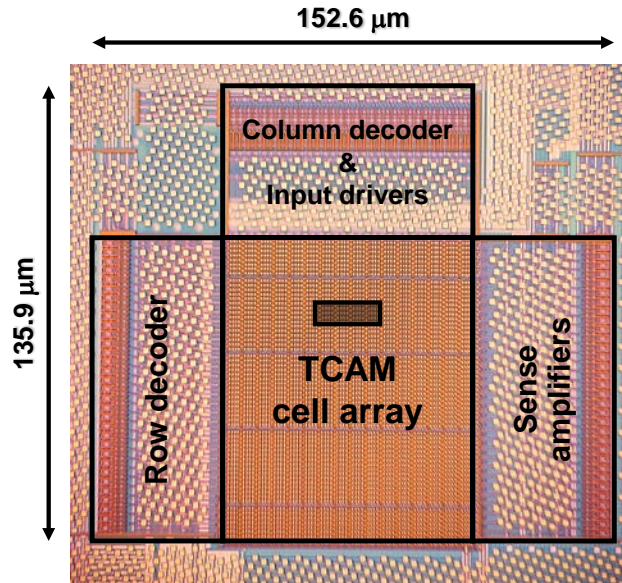


Figure 1: 2k-bit Standby-power-free TCAM test chip with nonvolatile logic-in-memory architecture.

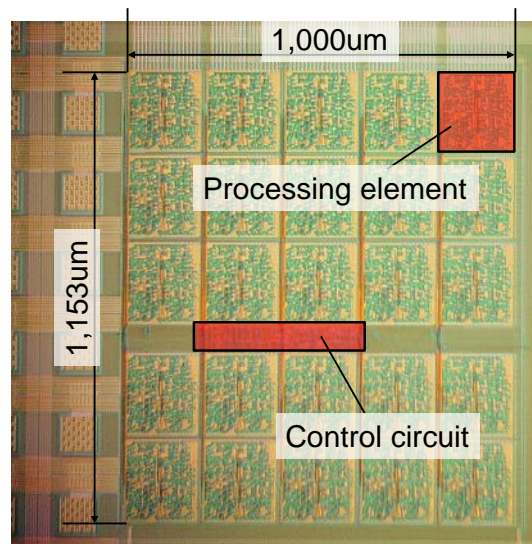


Figure 2: Motion-vector extraction test chip using MTJ-oriented circuit-design automation tools.

Recent Development of Artificial Cognitive Memory

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Artificial cognitive memory (ACM) is the key component for development of bio-inspired computer. Unlike the current solid state memories, ACM not only store the information, but also process information. In this talk, the recent development of ACM will be presented. The main challenges and the possible solutions for the development of ACM will be discussed.

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Magnetic ratchet for 3-dimensional memory and logic

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One of the major challenges for future electronic memory and logic devices is finding viable ways of moving from today's 2-dimensional structures which hold data in an XY mesh of cells to 3-dimensional structures in which data are stored in an XYZ lattice of cells. This could allow a many-fold increase in performance. A suggested solution is the shift register - a digital building block that passes data from cell to cell along a chain. We have discovered a way of implementing a 3-dimensional spintronic unidirectional vertical shift register between sub-nanometer thickness perpendicularly magnetized CoFeB layers similar to those used in MRAM [1]. By carefully controlling the thickness of each magnetic layer and the RKKY exchange coupling between layers we form a ratchet which allows information in the form of a sharp magnetic kink soliton to be pumped unidirectionally from one magnetic layer to another.

In this talk I show experimental results from a 44-layer sample in which digital bits are injected into the bottom layer and then progressively shifted from layer to layer before emerging from the top. I show how several bits can synchronously propagate through the same multilayer, how we can controllably annihilate consecutive data bits and finally how we can use data bits to probe the magnetic properties of individual buried magnetic layers. This simple and efficient shift-register demonstrates a route for spintronics to be used to create 3-dimensional microchips for memory and logic applications.

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Non-volatile Spin Logic

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Reduction of power leakage and interconnect delay are two major problems of VLSI circuits beyond 65 nm. Memory-in-logic architecture employing conventional CMOS logic with embedded non-volatile memory elements is expected to provide both almost zero power consumption in standby mode and short interconnect delay. In order to fully take advantages of the memory-in-logic architecture, it is important to use non-volatile memory elements that have fast switching, low write current density, unlimited endurance, excellent scalability and compatibility with CMOS logic [1-3].

Fig. 1 shows a circuit diagram of a non-volatile CMOS inverter [4] with embedded magnetic tunnel junction (MTJ). It employs the MTJ with perpendicular anisotropy to insure the excellent scalability, high speed (switching time $\tau_s < 10$ ns) and low switching current density ($J_s \leq 1 \cdot 10^6$ A/cm²). The low switching current density provides a possibility to use one switching transistor for controlling a logic state of the MTJ. Moreover, both elements can be built with similar technology node. To memorize the logic state of the CMOS inverter the bidirectional switching current in the MTJ must be provided. It is achieved by using a memory voltage source V_M that satisfies to the following condition: $V_{DD} > V_M > GRD$. Ideally, the potential of the memory voltage source can be $V_M = V_{DD}/2$.

The proposed solution can be extrapolated to a majority of fundamental logic circuits such as latches, adders, multiplexers and others for providing them with a non-volatility [5-7]. The non-volatile spin logic circuits can dramatically change a design of field programmable gate arrays (FPGA). Fig. 2 illustrates a comparison of the CMOS FPGA with a spin FPGA having similar logic density and built with similar technology node. It suggests that the spin FPGA can provide almost zero power consumption in the standby mode of operation, substantial reduction of cost and die size without speed degradation. Furthermore, the spin FPGA has an excellent reconfiguration capability at runtime operation.

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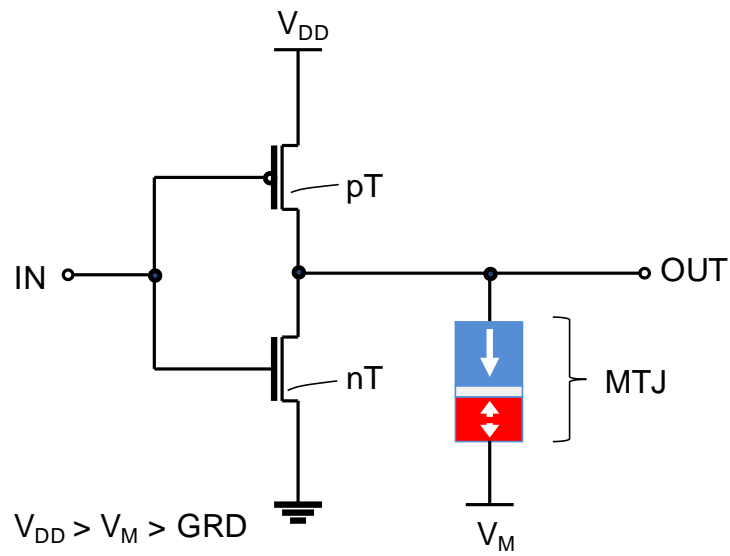


Fig.1. Schematic circuit diagram of a non-volatile spin inverter.

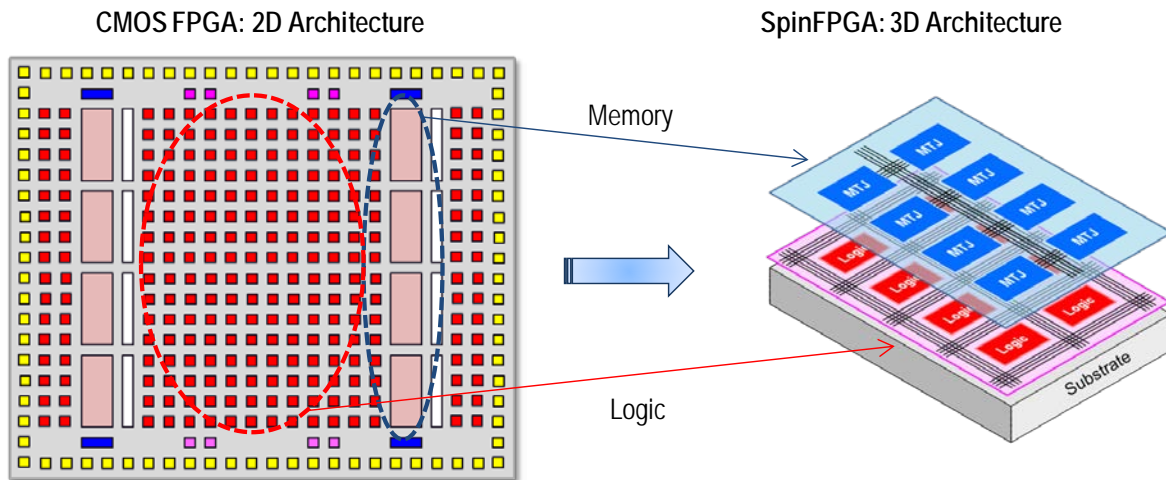


Fig.2. Comparison of a conventional CMOS FPGA with spin FPGA having a similar logic density.

Emerging Nonvolatile Memories from an Enterprise System

Company Perspective

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MRAM and PCM in close to their modern forms have been under rather serious investigation for almost two decades now. Each has been introduced into the market. MRAM's features of being relatively fast and nonvolatile with unlimited endurance have made it particularly suitable for log file applications, which do not stress density. PCM as a relatively fast and high endurance nonvolatile memory with good scaling properties has penetrated the mobile phone market, supplanting in some cases NOR Flash, which is encountering severe scaling challenges. This talk will review the attractive attributes of MRAM and PCM and discuss how these technologies need to evolve to become more pervasive and how these emerging memories might address needs for enterprise computing.

MRAM in particular will be discussed in some detail, including recent results for spin-transfer-torque MRAM with perpendicular magnetic anisotropy materials. A particular interest for high-performance computing would be if MRAM could perform well enough for cache memory applications, positioning it near the fast end of a hierarchy of memory types with different access times and densities. A challenge for the magnetic tunnel junction device in this regime is efficient writing, i.e., maintaining high thermal stability while requiring only modest write currents. In this regard, recent results encouragingly indicate that devices with 20nm diameter or less can perform at and even beyond what might have been expected to be ideal expectations from a single-domain model. These and other results will be discussed in the context of memory hierarchy needs for enterprise computing.

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Voltage Controlled Spintronics for Nonvolatile Nanoelectronics – A new paradigm

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As CMOS approaches its scaling limits, new paradigms may emerge. One critical issue is the energy dissipation both in switching and standby, the latter of which arrives from lack of remembering the state when powered off. We will give a brief overview of the current challenges of CMOS in terms of energy dissipation and variability. Then I will describe the advantage of collective spin memory devices in terms of nonvolatility, low switching energy, high speed, high endurance, and scalability. These advantages offer a potential of incorporating nonvolatile spin transfer torque (STT-RAM)¹ with CMOS for embedded application, e.g., replacing volatile CMOS Static RAM (SRAM), followed by discussion of integration of CMOS reconfigurable circuits² with STT-RAM. We will then present the recent advances and scaling limits of the STT memory as well as new development using the spin Hall Effect to reduce the write current.

To further reduce the switching energy, I will describe a new concept of electric-field control of magnetism, or voltage-controlled magnetoelectric (ME) memory (Me-RAM)³. Only recently, it is shown to be possible to use electric field to control metallic magnetism. For the latter, we will describe a couple of fundamental mechanisms of voltage control of magnetic moment and direction. With further advances in this area, we anticipate that the energy reduction of several orders of magnitudes beyond that of STT. The integration of magnetic devices will reduce the standby leakage of CMOS circuits and thus enable further scaling of CMOS with improved performance. These types of device may be integrated directly on top of front-end processed CMOS using back-end process. They will enable standalone and imbedded applications, making possible new generations of nonvolatile instant-on electronics and other systems.⁴ A potential new paradigm of instant-on, nonvolatile electronic circuits and nano-systems may emerge.

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Voltage induced unipolar switching in magnetic tunnel junctions with tunable energy barrier

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It is interesting to study the effect of voltage induced switching in magnetic nanostructures, partly driven by the premise that, if feasible, voltage-controlled magnetization reversal would be far more energy efficient and be compatible with the ubiquitous semiconductor devices. However, such effects in metals are expected to be negligible since the electric field due to the applied voltage would be screened in the interior except within a few monolayers at the metal surface. On the other hand, a voltage may exert marked effects in ultrathin thin films with magnetic properties dominated by interfacial magnetic anisotropy. Here we show, using magnetic tunnel junctions (MTJs), the pronounced effects of voltage controlled magnetic anisotropy in very thin CoFeB layers, where the magnetic anisotropy originates solely from the CoFeB/MgO interfaces. We demonstrate that electric field, both its magnitude and direction, under low voltages ($\leq \pm 1.5$ V), can systematically alter the perpendicular magnetic anisotropy of the thin CoFeB layers interfaced with the MgO barrier. More importantly, voltage induced unipolar switching, as opposed to conventional current induced bipolar switching due to the spin-transfer torque effect, has been realized in such MTJs. Most notably, we have observed voltage-induced switching at a very low current density of 2×10^4 A/cm², far lower than those for current switching.

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Voltage-controlled Exchange Bias for ultra-low power MRAM Applications

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Voltage-controlled spintronics is of particular importance to continue progress in information technology through reduced power consumption, enhanced processing speed, integration density, and functionality in comparison with present day CMOS electronics. Controlling interface magnetism by purely electrical means is a key challenge to better spintronics. I report on the antiferromagnetic (AF) magnetoelectric (ME) Cr₂O₃ (chromia) for voltage-controlled interface magnetism enabling dissipationless writing of non-volatile information in magnetic random access memories. The novel spintronic device exploits voltage-controlled boundary magnetization (BM), a magnetic moment that emerges as a robust equilibrium property at the surface or interface of a ME antiferromagnet. Switching of BM enables switching of the ferromagnetic free layer of a magnetic tunnel junction (MTJ) through a voltage-pulse. It sets the state of the memory element defined by high and low resistance levels of the MTJ (Fig. 1). Robust isothermal electric control of exchange bias (EB) achieved near room temperature in the EB heterostructure Cr₂O₃(0001)/CoPd is the key physical building block of such an ultra-low power MRAM [1]. Voltage-controlled EB provides macroscopic evidence for electrically switchable BM. First-principles and symmetry considerations show that BM is a generic property of ME antiferromagnets. Spin-resolved UPS of a chromia (0001) surface provides averaged information of the BM. Laterally resolved X-ray PEEM (Fig.2) and *T*-dependent MFM reveal microscopic details [2]. Our data on electrically controlled EB lay the foundation for a new route towards voltage-controlled spintronics such as ultra-low power MRAMs.

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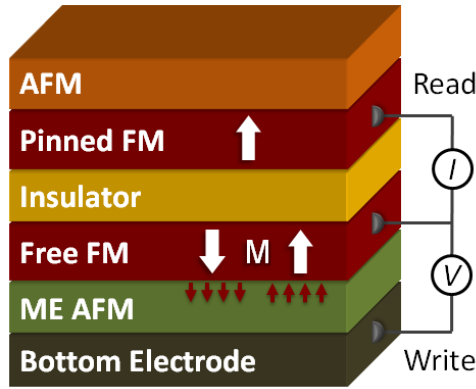


Fig.1: Magnetoelectric-MTJ. Free layer magnetization is switched by voltage-controlled boundary magnetization of a magnetoelectric antiferromagnet which controls the MTJ resistance.

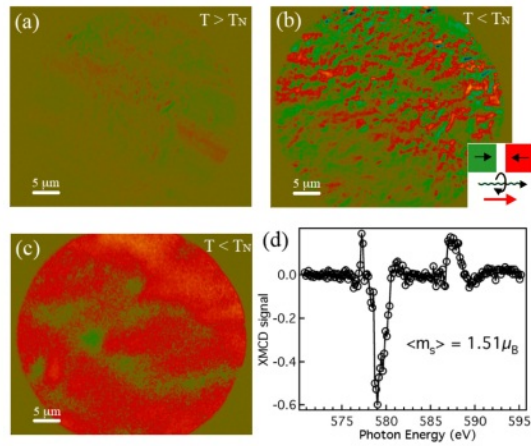


Fig.2: (a-c) Cr_2O_3 (0001) film imaged by XMCD-PEEM at the Cr L-edge. (a) No contrast at 584 K. (b) Multi-domain state after zero-field cooling. Inset shows spin polarization with respect to positively circularly polarized incident light. (c) Nearly single-domain state at 223 K after ME field-cooling. (d) XMCD spectrum recorded from within one domain.

Reconfigurable Spin Switch for Digital/Analog Computing

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STT-MRAM memory (in-plane and PMA) is being widely developed and commercialized enabled in large part by the experimental advances in the fields of spintronics and magnetics that have made it possible both to read information from (via magneto resistance) and to write information on magnets (via spin transfer torque). It is natural to ask whether these advances can enable novel spin-logic devices as well. *Logic devices* however, require fundamental properties such as input-output isolation, gain and fan-out in order to be interconnected into functional circuits without the aid of intervening CMOS switches. Recently, we have shown that [1] the established physics of spin valve devices together with the discovered giant spin-Hall effect [2] could be used to construct a non-volatile reconfigurable spin switch (RSS) [Fig.1] having the transistor-like properties [3] mentioned above. *Both Boolean and non-Boolean* logic could be implemented using the proposed RSS device but based on the state of the art physical mechanisms for reading and writing information, we do not anticipate any significant advantage over CMOS switches for standard logic devices. However, the non-volatility and reconfigurability associated with magnets could enable a new class of unconventional devices that cannot be implemented with CMOS. *Signal processing* in mobile devices is one such application that might be able to take advantage of RSS. Figure 2b shows a diagram of finite impulse response filter (FIR) heavily used in signal processing [4]. (In particular an implantation using RSS devices is shown). Direct sequence spread spectrum in mobile devices uses a similar structure except that instead of using the impulse response, it uses stored reference codes to de-code an incoming signal which contains the information of multiple users. Figure 2a shows an example where an input data stream (top left) carries coded data bits 1 and 0 for two different users. Each user extracts its own data (Fig.2c) with a unique 64 bit Walsh code using the correlator (Fig.2b). The RSS can take in both digital as well as analog inputs. The unique hybrid digital/analog nature of RSS could reduce or eliminate the usage of A/D or D/A convertors routinely used in wireless technology. Moreover, RSS could find use in mixed signal applications as well.

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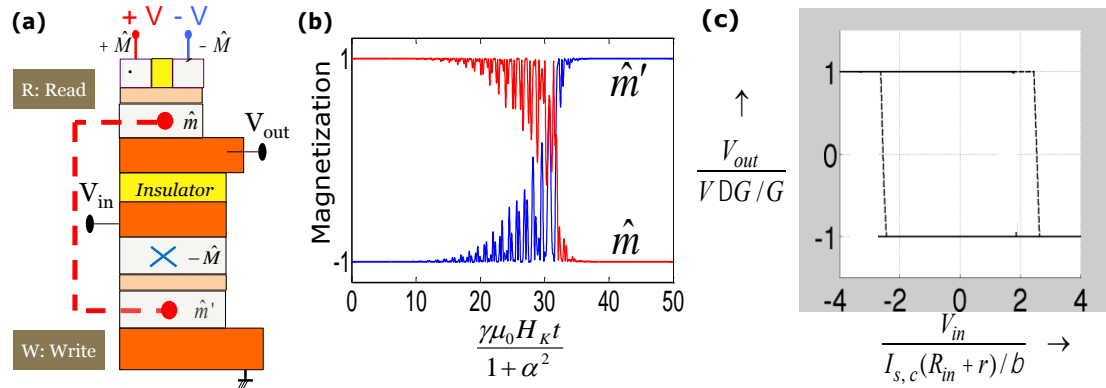


Figure 1. (a) Reconfigurable spin switch (RSS). (b) An example of a switching event where the read unit magnet, m , follows the write unit magnet, m' . (The two magnets are coupled by the stray fields.). (c) Inverter-like input-output characteristics of RSS.

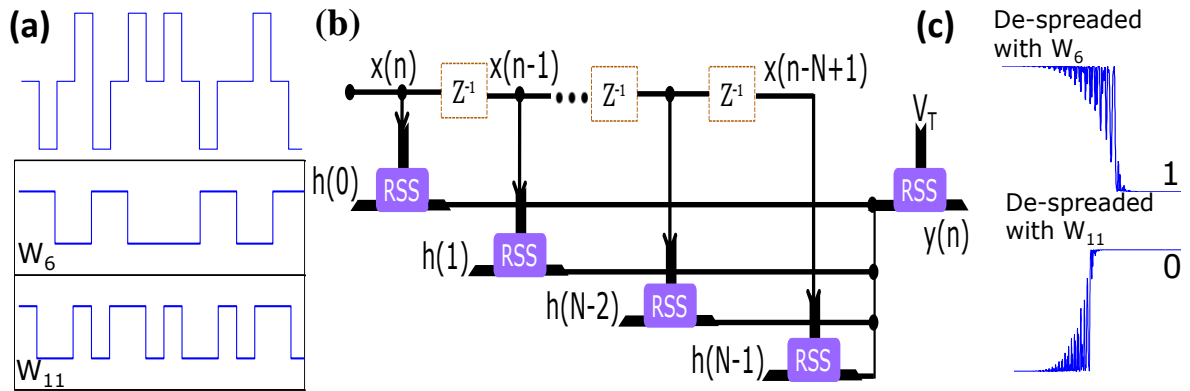


Figure 2. De-coding example in direct sequence spread spectrum using RSS. (a) Top left: coded signal contains both bits 1 and 0. Bottom: As an example, two Walsh codes are shown. (b) An implementation of FIR filter using RSS devices. (c) The decoded data bits from incoming signal (top left in 'a') are shown. The incoming signal goes through the FIR filter, 'b', which uses Walsh codes W_6 and W_{11} to compute the correlation with the input data stream 'x'.

Spintronics Based NV-Memory/Logic for Low Power Systems

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Recently in semiconductor memories, it is becoming difficult to meet the target performance requirements by technology development based solely on device scaling. Firstly, the speed gap between each memory levels in addition to the speed gap between the operation speed of logic and that of memory have expanded year by year. Moreover, the power consumption due to the increase in memory capacity and increased operation speed is rapidly increasing.

In this paper, the directionality of the revolution of the semiconductor memory hierarchy structure in the future from the background mentioned above is discussed. The realization of this revolution in the memory layers with STT-MRAM memories, which solve both the issues of speed gap and power consumption simultaneously, is introduced. In addition, from the viewpoint of the super-low power consumption system for the future, the impact of spin devices as the next generation nonvolatile memory and as the element for future generation high-level nonvolatile logic, which combines both the STT-MRAM with semiconductor CMOS logic, is discussed.

Acknowledgements

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Neuromorphic Computing with Memristive Circuits

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In this talk we will discuss recent experimental results on pattern classification and recognition tasks implemented with memristive [1] (ReRAM [2]) neural networks. The Pt/TiO_{2-x}/Pt memristive devices (Fig. 1a, b), which are utilized in both demonstrations, are fabricated with nanoscale e-beam-defined protrusion which localizes the active area during the forming process to $\sim(20\text{ nm})^3$ volume and as a result helps in improving device yield.

In particular, we will first discuss demonstration of pattern classification task for 3×3 binary images by a single-layer perceptron network implemented with 10 x 2 memristive crossbar circuits (Fig. 1c) in which synaptic weights are realized with memristive devices. The perceptron circuit is trained by ex-situ and in-situ methods to perform binary classification for a set of patterns from an original work by Widrow [3]. In the ex-situ case, the synaptic weights are calculated on the precursor software-based network and then imported sequentially to the crossbar circuits using variation-tolerant programming algorithm [4]. For the in-situ training, the weights are adjusted in parallel following perceptron learning rule by applying voltage pulses from pre-synaptic and post-synaptic neurons. Both approaches work successfully (Fig. 1d) despite significant variations in switching behavior of memristive devices as well as half-select and leakage problems in crossbar circuits [5].

We then present experimental demonstration of pattern recognition task, in particularly showing 4-bit analog-to-digital conversion (ADC) operation implemented with Hopfield recurrent neural network [6] (Fig. 2a). A 4-bit ADC is implemented with four inverting amplifiers (neurons), each of which is made with three Si IC operation amplifiers, and a 4×6 memristor crossbar which defines the connectivity among neurons (and bias). Just like for the previous task, the memristors are tuned precisely to the values described in the original work [6] using the developed algorithm [4]. Fig. 2b shows the measured binary output code for a quasi-DC sweep of input.

Although the considered circuits are simple and hardly practical by itself, the established work presents a proof-of-concept demonstration for highly anticipated efficient memristor-based artificial neural networks and paves the way for extremely dense, high-performance information processing systems.

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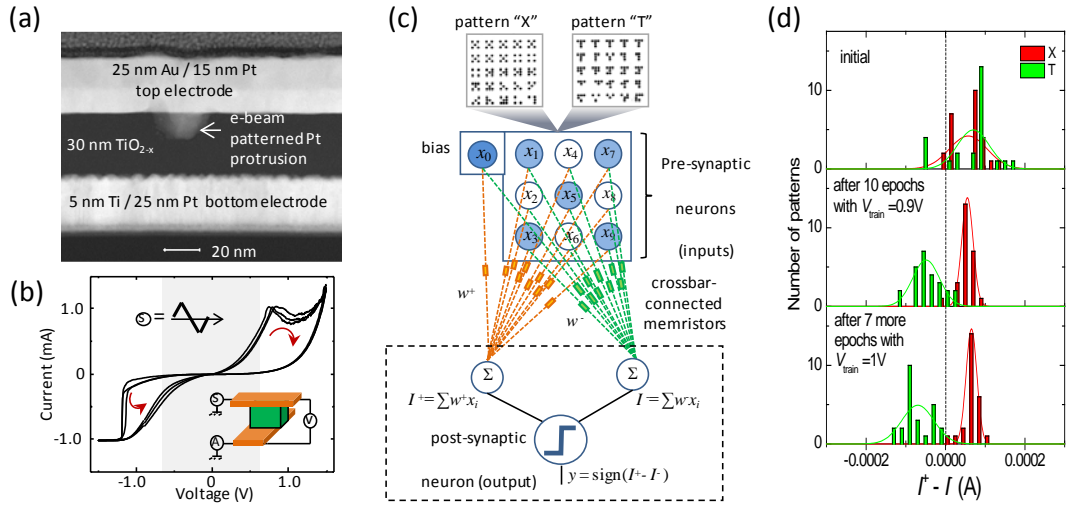


Figure 1: Pattern classification with memristive crossbar circuit: (a) A zoom-in on the active part of a TiO_{2-x} device, (b) I-V showing multiple set and reset switching cycles, (c) general scheme for pattern classification experiment showing two sets of patterns used for training and testing, and (d) the experimental results for ex situ training.

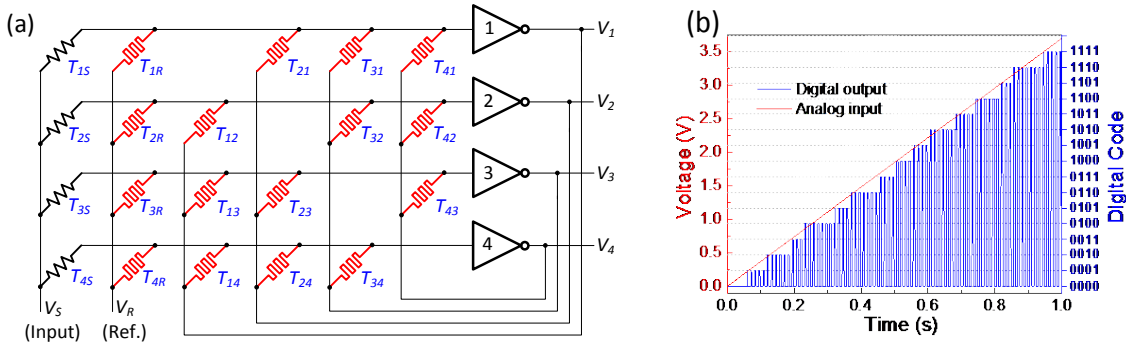


Figure 2: Pattern recognition with memristive crossbar circuit: (a) Schematics of Hopfield neural network-based ADC, and (b) measured digital output voltage of the ADC circuit as a result of an application of analog input voltage ramp (shown with red) which is varied from 0 to its maximum value. The outputs of the neurons are periodically reset with a frequency of 80Hz.

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Embedded STT-MRAM: Tailoring Attributes for Mobile Systems

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Advanced mobile computing and connectivity systems are sophisticated or complex in their architectures for which energy efficiency has become a critical figure of merit. STT-MRAM offers intrinsically compelling attributes which can realize disruptive memory solutions for advanced mobile SOC. Embedded STT-MRAM can be designed and integrated in a fully logic-compatible way both in process and in supply voltage, so that it can be offered in custom macros whose attributes are tailored for relevant applications. For the near term, STT-MRAM is preferred as an embedded nonvolatile memory (NVM) to serve battery-powered mobile connectivity and security systems. This type of STT-MRAM can provide a memory subsystem not only by storing codes, but also by fast storing and executing data. This simplifies the conventional memory subsystem and also extends battery life. Further, its logic-friendly design and process compatibility can realize such benefits at advanced CMOS nodes for which there is no conventional NVM alternative. A potentially more compelling application is sought with high-performance STT-MRAM which can serve as an alternative to 6T-SRAM or embedded DRAM in emerging CMOS nodes. An example is Level-3 cache for mobile processors. In addition, there is a significant range of SRAM for which its leakage power and cost (chip area) are critical drawbacks. Despite the fact that STT-MRAM is slower than SRAM as a device, the memory subsystem can be architected in a way that the performance can be comparable or possibly better at a system level.

Orthogonal Spin-Transfer Torque Magnetic Random Access Memory

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Orthogonal spin-transfer magnetic random access memory (OST-MRAMTM) uses a spin-polarizing layer magnetized perpendicularly to a free layer to achieve large spin-transfer torques, ultra-fast and energy efficient switching [1]. We have fabricated and studied OST-MRAM devices that incorporate a perpendicularly magnetized spin-polarizing layer and a magnetic tunnel junction, which consists of an in-plane magnetized free layer and synthetic antiferromagnetic reference layer [2]. Reliable switching is observed at room temperature with 0.7 V amplitude pulses of 500 ps duration. The switching is bipolar, occurring for positive and negative polarity pulses, consistent with a precessional reversal mechanism, and requires an energy of less than 450 fJ. Our recent single shot time sub-nanosecond time resolved measurements show that the switching can occur by direct (e.g., AP->P) or precessional reversal (e.g. AP->P->AP-->P) depending on the bias and pulse conditions, enabling different modes of device operation. These OST-MRAM device characteristics will be presented and compared to those of other STT-MRAM approaches.

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Mn-based Magnetic Alloys and Magnetic Tunnel Junctions for STT-MRAM applications

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Spin-transfer-torque magnetoresistive random access memory (STT-MRAM) is one of the candidates for a high capacity and fast nonvolatile memory. Several groups demonstrated that a magnetic tunnel junction (MTJ) with perpendicularly magnetized electrodes is advantageous to scaling for giga bit class STT-MRAM because a high perpendicular magnetic anisotropy (PMA) increases a thermal stability of magnetization directions even though a size of device decreases down to several nm [1,2]. In order to develop STT-MRAM with capacity beyond Gbit, free layer electrode magnetic materials should have a large PMA K_u^{eff} which is larger than 10 Merg/cm³ as well as a small damping constant α less than 0.01, for sufficient data retention and critical current density J_C small enough to integrate with MOS-FET. Exploration of such key materials is one of the challenging issues for realization of STT-MRAM. Moreover, it is crucial that MTJs with such materials exhibit tunnel magnetoresistance ratio (TMR) more than 150% at room temperature.

An interesting candidate of such materials is a Mn-Ga alloy, that is one of hard magnets such as Mn-Al but those have not been known well. Recent theory predicted that Mn₃Ga with $D0_{22}$ ordered structure, which is a tetragonally distorted $D0_3$ structure; exhibits spin polarization of 88% [3]. We demonstrated the compatibility of large $K_u > 10$ Merg/cc and small $\alpha < 0.008$ for the alloy films [4-6], and also predicted large TMR $> 600\%$ from first principles calculation [7]. Experimental TMR ratio is very sensitive to the interface properties of Mn-Ga/MgO, that demonstrated by our recent studies on TMR in Mn-Ga/MgO MTJs with thin Fe or Co layer insertion [8]. In this talk, we will discuss details of TMR for Mn-Ga MTJ as well as exploration into other Mn-based alloy for MRAM application [9].

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NVE technology summary: MRAM and beyond

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Since our incorporation in 1989, NVE set out to provide innovative solutions to unique problems in memory and sensors by leveraging giant and tunneling magnetoresistance technologies. The first portion of this talk will cover our commercially successful products that stem from earlier work in developing our technology primarily through the United States government's small business innovation research (SBIR) program. These include our magnetic sensor and galvanic isolator products. Also, while we don't offer a commercial MRAM product recent efforts have been made in providing custom solutions. The latter portion of the talk will be dedicated to some of the current challenges and efforts we are putting forward to further grow our core business. These include development of magnetic biosensors as well as new core technology utilizing magnetic films with perpendicular magnetic anisotropy to be sensitive to magnetic fields perpendicular to the sensor die and enhance the range of detection while preserving device sensitivity.

Study on electrical and magnetic performances of thin film $\text{Cr}_2\text{O}_3/\text{Fe}_2\text{O}_3$ sesquioxide with ME effect

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Magnetoelectric (ME) effect has been paid much attention to be applied to a nonvolatile memory (NVM). Cr_2O_3 is a typical sesquioxide that has ME effect and its antiferromagnetic Neel temperature is $T_N = 307$ K, which is higher than RT. A robust isothermal electric control of exchange-bias at RT is actually reported for bulk Cr_2O_3 when both electric field $E = 0.02$ [MV/cm] and magnetic field $H = -1.54$ [kOe] was applied [1]. But ME effect has not yet been clarified in Cr_2O_3 thin films because of its large leakage current while ME effect like behavior up to 200K is reported to be observed in an ultrathin $\text{Cr}_2\text{O}_3/\text{Fe}_2\text{O}_3$ Nano-Oxide Layer (NOL) [2]. When considering the application of ME effect to NVM technology for voltage-controlling magnetization switching, there are some problems except the above issue, which should be resolved. The first is to realize and design an effectually high exchange-bias filed between Cr_2O_3 and FM thin film layers in the higher temperature range than RT, means high blocking temperature (T_B), where the properly low coercive force of FM is also required. The second is to invest FM layer with a perpendicular anisotropy which is thought to be caused by both of the hybridization of FM 3d and O 2p orbitals and the magnetic coupling at the interface between FM and Cr_2O_3 . The third is to confirm ME effect in the thin film Cr_2O_3 after getting Cr_2O_3 thin film which shows good electrical properties. In this study, electrical and magnetic performances of the thin film $\text{Cr}_2\text{O}_3/\text{Fe}_2\text{O}_3$ sesquioxide were investigated. We successfully fabricated the Cr_2O_3 thin film with small leakage current. The electrical properties were measured in the perpendicular direction to the film. Figure 1 shows the leakage current properties of the sample. The leakage current density at $E = 0.02$ [MV/cm] is as small as 3×10^{-6} [A/cm²]. From the impedance measurement, the parasitic resistance, the film resistance and the capacitance were 16.6 [Ω], 80.2 [k Ω] and 17.2 [nF], respectively. Dielectric constant ϵ_r calculated from these results was 13.8, which is almost same as that reported ($\epsilon_r = 11.9$). In addition, we also successfully observed the effect of Fe_2O_3 buffer layer on H_{ex} and T_B . Figure 2 displays the temperature dependence of the exchange anisotropy energy (J_K). Cr_2O_3 with thin Fe_2O_3 buffer (5 nm) shows high J_K up to 0.44 (erg/cm²) and higher T_B more than 200K. In presentation, the control of both of Neel temperature for Cr_2O_3 and Morin temperature for Fe_2O_3 is also discussed from a perspective of future NVMT.

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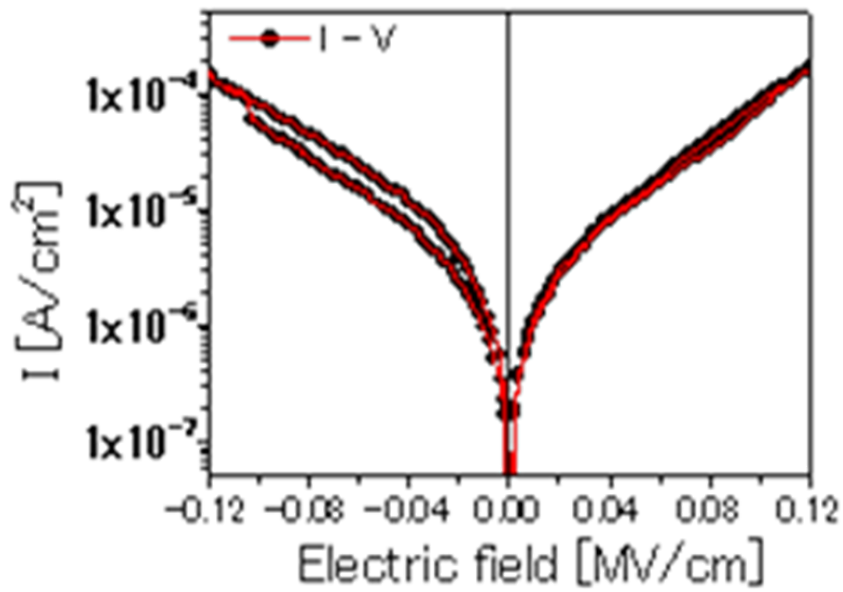


Fig. 1 I-V properties of the sample. Electric field was applied from -0.12 [MV/cm] to 0.12 [MV/cm].

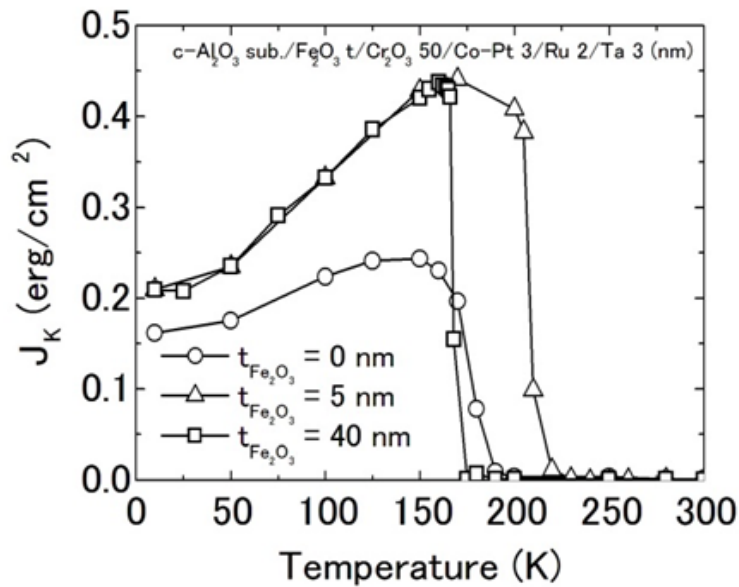


Fig.2 Temperature dependence of exchange anisotropy energy of Cr_2O_3 film by varying Fe_2O_3 buffer layer thickness.

Processing of Magnetic Tunnel Junction Stacks for STT

MRAM Applications

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The material systems for in-plane magnetic tunnel junctions (iMTJ) used in STT MRAM have evolved from MTJ readers used in HDD over last 7 years, and hence are relatively well characterized. Here we will report spin torque switching for such a simple MgO based iMTJ with CoFe₂₀B₂₀ storage layer thickness of 11, 14 and 18 Å deposited by sputtering. TMR as measured by CIPT, was 100%, 155% and 200% respectively, and the RA product 13-15 Ohm μm². The minimum critical current for switching was reduced from 6 MA/cm² (0.8V) for 18Å to 3 MA/cm² (0.5V) for 11 Å. The reason for this reduction is the lower effective field (H_{eff}) of the thinner samples, due to the perpendicular anisotropy appearing at the CoFeB/MgO interface [1, 2]. For further scalability of STT-MRAM to smaller bit sizes of < 40nm, complete perpendicular anisotropy of magnetic tunnel junction (pMTJ) is preferred over iMTJ. There is no consensus yet on which material system for pMTJ will be able to meet the requirements for low critical current, high thermal stability and ease of integration. Deposition parameters such as low deposition pressure, angled deposition and low base vacuum are important to get high anisotropy and TMR. In addition, post deposition thermal processing budget is critical for these material systems to maximize TMR and perpendicular anisotropy in these systems. We studied both top and bottom pinned pMTJ, with Co/Pt multilayer based synthetic anti-ferromagnet (SAF) and thin CoFeB free layer, which is a basic configuration that can be used to gauge process capability. The stacks were deposited in the newly developed multi-cathode sputter deposition chambers and were subsequently annealed for times ranging from few milli-seconds to few minutes at temperatures between 1000°C to 260°C. This anneal was used for MgO crystallization as well as to maximize perpendicular anisotropy resulting from MgO / CoFeB interface [3]. For reference, standard anneals of 300°C/1 hour gives a baseline of >100% TMR for RA ~ 10 Ω-μm² for both top and bottom pinned structures. The interface anisotropy (K_s) was calculated at ~1-2 ergs/cm for these systems.

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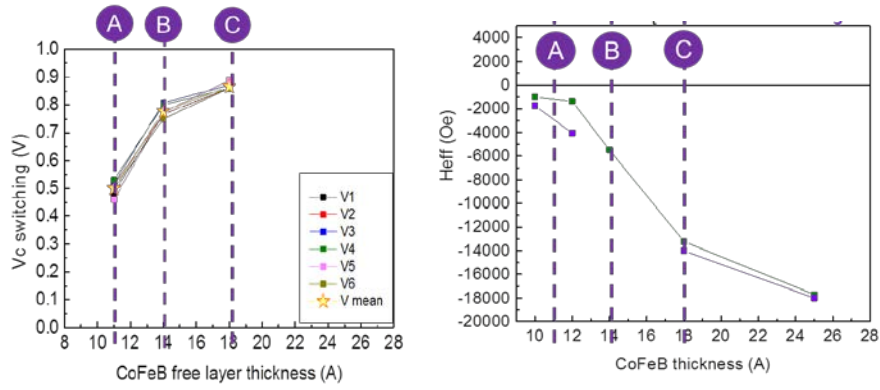


Fig. 1: switching characteristics of iMTJ: (a) V_c and (b) H_{eff} as function of CoFeB thickness.

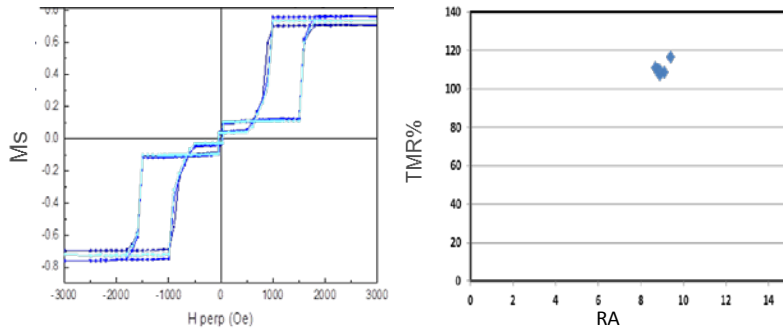


Fig. 2: Bottom pinned pMTJ characteristics for 300mm wafer: (a) M-H curve, (b) RA-TMR

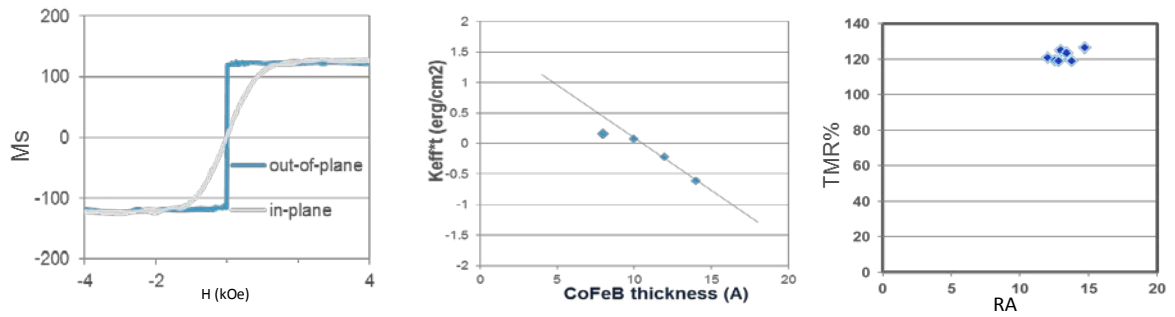


Fig. 3: Top pinned MTJ characteristics for 300mm wafer: (a) M-H plot of storage layer, (b) K_{eff} as function of thickness and (c) RA –TMR at 10Å