1. An instruction set consists of three types of instructions, I1, I2, and I3, and runs on microprocessor M with a clock rate of 1GHz.

   The table below shows (a) the number of cycles, C, required to execute each instruction type, and (b) the number of instructions of each type within two programs P1 and P2 based on this instruction set.

	I1	I2	I3
C	2	1	3
N (P1)	2000	3000	4000
N (P2)	4000	2000	4000

   (a) What is the average number of cycles per instruction (CPI) for each program?
   (b) Which program completes execution earlier?
   (c) In general – i.e., not just for the cases described in this problem – when you compare two programs, is it always true that the program with the better CPI has the faster execution time? Explain.
   (d) Let us say that we have the freedom to change the clock period of microprocessor M without affecting any entries in the table above. Let the execution time of P1, executed at a clock frequency of 1GHz, be T units. At what clock speed should P2 be executed to ensure that it is also completed in exactly T units?

   [5 points for each part]

2. A processor has a standard five-stage execution pipeline, with the following stages:

Instruction fetch (IF)	fetches the instruction from an instruction memory
Instruction decode (ID)	fetches the operands of the instruction from the register file and decodes the instruction
Execute (EX)	executes ALU instructions
Memory (MEM)	performs read/write operations on the data memory
Writeback (WB)	writes data back to the register file

   Assume that each pipeline stage requires a single clock cycle. Consider the execution of the following program on this pipelined processor:

```
I1:  R1 <- R2 + R3
I2:  R4 <- Mem(R1)
I3:  R2 <- Mem(R2)
I4:  R4 <- R4 + R5
I5:  R6 <- Mem(R3)
I6:  R1 <- R6 + R7
```

   Here, `Rn` corresponds to register `n`, and `Mem(Rn)` corresponds to the contents of the memory location whose address is given by the contents of register `Rn`. For convenience, the instructions are numbered from I1 to I6.

   (a) Identify all data or control hazards in the program.
   (b) Assume that no pipeline forwarding is used, and that you are not allowed to reorder instructions. How many nops/pipeline stalls must be introduced to maintain program correctness?
   (c) Repeat (b) for the case where pipeline forwarding is used, but instructions may not be reordered.
   (d) Repeat (b) for the case where pipeline forwarding is used *and* instructions may be reordered.

   [5 points for each part]