A modern NMOS transistor has the following room temperature characteristics:

Channel/gate length (L)	45 nm
Channel width (W)	450 nm
Effective gate oxide thickness (t_{ox})	1.5 nm
Channel doping (N_A)	$5*10^{17}$ cm^{-3}
Effective room temperature mobility (μ_{eff})	150 cm^2/V-sec
Gate workfunction (ϕ_m)	4.2 eV

At room temperature silicon has the following properties: the bandgap is 1.12 eV, the intrinsic carrier concentration is 10^{10} cm^{-3}, and the electron affinity is 4.05 eV. Assume that the mobility is independent of voltage. Also note that $q=1.6*10^{-19}$ coul; $\varepsilon_o=8.84*10^{-14}$ F/cm, kT=0.0257 eV.

a) Ignoring charges in the gate insulator and interface states, calculate the threshold voltage. Next, if the oxide had 10^{11} cm^{-2} of fixed charge (i.e. positive charge at the Si/SiO_2 interface), what would the threshold voltage be? (1.25 points)

b) If the device operates with a supply voltage of 1.2 V, calculate the maximum current that this transistor supplies. You can assume simple long channel behavior without velocity saturation. Assume the first answer in part a with no oxide charge. (1.5 points)

c) Explain qualitatively how the answers to parts a and b would depend on temperature over the range 50 K < T < 400 K (you only need to say increase, decrease, or stay the same – no need to derive equations). Justify your answer by explaining how the parameters that go into the threshold voltage and drain current equations change with temperature and what effect is dominant in different temperature regimes. Draw a rough plot of how the answer for part b would vary with temperature over this range. (1.25 points)