A modern NMOS transistor has the following room temperature characteristics:

Channel/gate length (L)	45 nm
Channel width (W)	450 nm
Effective gate oxide thickness (t_{ox})	1.5 nm
Channel doping (N_A)	$5*10^{17}$ cm^{-3}
Effective room temperature mobility (μ_{eff})	150 cm^2/V-sec
Gate workfunction (ϕ_m)	4.2 eV

At room temperature silicon has the following relevant properties: the bandgap is 1.12 eV, the intrinsic carrier concentration is 10^{10} cm^{-3}, and the electron affinity is 4.05 eV. Assume that the mobility is independent of voltage. Note q=1.6*10^{-19} coul; ε_o=8.84*10^{-14} F/cm, kT=0.0257 eV.

a) Ignoring charges in the gate insulator and interface states as well as leakage currents, calculate the threshold voltage. Also, if the oxide had 10^{11} cm^{-2} of fixed charge (i.e. positive charge at the Si/SiO$_2$ interface), what would the threshold voltage be?

Solution for no charge

$$V_T = \varphi_{MS} + 2\varphi_F + \frac{k_{Si}}{k_{ox}} * t_{ox} \sqrt{\frac{4qN_A}{k_{Si}\varepsilon_o}\varphi_F}$$

$$\varphi_F = 0.0257V * \ln(N_A / n_i) = 0.0257V * \ln(5*10^7) = 0.46V$$

$$\varphi_{MS} = 4.2eV - (4.05eV + 1.12eV / 2 + 0.46eV) = -0.87V$$

$$V_T = -0.87 + 0.92 + \frac{11.8}{3.9} * 1.5*10^{-7} cm \sqrt{\frac{4*1.6*10^{-19} coul * 5*10^{17} cm^{-3}}{11.8*8.84*10^{-14} \frac{F}{cm}} 0.44V} = 0.23V$$

If we had 10^{11} cm^{-2} of fixed charge, the change in threshold would be Q/Cox

$$\Delta V_T = -1.6*10^{-19} coul *10^{11} cm^{-2} * \left[\frac{3.9*8.84*10^{-14} F / cm}{1.5*10^{-7} cm}\right]^{-1} = -7mV$$

V_T is 0.22V. This change is very small due to the small t_{ox} and so the large Cox.

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b) If the device operates with a supply voltage of 1.2 V, calculate the maximum current that this transistor supplies. You can assume simple long channel behavior without velocity saturation. Assume the first answer in part a with no oxide charge.

Solution

The maximum current will occur when $V_{DS} = V_{GS} = 1.2$ V. The device will be in saturation. Then

$$I_{DS} \approx \frac{W}{2L} \mu_{eff} C_{ox} (V_{gs} - V_t)^2$$

$$I_{DS} \approx \frac{1}{2} * 10 * 150 cm^2 / V - \sec \frac{3.9 * 8.84 * 10^{-14} F / cm}{1.5 * 10^{-7} cm} (1.2 - 0.23)^2 = 1.6 mA$$
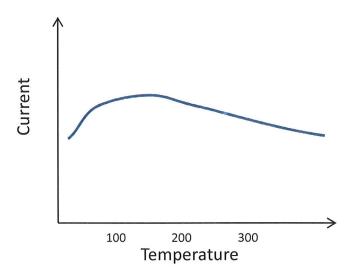
c) Explain qualitatively how the answers to parts a and b would depend on temperature over the range 50 K < T < 400 K (you only need to say increase, decrease, or stay the same – no need to derive equations). Justify your answer by explaining how the parameters that go into the threshold voltage and drain current equations change with temperature and what effect is dominant in different temperature regimes. Draw a rough plot of how the answer for part b would vary with temperature over this range.

Solution

Near room temperature and above, the mobility decreases with increasing temperature due to phonon scattering. The effect is less pronounced in these heavily doped devices than in older, more lightly doped devices. Also, kT and n_i increase with temperature. These effects lead to a decrease in threshold voltage that would lead to an increase in current with increasing temperature, but the mobility is typically the dominant effect.

At sufficiently low temperature, phonon scattering no longer dominates and the mobility becomes much less temperature independent. At that point the current may actually start to fall due to the increasing threshold voltage. At very low temperature (~100 K) carrier freeze-out occurs. Under these conditions the Fermi level goes toward the band edge. In the limit of complete freeze out it must be between the acceptor level and the valence band edge. This increases the threshold voltage since for such thin gate oxides, V_T is dominated by the ϕ_{MS} and $2\phi_f$ terms.

If one only considers drive current, it would be best to be in the range of temperature where phonon scattering is unimportant, this is likely to be in the 100 to 200 K range. Other effects such as subthreshold leakage and junction leakage, as well as the heating caused by device operation would favor a somewhat lower temperature.