The circuit shown below is an actively cascoded operational amplifier. The intent of the differential amplifiers is to boost the output resistance looking into the drain of the various MOSFETs they are paired with. E.g., the amplifier connected between gate and source of MOSFET M_{3A} is a negative feedback element that boosts the resistance looking into the drain of M_{3A} by a factor of A_1+1, where A_1 is the differential gain, and so on. The labels "P" and "N" on the amplifiers simply represent the positive (or non-inverting) input and negative (or inverting) inputs and "O" is the output. The gain of the amplifiers paired with the PMOS transistors (A_1) is different from the gain of the amplifiers paired with the NMOS transistors (A_2) in order to equalize the output resistances. Other than finite gain, the differential amplifiers are otherwise ideal.

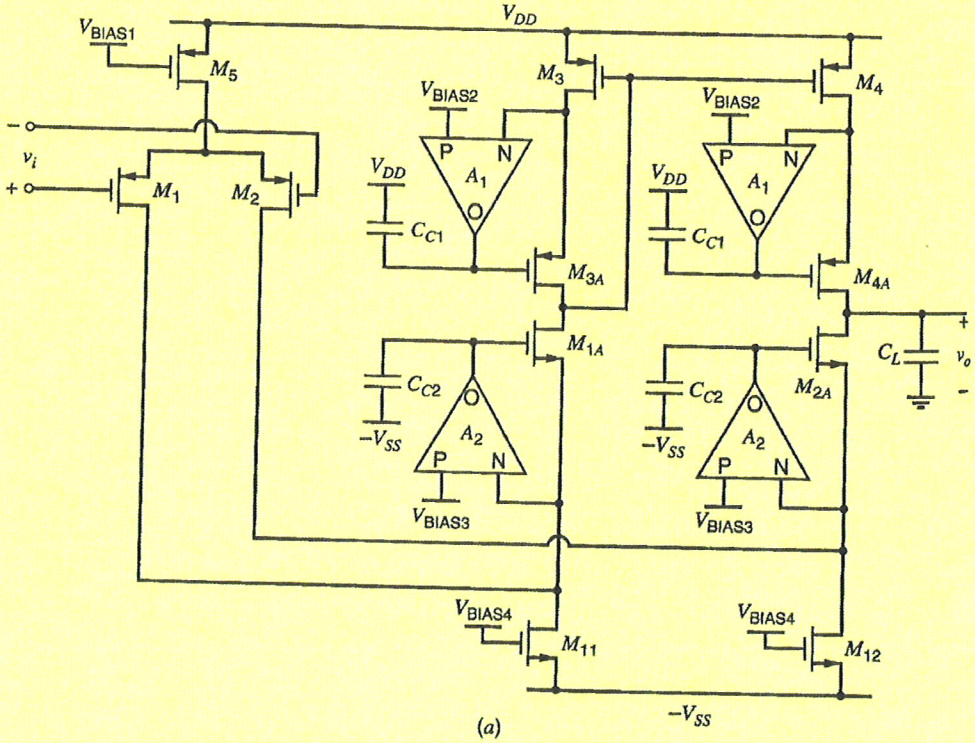
For small signal modeling purposes, use a simple level=1 model consisting of a transconductance and output resistance (ignore the body effect). Drain current and output resistance may be calculated using the following equations:

$$I_D = \frac{KP}{2}\frac{W}{L}(V_{GS} - V_{TO})^2$$

$$r_o = \frac{1}{\lambda I_D}$$

$$g_m = \sqrt{2 I_D KP \frac{W}{L}}$$

Use the parameters listed below for the transistors:
NMOS: VTO=0.7, KP=0.12 mA/V^2, λ=0.1
PMOS: VTO=-0.7, KP=0.03 mA/V^2, λ=0.2



(a)

1) (1 point) The various V_{BIAS} voltages are adjusted to give I_{D5}= I_{D11}=I_{D12}=25μA. What are the various aspect ratios W/L of all the transistors in the circuit to set the over-voltage (V_{GS}-V_{TO}) of each transistor to 100mV?
2) (1 point) Given the above W/L rations, if the differential gain A_1 is 100, what differential gain A_2 is required to match the small signal resistance seen looking into the drain of M_{2A} with the small signal resistance seen looking into M_{4A}?
3) (2points) What is the approximate overall voltage gain v_o/v_i of this amplifier?

HINT: The exact analyses of questions 2 and 3 are quite complicated. One approximation that greatly simplifies the caculation is to short the node connecting the sources of M1 and M2 to ground when determining small signal output resistance