

Problem 1 [1.8 points]

(a) [0.3 points] Derive the minterm canonical form and the maxterm canonical form of the function $f(A,B,C) = A + C$.

(b) [0.3 points] Realize the function $f(A,B,C,D) = A'C' + A'B'D' + ACD + A'BD$ using a single 8-to-1 multiplexer. Use A, C and D as the select inputs where A is the most significant and D is the least significant.

(c) [0.3 points] Repeat part (b), but this time using a single 4-to-1 multiplexer and a minimum number of basic gates (e.g. inverters, ANDs and ORs). Use A and C as the select inputs where A is the most significant bit.

(d) [0.3 points] Find all input tests that can detect whether there is a single stuck-at-1 fault on the output line of boolean function $F=AB+BC$. A stuck-at-1 fault is when a signal line is permanently shorted to 1 due to a defect.

(e) [0.3 points] Algebraically prove that $A'BD' + BCD + ABC' + AB'D = BC'D' + AD + A'BC$. Explain each step of the derivation.

(f) [0.3 points] Using a D-flip-flop and/or basic gates, implement a circuit whose output will toggle whenever the input signal X switches from 0 to 1 (this circuit is a 1-bit counter).

Problem 2 [1.2 points]

Below is a state transition table with the outputs missing. The output should be $Z=X'B'+XB$.

(a) [0.2 points] Complete the state transition table.

(b) [0.4 points] Give the state graph.

(c) [0.6 points] For an input sequence of $X=10101$, draw the timing diagram showing the clock, X, A, B, C, and Z. State changes occur on the rising clock edge. What is the correct output sequence for Z? Change X between rising and falling clock edges so that we can see glitches (also known as timing hazards) on the diagram. Assume that the initial state is $ABC=000$.

ABC (present state)	ABC (next state)		Z	
	X=0	X=1	X=0	X=1
000	011	010		
001	000	100		
010	100	100		
011	010	000		
100	100	001		

Problem 3 [1.0 points]

(a) [0.7 points] Realize the following state table using a minimum number of AND gates, OR gates, and D-flip-flops. Assume both true and complimentary signals are available for inputs X_1 , X_2 , and X_3 .

Present state	$X_1X_2X_3$:	Next state								Z
		000	001	010	011	100	101	110	111	
A		A	A	B	B	B	B	A	A	0
B		A	B	B	A	A	B	B	A	1

(b) [0.3 points] What is the minimum clock period for this circuit? Assume the propagation delay of the flip-flop is 4ns, the setup time for the flip-flop is 2ns, and the delays of the AND and OR gates are 5ns.