Problem 1 [1.8 points]

(a) [0.3 points] Derive the minterm canonical form and the maxterm canonical form of the function f(A,B,C) = A + C.

(b) [0.3 points] Realize the function f(A,B,C,D) = A'C'+A'B'D'+ACD+A'BD using a single 8-to-1 multiplexer. Use A, C and D as the select inputs where A is the most significant and D is the least significant.

(c) [0.3 points] Repeat part (b), but this time using a single 4-to-1 multiplexer and a minimum number of basic gates (e.g. inverters, ANDs and ORs). Use A and C as the select inputs where A is the most significant bit.

(d) [0.3 points] Find all input tests that can detect whether there is a single stuck-at-1 fault on the output line of boolean function F=AB+BC. A stuck-at-1 fault is when a signal line is permanently shorted to 1 due to a defect.

(e) [0.3 points] Algebraically prove that A'BD'+BCD+ABC'+AB'D = BC'D'+AD+A'BC. Explain each step of the derivation.

(f) [0.3 points] Using a D-flip-flop and/or basic gates, implement a circuit whose output will toggle whenever the input signal X switches from 0 to 1 (this circuit is a 1-bit counter).

Solutions

(a) f (A,B,C)= [redacted],3,4,5,67) = A'B'C+A'BC+AB'C'+AB'C'+ABC'+ABD = [redacted],2) = (A+B+C)(A+B'+C)

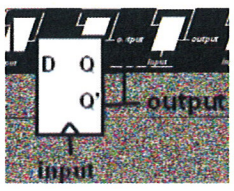
(b) The eight inputs to the mux should be I0=I1=I7=1, I2=B', I3=B, I4=I5=I6=0

(c) The four inputs to the mux should be I0=1, I1=B'D'+BD, I2=0, I3=D

(d) This fault can be detected only when the output F = 0, or AB+BC=B(A+C)=0, leading to ABC= 000, 001, 100, 101, 010 (5 distinct tests)

(e) A'BD'+BCD+ABC'+AB'D
= A'BD'+BCD+ABC'+AB'D+<u>BC'D'+A'BC+ABD</u> (add consensus terms)
= <u>AD</u>+A'BD'+BCD+ABC'+BC'D'+A'BC (AB'D+ABD=AD)
= AD+(<u>BC'D'+A'BC</u>)+BCD+ABC'+BC'D'+A'BC (A'BD' is consensus of BC'D' and A'BC)
= AD+(BC'D'+A'BC)+(<u>AD+A'BC</u>)+BC'D'+A'BC (BCD is consensus of AD and A'BC)
= AD+BC'D'+A'BC (eliminate redundant terms)

(f)



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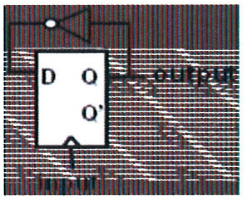


Problem 2 [1.2 points]
Below is a state transition table with the outputs missing. The output should be Z=X'B'+XB.
(a) [0.2 points] Complete the state transition table.

(b) [0.4 points] Give the state graph.

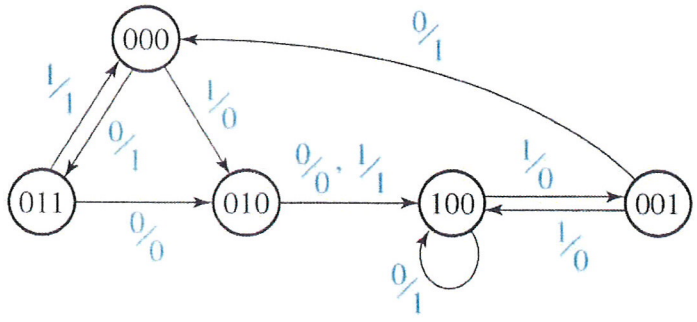
(c) [0.6 points] For an input sequence of X=10101, draw the timing diagram showing the clock, X, A, B, C, and Z. State changes occur on the rising clock edge. What is the correct output sequence for Z? Change X between rising and falling clock edges so that we can see glitches (also known as timing hazards) on the diagram. Assume that the initial state is ABC=000.

ABC (present state)	ABC (next state) X=0	ABC (next state) X=1	Z X=0	Z X=1
000	011	010		
001	000	100		
010	100	100		
011	010	000		
100	100	001		

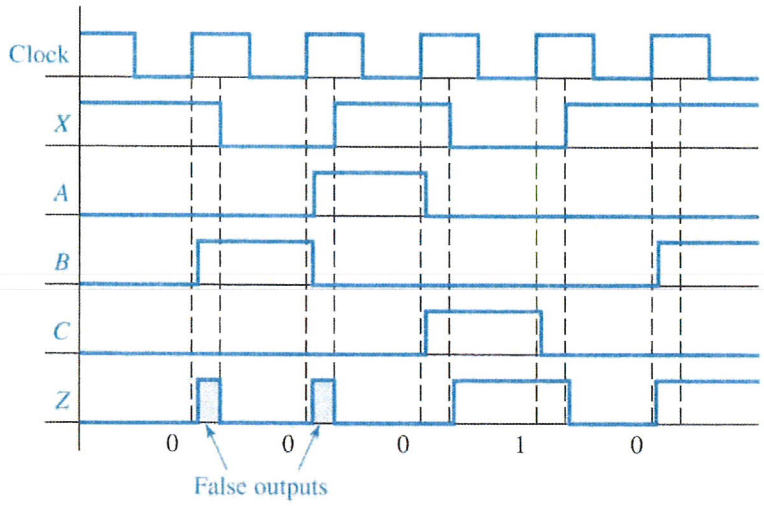
Solutions
(a)

ABC (present state)	ABC (next state) X=0	ABC (next state) X=1	Z X=0	Z X=1
000	011	010	1	0
001	000	100	1	0
010	100	100	0	1
011	010	000	0	1
100	100	001	1	0

(b)



(c)



Correct output sequence: 00010

Problem 3 [1.0 points]

(a) [0.7 points] Realize the following state table using a minimum number of AND gates, OR gates, and D-flip-flops. Assume both true and complimentary signals are available for inputs X_1, X_2, and X_3.

		Next state								
Present state	$X_1X_2X_3$:	000	001	010	011	100	101	110	111	Z
A		A	A	B	B	B	B	A	A	0
B		A	B	B	A	A	B	B	A	1

(b) [0.3 points] What is the minimum clock period for this circuit? Assume the propagation delay of the flip-flop is 4ns, the setup time for the flip-flop is 2ns, and the delays of the AND and OR gates are 5ns.

Solutions

(a) $D=X_1'X_2Q'+X_1X_2'Q'+X_2'X_3Q+X_2X_3'Q$ (three 3-input ANDs, one 4-input OR, and a D-flip-flop)

(b) 4+2+5+5=16 ns