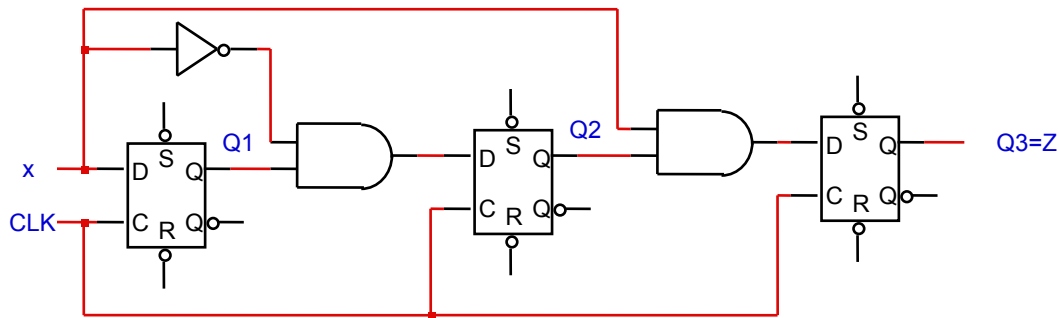


(a) Show how to implement any Boolean function of 10 variables using a ROM module (of size 256 x 8 bits) and a 4-to-1 multiplexer. (i.e., draw a block diagram showing how to connect these modules, and clearly indicate/label inputs and outputs for each module).

(b) Consider the following circuit implementing single input (x), single output (Z) sequence detector. Assuming the initial state is always $Q1\ Q2\ Q3 = 000$, construct a *minimal* state table for a circuit that performs the same function as this circuit. What is the input pattern detected by this circuit?

Note: a minimal state table ~ state table with minimal number of states.



Solution

(a) Denote the function of 10 variables as $F(x_0, x_1, \dots, x_7, x_8, x_9)$. Then ROM can implement any 4 Boolean functions of 8 variables, say x_0, x_1, \dots, x_7 . (these are ROM address lines). The remaining inputs x_8, x_9 serve as select inputs of a 4-to-1 multiplexer. The ROM outputs are forwarded to data inputs of the mux, effectively implementing an expansion of a 10-variable function over variables x_8, x_9 , according to Shannon's theorem. That is, the data inputs to the Mux are:

$$I_0 = F(x_0, \dots, x_7, 0, 0) \quad I_1 = F(x_0, \dots, x_7, 0, 1) \quad I_2 = F(x_0, \dots, x_7, 1, 0) \quad I_3 = F(x_0, \dots, x_7, 1, 1)$$

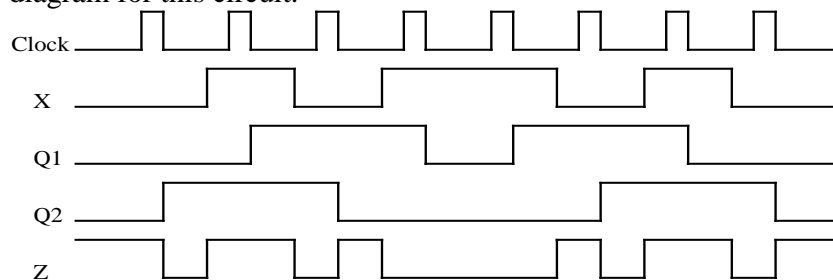
(b) Only four states can be reached from the initial state 000. The next-state table is shown below

$Q_1Q_2Q_3$	X=0	X=1	Z
A-000	000	100	0
B-100	010	100	0
C-010	000	101	0
D-101	010	100	1

This table has only 4 states. So this network can be implemented using just 2 flip-flops. This Moore-style sequence detector generates output $Z=1$ (in state D) if and only if the input pattern 101 is received.

Another Option for Part (b)

A synchronous sequential circuit has one input, X, one output, Z, and two flip-flops, Q1 and Q2. A timing diagram for the circuit is shown below (assuming zero delays in the FFs and the gates.) Is this circuit a Mealy or a Moore model circuit? Construct a transition table and diagram for this circuit.



Solution:

It is a Mealy model since the output changes when the input changes without the state changing.

Transition and Output Table:

Q2	Q1	X=0	X=1
0	0	10, 1	01, 0
0	1	11, 1	00, 0
1	0	00, 0	11, 1
1	1	01, 0	10, 1