Problem #10 Computer Architecture – Solutions

(a) $X = c01480\ldots0$ (hex)

$$= \underset{S}{1}\underbrace{100\ 0000\ 0001}_{E}\ \underbrace{0100\ 1000\ 0\cdots0}_{F}$$

$$\Rightarrow E = 2^{10} + 1 = 1025$$

$$\Rightarrow X = (-1)^1(\underset{\uparrow \text{ implied } 1}{1}.01001)\cdot 2^{1025-1023}$$

$$= -1.01001\cdot 2^2 = -101.001$$

$$\Rightarrow 2X = -1010.01$$

$Y = c02410\ldots0$ (hex)

$$= \underset{S}{1}\underbrace{100\ 0000\ 0010}_{E}\ \underbrace{0100\ 0001\ 0\cdots0}_{F}$$

$$\Rightarrow E = 2^{10} + 2 = 1026$$

$$\Rightarrow Y = (-1)^1(1.01000001)\cdot 2^{1026-1023}$$

$$= -1.01000001\cdot 2^3 = -1010.00001$$

$$\Rightarrow -4y = 101000.001$$

calculation of $2x-4y$:

$$\begin{array}{r} 101000.001 \\ -\,001010.010 \\ \hline 011101.111 \end{array}$$

$$= 1.1101111 \cdot 2^{\textcircled{4}} \rightarrow 1027-1023$$

$\Rightarrow E = 1027 = 1024+2+1$

$= 10000000011$

$S = 0$

$F = 1101111$

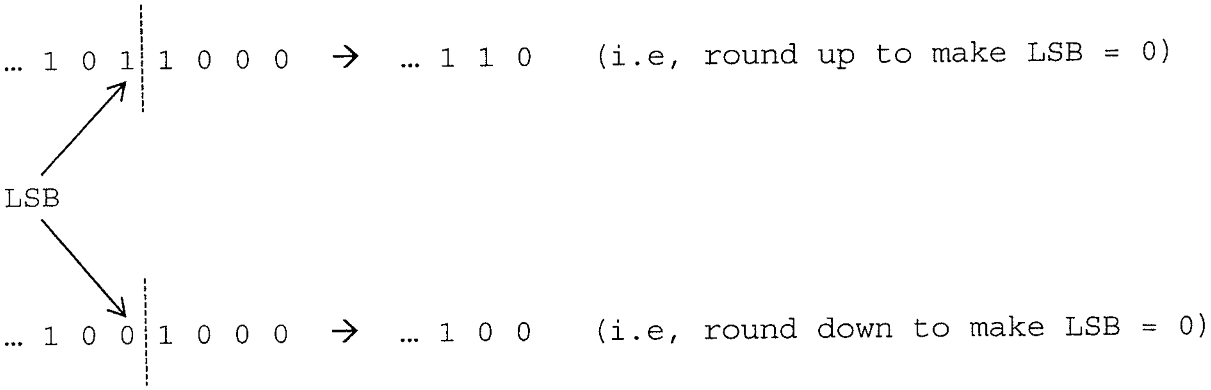
$\Rightarrow$ IEEE format is:

$$\underbrace{0\ 100}_{4}\underbrace{0000}_{0}\underbrace{0011}_{3}\quad\underbrace{1101}_{D}\underbrace{1110}_{E}\underbrace{0\cdots0}_{0\cdots0}$$

$$\Rightarrow \boxed{403DE00000000000}$$

(b) RNE rounds the result conventionally in those cases in which the contribution from the additional bit positions is either greater than or less than half of an LSB (i.e., rounds up if the contribution from the additional bit positions is more than half of an LSB, and rounds down if the contribution from the additional bit positions is less than half of an LSB).

In the special case where the contribution from the additional bit positions is exactly half of an LSB, RNE rounds in such a way as to make the LSB = 0. Two examples are as follows:



... 1 0 1 | 1 0 0 0 → ... 1 1 0 (i.e, round up to make LSB = 0)

LSB

... 1 0 0 | 1 0 0 0 → ... 1 0 0 (i.e, round down to make LSB = 0)

Therefore, on average, in those cases where the contribution from the additional bits is exactly half of an LSB, the result will be rounded up or rounded down approximately the same number of times. This means that the rounding procedure will be essentially free of any inherent bias.

(c) This cache has 8 sets (numbered 0 through 7), and each set contains 8 slots.

Note the following about the specific addresses listed:

(i) All of the even-numbered addresses are mapped into set 6, since they each have a remainder of 6 when divided by 8.

(ii) All of the odd-numbered addresses (except for 33) are mapped into set 5, since they each have a remainder of 5 when divided by 8.

(iii) Address 33 is mapped into set 1, since it has a remainder of 1 when divided by 8.

The hits and misses, as well as the final cache contents, are shown on the following page.

set	address
0	(not used)
1	33
	…
2	(not used)
3	(not used)
4	(not used)
5	53
	61
	29
	37
	45
	21
	77
	85
6	30
	~~86~~ 62
	6
	22
	~~14~~ 46
	78
	70
	54
7	(not used)

30-miss
86-miss
53-miss
61-miss
29-miss
37-miss
30-hit
45-miss
6-miss
22-miss
14-miss
6-hit
53-hit
29-hit
78-miss
22-hit
70-miss
61-hit
54-miss
62-miss
(replaces 86)
45-hit
30-hit
21-miss
77-miss
85-miss
46-miss
(replaces 14)
33-miss

(d) Instructions are:

5B 00 00 37

$\underbrace{0101\ 1}_{\text{LDI}}\underbrace{011\ 0000}_{\text{r12}}\ \underbrace{\ldots}_{,}\ \underbrace{0011\ 0111}_{\#55}$

---

13 59 00 3F

$\underbrace{0001\ 0}_{\text{SUB}}\underbrace{011\ 01}_{\text{r13},}\underbrace{01\ 1001}_{\text{r12},}\ \underbrace{0\ \cdots\ 0011\ 1111}_{\#63}$

---

13 DA 60 00

$\underbrace{0001\ 0}_{\text{SUB}}\underbrace{011\ 11}_{\text{r15},}\underbrace{01\ 1010}_{\text{r13},}\ \underbrace{0110\ 0}_{\text{r12}}\ \ldots\ 0$

F8 00 00 00

$\underbrace{1111\ 1}_{\text{HLT}}000\ \ 0\ \cdots\ 0$

Results after each instruction are:

```
Instruction #1:         LDI r12, #55
Condition codes:        C=x  V=x  Z=x  N=x
R[12 - 15]:             00000037  xxxxxxxx  xxxxxxxx  xxxxxxxx

Instruction #2:         SUB r13, r12, #63
Condition codes:        C=1  V=0  Z=0  N=1
R[12 - 15]:             00000037  fffffff8  xxxxxxxx  xxxxxxxx

Instruction #3:         SUB r15, r13, r12
Condition codes:        C=0  V=0  Z=0  N=1
R[12 - 15]:             00000037  fffffff8  xxxxxxxx  ffffffc1

Instruction #4:         HLT
Condition codes:        C=0  V=0  Z=0  N=1
R[12 - 15]:             00000037  fffffff8  xxxxxxxx  ffffffc1
```