The circuit shown below is a differential amplifier. The transistors Q1, Q2, Q6, Q7, and Q8 are NMOS. Q3, Q4, and Q5 are PMOS. All transistors have their bodies connected to their sources, as shown in the figure. The non-inverting input is located at the gate of Q1, inverting input is located at the gate of Q2, and the output is located at the connected drains of Q5 and Q6.

The parameters have the following values (see the attached tables 5.1, 5.2, and 7.2):
\[ V_{in}=V_{tp}=0.5\, \text{V}, \quad k_n=2k_p=40\mu\text{A/V}^2, \quad |V_A|=10\, \text{V}. \]

W/L ratios:

<table>
<thead>
<tr>
<th></th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q5</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>20/1</td>
<td>20/1</td>
<td>40/1</td>
<td>80/1</td>
<td>40/1</td>
</tr>
<tr>
<td>Q6</td>
<td>Q7</td>
<td>Q8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20/1</td>
<td>40/1</td>
<td>20/1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Finally \[ V_{DD}=V_{SS}=5\, \text{V} \] and the resistor R1 has been selected to make the drain current of Q6 equal to \[ 9\mu\text{A} \]. VBIAS is adjusted to allow for maximum output range.

![Circuit Diagram](image)

a) Determine the overall differential voltage gain of this amplifier. (2 points)
b) What value of VBIAS gives the maximum output range? What is that range? (1 point)
c) The voltage gain of this amplifier can be boosted significantly if Q8 is modified by adding an identical transistor in a cascode connection to Q8 (call it Q8A). If this is done what will the gain increase? (1 point)
Table 5.1 Regions of Operation of the Enhancement NMOS Transistor

<table>
<thead>
<tr>
<th>Region</th>
<th>Expression</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Triode Region</td>
<td>$i_D = \frac{1}{2} k_n' \left( \frac{W}{L} \right) v_{DS}^2$</td>
<td>$v_{DS} &lt; v_{OV}$</td>
</tr>
<tr>
<td>Saturation Region</td>
<td>$i_D = \frac{1}{2} k_n' \left( \frac{W}{L} \right) v_{OV}^2$</td>
<td>$v_{DS} \geq v_{OV}$</td>
</tr>
</tbody>
</table>

- $v_{GS} < V_{in}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{in} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end.

**Triode Region**
- Continuous channel, obtained by: $v_{GD} > V_{in}$
- or equivalently: $v_{DS} < v_{OV}$

Then,
- $i_D = k_n' \left( \frac{W}{L} \right) \left[ (v_{GS} - V_{in}) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$
- or equivalently,
- $i_D = k_n' \left( \frac{W}{L} \right) \left( v_{GS} - \frac{1}{2} v_{DS} \right) v_{DS}$

**Saturation Region**
- Pinched-off channel, obtained by: $v_{GD} \leq V_{in}$
- or equivalently: $v_{DS} \geq v_{OV}$

Then,
- $i_D = \frac{1}{2} k_n' \left( \frac{W}{L} \right) (v_{GS} - V_{in})^2$
- or equivalently,
- $i_D = \frac{1}{2} k_n' \left( \frac{W}{L} \right) v_{OV}^2$
Table 5.2 Regions of Operation of the Enhancement PMOS Transistor

<table>
<thead>
<tr>
<th>Condition</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$v_{SG} &lt;</td>
<td>V_{tp}</td>
</tr>
<tr>
<td>$v_{SG} =</td>
<td>V_{tp}</td>
</tr>
</tbody>
</table>

**Triode Region**

- Continuous channel, obtained by:
  - $v_{DG} > |V_{tp}|$
  - or equivalently $v_{SD} < |V_{OV}|$
- Then $i_D = k_p \left( \frac{W}{L} \right) \left( v_{SG} - |V_{tp}| \right) v_{SD} - \frac{1}{2} v_{SD}^2$
- or equivalently $i_D = k_p \left( \frac{W}{L} \right) (v_{SD} - |V_{tp}|) v_{SD}$

**Saturation Region**

- Pinched-off channel, obtained by:
  - $v_{DG} \leq |V_{tp}|$
  - or equivalently $v_{SD} \geq |V_{OV}|$
- Then $i_D = \frac{1}{2} k_p \left( \frac{W}{L} \right) (v_{SG} - |V_{tp}|)^2$
- or equivalently $i_D = \frac{1}{2} k_p \left( \frac{W}{L} \right) v_{OV}^2$
### Table 7.2 Small-Signal Models of the MOSFET

**Small-Signal Parameters**

**NMOS transistors**

- Transconductance:
  \[ g_m = \mu_c C_{ox} \frac{W}{L} V_{GS} = \sqrt{2\mu_c C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{GS}} \]

- Output resistance:
  \[ r_o = \frac{V_D}{I_D} = \frac{1}{g_m} \]

**PMOS transistors**

Same formulas as for NMOS except using \( V_{GS} \), \( |V_A| \), \( I_A \) and replacing \( \mu \) with \( \mu_p \).

**Small-Signal, Equivalent-Circuit Models**

![Diagram of Hybrid-\( \pi \) and T models]

- **Hybrid-\( \pi \) model**
- **T models**