(a) If r6 = 0, then r8 = 1. For all other values of r6, r8 = 0.

(b) flow dependence from instruction I1 to instruction I3 through r4
flow dependence from instruction I2 to instruction I3 through r6
instruction I1 is anti-dependent on instruction I2 through r6
instructions I1 and I3 are output dependent through r4

(c) \( z_1 = x_1 + y_1 \) using RMI.
\[ z_2 = x_2 + y_2 \] using RPI.
These will guarantee that \( z_1 \) is less than or equal to the real value of \( x + y \) and that \( z_2 \) is greater than or equal to the real value of \( x + y \).

(d) In a write-through cache, when a write occurs both the cache and the next level of the memory hierarchy (e.g. main memory in a system with only one level of cache) are updated with the new value. Thus, the two levels of memory are always consistent with each other. On the other hand, in a write-back cache, only the cache is updated on a write. The next level of the memory hierarchy would be updated at the time that the cache block is replaced. As a result, a write-through cache typically requires a higher bus bandwidth.

(e) page size of 128K bytes => 17-bit page offset => 40 – 17 = 23-bit virtual page number:

\[
\begin{array}{c|c}
\text{virtual page number} & \text{page offset} \\
\hline
\end{array}
\]

\[
\begin{array}{c|c}
\multicolumn{2}{c}{40} \\
\hline
23 & 17 \\
\hline
\end{array}
\]

=> number of page table entries is \( 2^{23} \)
each entry is 48 bits = 6 bytes

=> total size of the page table = \( (2^{23})(6 \text{ bytes}) = 48 \text{ Mbytes} \)