(a) (2points) The circuit shown below implements a positive edge-triggered D flip-flop using 6 NAND gates. Assuming that each NAND gate is replaced with NOR gate, what is the function of this new circuit? – Explain your answer.

Solution: with NOR gates, this circuit implements negative edge-triggered D flip-flop. Explanation is given below.

Consider the output-stage SR flip flop:
For this output flip-flop, the values SR determine the operation (function) of the circuit. Consider 4 possibilities for the input stage of the circuit:

- When CP=1 and D=0 \( \rightarrow \) stable values SR = 00
- When CP=0 and D=0 \( \rightarrow \) stable values SR = 01
- When CP=1 and D=1 \( \rightarrow \) stable values SR = 00
- When CP=0 and D=1 \( \rightarrow \) stable values SR = 10

So the output-stage FF is:
- reset when D=0 and CP: 1\( \rightarrow \) 0
- set when D=1 and CP: 1\( \rightarrow \) 0

This is a negative edge triggered D flip-flop.

(b) (2 points) Consider a single input, single output Mealy-style sequence detector such that \( Z=1 \) if and only if the input \( x \) has been alternating for last two clock cycles. In other words, the output \( Z=1 \) if and only if the input sequence 010 or 101 is detected.

For example:
\[
\begin{align*}
x &= 0010100011101000... \\
Z &= 0001110000001100...
\end{align*}
\]

Implement this sequence detector using an 8-bit serial-in, parallel-out shift register (shown below) and a few gates. This shift register has a single serial input (SI), and 8 outputs A,B,...,G,H. Assume that initially the register is cleared.

![Shift Register Diagram]

**Solution:**
Apply input \( X \) to Serial Input, and then use two most recently received inputs stored as contents of A and B in the shift register.
Then output \( Z=1 \) if \( (AB=01 \text{ and } X=1) \) OR \( (AB=10 \text{ and } X=0) \).
So the Mealy output \( Z = XA'B + X'AB' \) which can be implemented using AND, OR, NOT gates (not shown).