

# Hakim Alhussien

**CAMPUS:**

200 Union St. SE  
Minneapolis, MN 55455  
Phone: 612-229-2080, Fax: 612-626-1050  
[hakimh@umn.edu](mailto:hakimh@umn.edu)

**PERMANENT:**

1237 Ray Place  
St. Paul, MN 55108

**OBJECTIVE:** To find a full time job position in the area of digital signal processing or VLSI design of data storage systems

**EDUCATION:** **Philosophical Doctor in Electrical Engineering, expected graduation date: fall 2008**

University of Minnesota, Minneapolis, Minnesota  
Thesis: Channel Matched Iterative Decoding for Magnetic Recording Systems  
Adviser: Prof. J. Moon  
GPA: 3.88/4.00

**Master of Science in Electrical Engineering, September 2003**

Jordan University of Science and Technology, Irbid, Jordan  
Thesis: Performance Bounds for Selection Combiners in WCDMA Rake Receivers.  
Adviser: Prof. Mohammad Banat

**Bachelor of Science in Electrical Engineering, September 2001**

Jordan University of Science and Technology, Irbid, Jordan  
Ranked first among 160 students and graduated with highest honors, GPA: 93.1/100

**EXPERIENCE:** **Research Assistant, May 2005 to Present**  
**Communications and Data Storage (CDS) Lab., Electrical and Computer Engineering,**  
**University of Minnesota, Minneapolis, Minnesota**

- Investigated channel estimation algorithms for MIMO-OFDM systems.
- Analyzed the capacity of ISI channels in AWGN and media noise.
- Developed a read channel model of perpendicular magnetic recording (PMR) systems.
- Designed PRML targets for the media noise dominated PMR read channel.
- Analyzed and simulated pattern-dependent noise prediction in PMR.
- Investigated turbo codes as inner codes for Reed Solomon (RS) codes, and studied their SER using the block-multinomial method.
- Designed and simulated low complexity turbo equalizers via trellis state-reduction techniques applied to noise predictive channel detectors.
- Analyzed the computational complexity of LDPC and convolutional code based turbo equalizer systems incorporating outer RS codes.
- Simulated ML decoding of the channel tailored error-pattern correction code (EPCC) developed in CDSLab.
- Developed an iterative SISO decoder for EPCC, and studied the BER and SER of EPCC enhanced turbo equalizers.
- Developed a turbo product code (TPC) based on EPCC component codes and studied its BER and SER.
- Investigated EPCC as means to enhance Quasi-cyclic LDPC code performance.
- Developed a tensor product code based on RS and EPCC and investigated the BER and SER of its hard decoder.
- Developed a tensor product code based on non-binary LDPC and EPCC and developed a soft decoder based on the soft-syndrome concept.
- Studied the design of non-binary LDPC using the progressive edge growth algorithm.

**Teaching Assistant, August 2004 to May 2007**

**Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota**

- Exam, project, and homework problem design and grading, lab administration, and substitute lecturing for courses and labs on communications, information theory, and error correction coding.

**Lecturer, May 2003 to July 2004**

**Electrical and Computer Engineering, Yarmouk University, Irbid, Jordan**

- Taught digital communications courses for senior level students.

**ASIC Design Engineer, Intern, Summer 2001**

**Telematix Corp. Newport Beach CA, Amman office location, Amman, Jordan**

- Designed I/O interfaces for USB devices.

**PROJECTS:**

**INSIC Extremely High Density Recording Program, May 2006 to February 2008**

**Title: Low Complexity Turbo Equalization.**

- Developed EPCC-enhanced low-complexity turbo equalizers for the signal processing realization of the 1 Tb/in<sup>2</sup> areal density roadmap.

**Verilog Implementation of Reed-Solomon Berlekamp-Massey Decoder, VLSI Design Lab**

- Designed a Berlekamp-Massey circuit with optimized area, power, and fault coverage.
- Run formal verification of circuit and simulation in AWGN.

**VLSI Circuit Design of A High Speed 16-bit Adder, VLSI Design I course project.**

- Designed a VLSI circuit with optimized area, power, and speed, using Cadence HDL, then simulated performance using HSPICE.

**COURSES:**

- Error Correcting Codes, Magnetic Recording, Information Theory, Digital Communications,
- Adaptive Signal Processing, Convex Optimization, Queuing Systems,
- VLSI Design I, VLSI Design lab, VLSI DSP systems, Matrix Computation.

**SKILLS:**

- C/C++, Matlab, Java,
- Verilog HDL, Simulink, Cadence SPW,
- Synopsys design tools, Cadence HDL simulators, HSPICE.

**SELECTED**

- PUBLICATIONS:**
- Hakim AlHussien, J. Park and J. Moon, "Iterative Decoding Based on Error-Pattern Correction," *IEEE Trans. Magn.*, vol.44, no.1, pp.181-186, Jan. 2008.
  - Hakim AlHussien and M. M. Banat, "Probability of Error Analysis of Predetection Generalized Selection Combining Receivers with Correlated Unbalanced Nakagami Branches," *Wireless Communications and Mobile Computing*, Vol. 7, No. 6, pp. 689-701, August 2007.

**PROFESSIONAL**

- ACTIVITIES:**
- Served as reviewer for several IEEE journals and served as TPC member in MCWC 2006 M-CSC 2007, and M-WCMC 2007.

- AWARDS:**
- The award for Academic Undergraduate Excellence 2000, awarded by Queen Rania of Jordan.

**REFERENCE:**

Prof. J. Moon, University of Minnesota, Minneapolis, MN

E-mail: [moon@umn.edu](mailto:moon@umn.edu), Phone: 612-625-7322

Prof. Tom Luo, University of Minnesota, Minneapolis, MN

E-mail: [luozq@ece.umn.edu](mailto:luozq@ece.umn.edu), Phone: 612-625-0242

Prof. Mohamed-Slim Alouini, Texas A&M University at Qatar, Qatar

E-mail: [alouini@qatar.tamu.edu](mailto:alouini@qatar.tamu.edu), Phone: +974-423-0019