Patterning of Electrons and Holes for Data Storage and High Resolution Charge Based Printing

Heiko O. Jacobs

University of Minnesota, Department of Electrical and Computer Engineering, 200 Union Street SE , Minneapolis, 55455, Email: hjacobs@ece.umn.edu, http://www.ece.umn.edu/users/hjacobs/

We review scanning probe based strategies to pattern charge in thin film electrets and present results on a new parallel strategy that is based on a flexible, electrically conductive, electrode. This electrode consist of a poly(dimethylsiloxane) (PDMS) stamp, patterned in bas-relief and supporting a 80-nanometer thick gold film. This stamp allows the formation of mulitple electric cantacts and parallel electrical exposure of a rigid surface. Using these stamps we have been able to pattern charge over > 1 cm^2 sized areas at ~100 nm resolution in less than 10 s. This process provides a new method for patterning; it suggests possible methods for high-density, charge-based data storage and for high-resolution charge-based printing.

Introduction

Electrets are materials than can retain trapped electrical charge or polarization (*1*). Systems that write and read patterns of charge have been explored extensively, because of their potential in rewriteable digital data storage (*2-5*). Current procedures based on scanning probes achieve a writing rate of 100 kbits/s at an areal density of 7 Gbits/cm2 (120 nm bit size), and achieve sub-100 nm resolution. Although this density is about 140 times the areal density of optical compact discs, the writing rate is slow. At this rate, a day is required to pattern an area of 1 cm^2. To overcome the speed limitation of scanning probe we present a methode that uses a conductive stamp that is flexible and that allows the formation of multiple electric contacts of different size and shape to a rigid surface.

Experimental

The experimental strategy is illustrated in Fig. 1 A-B. The stamp was poly(dimethylsiloxane) (PDMS), patterned in bas relief using procedures described before (*6*); it was ~5 mm thick and supported on a glass slide. The patterned surface of the PDMS stamp was made electrically conducting by thermal evaporation of 7 nm of chromium (as an adhesion promoter) and 80 nm of gold onto it. Poly(methylmethacrylate), an 80-nm film on a <100> n-doped silicon wafer with a resistivity of 3 ohm cm, was the charge storage medium. To generate a pattern of trapped charge, we placed the metal-coated PDMS stamp on top of the PMMA film and applied a voltage of 10 to 20 V between the gold on the PDMS and the back side of the silicon. During the patterning, we monitored the current (typically: 1 to 20 mA/cm^2) and the total charge transferred through the entire junction (10 to 100 mC/cm^2, 600 to 6000 $electrons/nm^2$). After turning off the applied potential, we removed the PDMS stamp by hand.

Results

Fig. 1 D shows ring type charge patterns with 130 nm sized features and (E) shows a surface patterned in a way that simulates high-density data storage (full-width at half-maximum, FWHM, <150 nm, density = 5 $Gbits/cm^2$). The surface charge distribution was detected using Kelvin probe force microscopy (*7*). The detected change in the surface potential is > 1 V which corresponds to a charge density of approximately 100 elementary charges / $(100\ nm)^2$. The smallest charged areas we have generated are about 150 nm wide. At these scales, the transfer function of the Kelvin probe limits the resolution (*8*). For more details and applications in the area of high resolution charge based printing we refere to a recent paper published in Science (9).

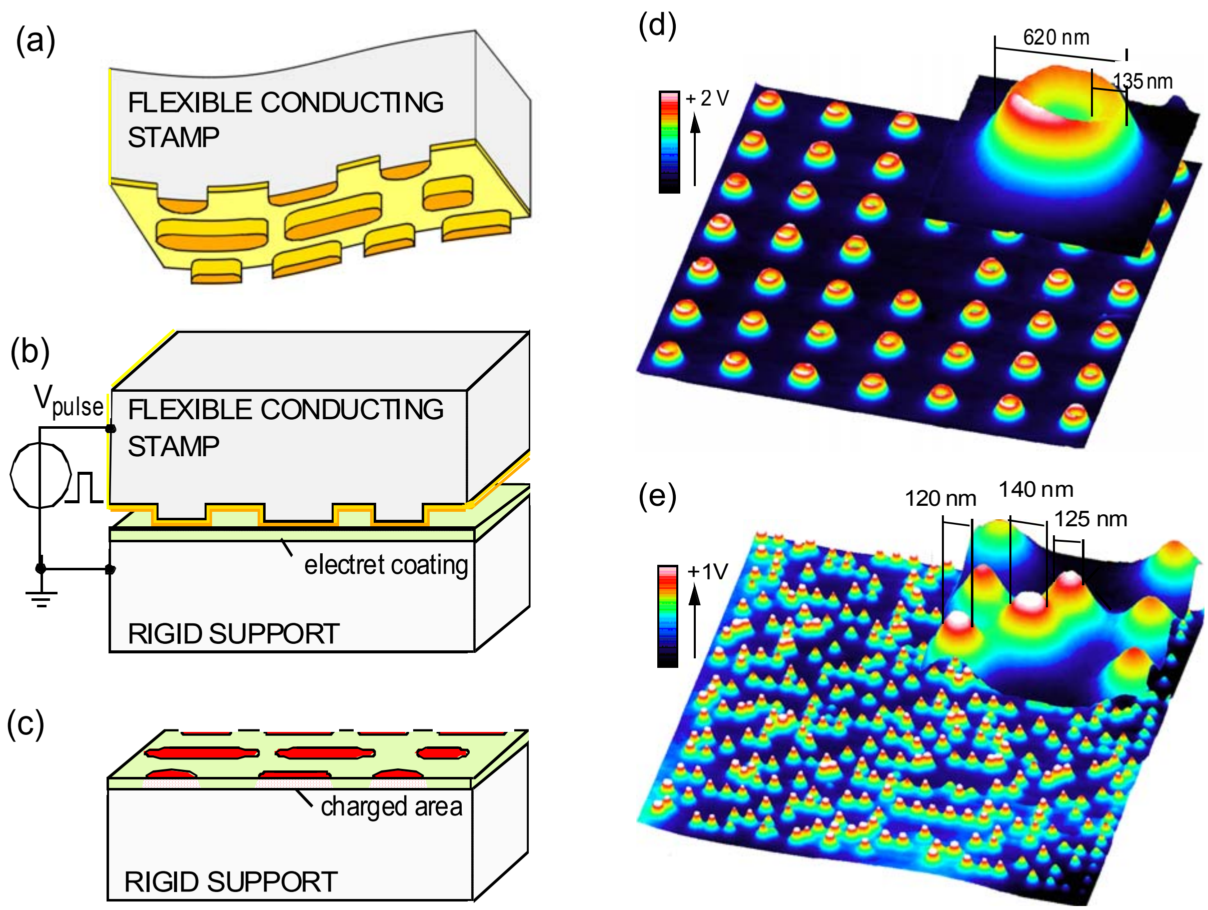

Fig. 1 Principle of parallel charge patterning (left) and representative images of different sized charge patterns (right). The illustration can be broken down as follows: (a) The flexible conducting stamp is placed on top of the electret and forms an electrical contact; (b) an external voltage is applied between both electrodes to pattern charge in the electret; (c) the stamp is removed and the charge pattern is recorded using Kelvin probe force microscopy; (d) results show a ring type charge patterns 620 nm in diameter (FWHM) with ~130 nm sized features; and (e) results show a pattern of trapped charges for high density data storage with <150 nm sized bits.

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