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Field-Effect Transistor Built with a Single Crystal Si Nanoparticle

Yongping Ding, Ying Dong, Stephen A. Campbell, and Heiko O. Jacobs
Department of Electrical Engineering, University of Minnesota

A. Bapat and U. Kortshagen
Department of Mechanical Engineering, University of Minnesota

Chris Perrey and C. Barry Carter
Department of Chemical Engineering and Materials Science, University of Minnesota

Abstract: Our program involve the synthesis, assembly, and structural and electrical characterization of single crystal Si nanoparticles. The goal of this work is developing high-speed electrical nanoparticle devices. In this article we review the processes needed to demonstrate a vertical transistor built using PtSi as a Schottky barrier source and drain. A surround-gate of Pt is insulated from body of the Si nanoparticle by 2 nm of SiO_2. A group of such nanoparticle transistors were self-aligned and connected in parallel for electrical characterization. The fabrication processes were based on conventional semiconductor manufacturing technologies without any sophisticated photolithography. Ultrathin etching and CMP steps were developed. As a result, control of the drain/source current by the gate voltage was observed on the transistor. We believe that this is the first time that such a transistor has been built using a crystalline Si nanoparticle.

1. Introduction

It is predicted that the continuous improvement in the performance of conventional, top-down integrated circuits will end in about ten years[1,2]. This has spurred a great deal of research into novel devices. In the near term, the most likely device to replace the conventional planar metal-oxide-semiconductor field effect transistor (MOSFET) is a nonplanar variation of the same device[3-6]. Such a nonplanar structure increases the device drive current by increasing the surface (channel) area of the transistors, but do not improve overall system performance as dramatically. Interconnect limits the performance of digital circuits that use such highly scaled devices. Copper and low permittivity insulators have reduced interconnect delays, but as devices scale below gate lengths of 50 nm, even these improvements become insufficient [7]. Interconnect limitations are even more obvious at the system level where chips running at 3 GHz are being put on boards running an order of magnitude slower. Many of the nanodevices that have been proposed as a long term replacement to the MOSFET display interesting physics, but have a limited current output or have poor yields that would necessitate a "fat-tree" architecture [8] which further exacerbates interconnect-related on-chip delays. Thus, once scaling of the planar MOSFET is complete, it is most likely to be replaced by a nonplanar version of the same device.

A much more powerful solution to these scaling limitations would be to move from integrated circuits to integrated systems: chips that have many levels of different types of devices on a single substrate. For example, such a system could have numerous layers of transistors interspersed with interconnect. GaAs devices might be used for RF communication, while silicon devices are used for logic. Optical devices such as lasers and LEDs could be used for off-chip and cross-chip communication and magnetic devices for remote power and nonvolatile storage. By monolithically integrating different materials and devices into a single component, system speed would increase substantially as "bus" distances fall from centimeters to microns. The obvious problem with this approach is that there is no known way to form single crystal layers of lattice-mismatched, chemically incompatible materials on an arbitrary substrate.

Using high-quality single crystal particles instead of heterogeneous epitaxial layers maybe a way to meet the materials requirements of this integrated information system. If their size and location can be controlled, one only needs islands of high quality single crystals that are the size of the device. As devices scale to tens of nm, this becomes an increasingly attractive approach. We therefore propose a new approach to the manufacture of information systems: the directed self-assembly of single crystal semiconductor nanoparticles for building devices.

In this study, we have attempted to fabricate a vertical PtSi Schottky barrier MOSFET with a wrap-around-gate using Si nanoparticles (SiNP) and conventional semiconductor manufacturing technologies. The performance of the single SiNP transistor was measured and extracted by a group of randomly distributed but self-aligned SiNP transistors that are connected in parallel. An on/off characteristic of such a P-channel device was obtained and is discussed.

2. Device Structure and fabrication Process

Figure 1(a) shows a schematic cross-section of a vertical wrap-around-gate FET built in a SiNP. A ~40 nm cubic Si nanoparticle is buried in a Pt/SiO_2/Pt/SiO_2/Pt multi-layer stack, where three layers of Pt act as source, gate and drain electrodes respectively. Two layers of CVD SiO_2 are employed as insulators. The thickness of Pt layer of gate electrode, corresponding roughly to the physical

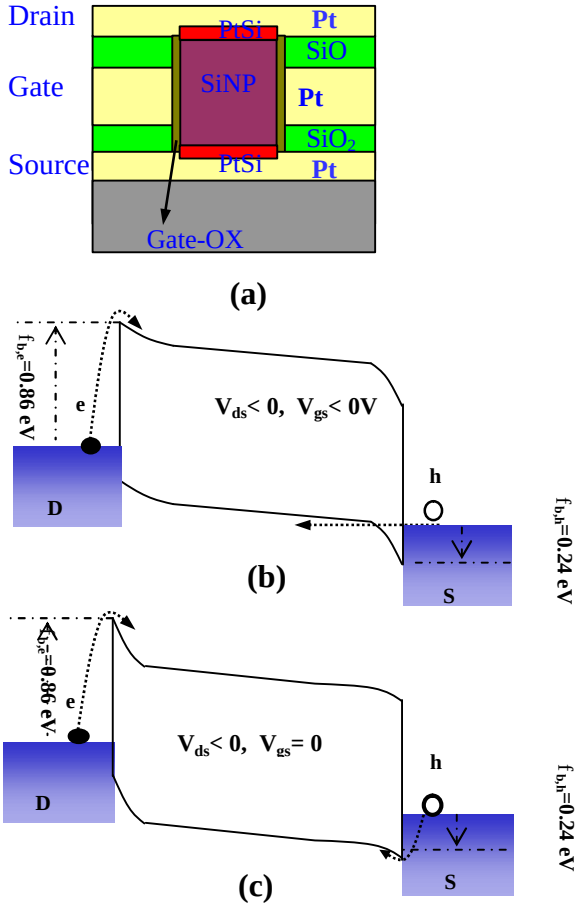

Fig. 1. (a) Cross-section schematic of the vertical PtSi Schottky source/drain SiNP-MOSFET. (b) Band diagram of the "on" state with a high gate bias, large electrical fields induced hole tunneling from the source. (c) Band diagram of the "off" state with no gate bias and a thick source barrier where the current is restricted to thermal emission.

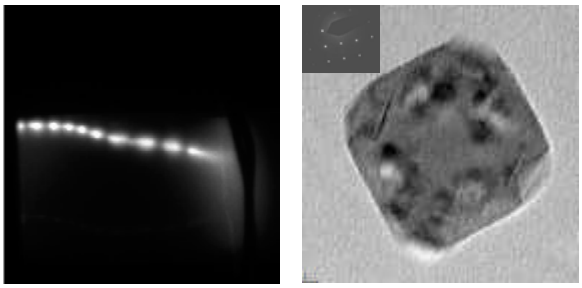

Fig. 2. (a) Pinched plasma discharge showing unsteady, extremely high density plasma. (b) Typical 40 nm particle showing single crystalline.

channel length, is about 15 nm. The side-faces of the SiNP is covered by a 2 nm chemical-thermal SiO_2 layer grown during processing. Thus the SiNP is electrically insulated from gate Pt layer. At the bottom and top of the SiNP, however, the source and drain Pt layers contact the particle directly. By proper heat-treatments, these two Pt layers react with the silicon to form PtSi/Si Schottky barriers. PtSi is often used as the source and drain of p-channel Schottky metal oxide semiconductor field-effect transistors (SBMOSFETs), because of it's low Schottky barrier height (0.24 eV) for holes but high barrier height (0.86 eV) for electrons. A small barrier is needed at source to induce large hole tunnel currents in the on state for practical values of gate voltage, as shown in Figure 1(b). Conversely, a high barrier for electrons is needed to suppress reverse tunneling and thermal emission of electron at drain in the off state, as in Figure 1(c). Because the field emission current depends on barrier height to the 3/2's power ($\phi_b^{3/2}$), large on/off ratios can be achieved, even in undoped SBMOSFETs of this type [9, 10].

The creation of nonagglomerated monodisperse cubes of single crystal silicon with (100) faces is a critical step in the device fabrication. By operating a silane plasma reactor in a "pinched-plasma" mode, extremely high power densities are achieved locally. This process is capable of making highly monodisperse cubes with (100) faces. Figure 2(a) shows the plasma discharge which is used to generate the SiNPs. Figure 2(b) shows a typical TEM of the generated particles. They are cubic with a size of ~ 40 nm. The corresponding selected-area electron diffraction pattern reveals their crystallinity. The regular diffraction spots could be indexed to [100] zone axis of diamond-like structure of Si crystal and the facets of the cube are determined to be (100)-faces. The generated SiNPs also have a good uniformity in size. Statistical measurement by TEM shows their standard deviation to be less than 3%.

The SiNPs were impacted onto a Pt- metallized substrate, which was deposited onto a patterned CVD SiO_2 layer. The windows in the oxide are the sites for building the SiNP transistor clusters. The SiNPs contact with the

bottom Pt layer only at in these window areas. Beyond the window areas, SiNPs stay on surface of the patterned CVD SiO_2, see Figure 3(a). After heat treatment, only those SiNPs at the window areas will react with the bottom Pt layer to form several nanometers of PtSi. The patterned substrate helps to remove the unwanted NPs. After the particle deposition another oxide payer is deposited (Figure 3(b)) and subsequently planarized by chemical mechanical polishing (CMP). When the thickness of covering SiO_2 layer decreases to the original oxide thickness, the particles outside the window areas are polished away as illustrated in Figure 3(c).

The number of NPs at every window is dependent on its area and on the particle deposition time. We defined windows ranging in size from 5x5 um^2 to 20x20 um^2. An average density of ~1.6 NPs/μm^2 were obtained after a 1 minute deposition. For ease of electrical connection and characterization of the nanoparticle transistor, all the SiNPs in the same window will be developed into a nanoparticle transistor simultaneously, putting all of the devices in a window in parallel.

After the CMP planarization, a dry etch process with a high SiO_2/Si selectivity was performed to etch back the SiO_2 uniformly. The etch is stopped when the thickness of the SiO_2 decreases to 10-15 nm, or about one third of the height of SiNPs. This 10-15 nm thin SiO_2 layer is used as the insulating layer between source and gate electrodes. The control of 10-15 nm CVD SiO_2 by dry etching is challenging, especially considering the additional requirement of low surface roughness. An AFM was employed to monitor this step. As shown in Figure 4(a) that the height of exposed SiNPs is ~ 26 nm and the mean roughness (Rq) of the SiO_2 surface after etching is ~1.5 nm or better.

In order to form the gate insulator surrounding the exposed SiNPs without exposing the PtSi contact to an excessively high temperature, the platform was first immersed into boiling H_2O_2 for 30 minutes and then put into an oxygen atmosphere at 500^0C for another 30

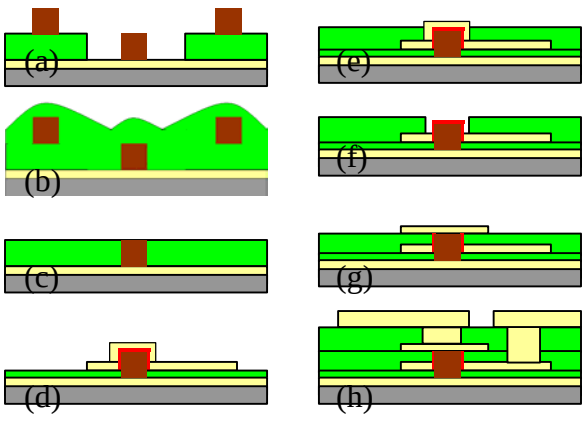

Fig. 3. Schematic of the fabrication process flow.

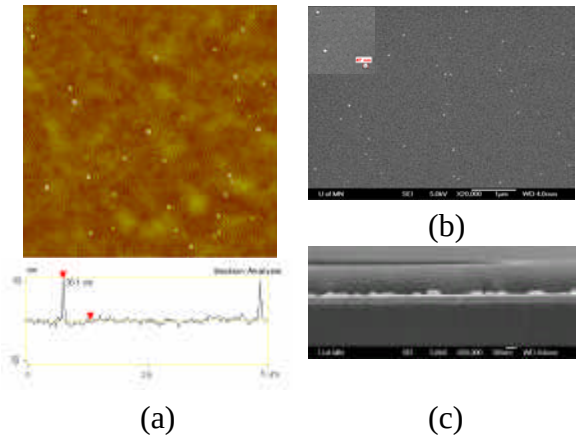

Fig. 4. (a) AFM picture after CVD SiO_2 etched back, showing the height of exposed SiNPs ~26 nm. (b) Over-view of the surface after gate-Pt deposition by FESEM. (c) Cross-sectional picture by FE-SEM before gate-Pt adjustment

minutes. Using the same oxidation process, a (100) Si monitor wafer revealed a ~2 nm thermal silicon oxide formed on surface and a leakage current as low as $1.8x10^{-5}$ A/cm^2 at a bias voltage of 0.5 V. This electrical performance can satisfy the requirements for the gate insulator of the transistor. A ~15 nm Pt metal layer was then deposited as gate metal surrounding the thermal silicon oxide coated SiNPs, as shown in Figure 3(d). The thickness control of the gate metal deposition serves to define the vertical channel length of the transistor. It is necessary to note that before this deposition, the platform had been patterned by photo resist. Nearly same pattern as the windows were used and aligned here, but extended in one direction. This extended area was reserved for a gate contact. A lift-off process was employed at this step. Figure 4(b) shows a SEM picture after the gate Pt deposition. The size of the SiNP became larger than as-deposited because of the Pt-coatings. Another cycle of CVD SiO_2 deposition and CMP was performed to planarize the surface. Figure 4(c) shows a cross-section SEM picture after this step. An etchback of the planarized surface is then done to expose the top of the Pt-encapsulated NPs. See Figure 3(e). Wet etching in diluted aqua regia followed to remove the Pt coating on the top of the NPs first and later along the side of the NPs. This is doe to prevent gate to drain short circuits. A goal for this step is shown in Figure 3(f): to gate Pt keep close contact with SiNPs in surround but no longer cover the particles on top and side. Any insufficient or over etching of the Pt gate will both result in failure of the transistor, either by shorting or a loss of gate control. A recess was then introduced after this wet etching but would be filled by following SiO_2 CVD. CMP was used for a third time to expose the tops of NPs prior to laying down a top Pt electrode, which reacted with the surface of SiNPs lightly

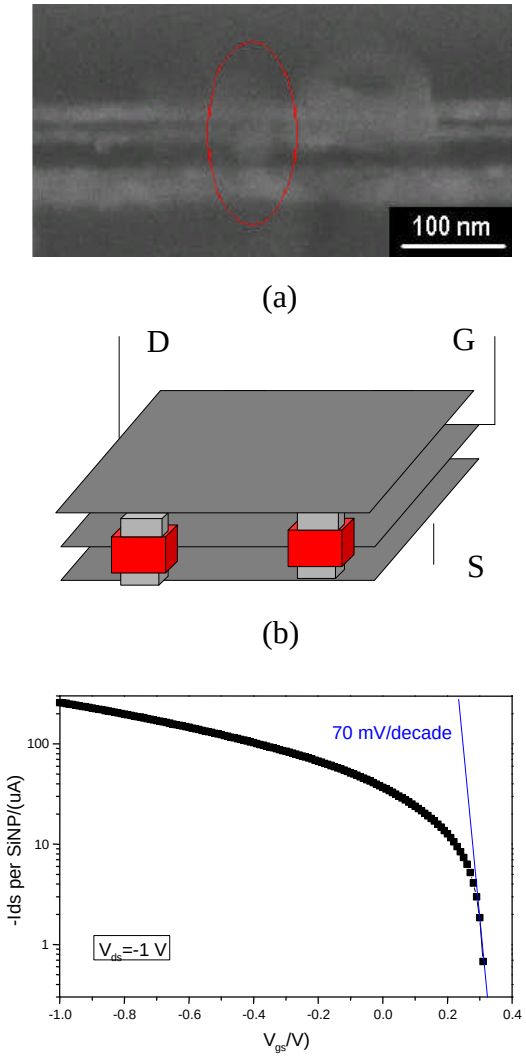

Fig. 5. (a) SEM of completed device showing three metal layers. (b) Schematic cluster of SiNP transistors in parallel. (c) Single SiNP transistor's I-V characteristics showing turn off characteristic of p-channel device

and formed the drain Schottky junction, as shown in Figure 3(g).

To get reliable electrical test results under microprobing, we built a test structure for the devices. This structure was designed to avoid direct contact of probes onto the top of the devices. A passive layer of 500 nm CVD SiO_2 was deposited, patterned and etched to realize contacts to the gate and drain, as shown in Fig 3(h).

3. Device Characteristics

Figure 5(a) shows a cross-sectional picture of a completed SiNP transistor by field emission SEM. The three layers of Pt metal embedded with a SiNP was observed. A group of such transistors were connected in parallel and measured, as illustrated in Figure 5(b).

A typical transistor outcome, controllable drain current (I_d) by varying the gate-source voltage (V_{gs}) was observed for the SiNP-transistors. Divided by the number of SiNPs connected in parallel in one group, the I_d-V_{gs} characteristic for one SiNP transistor is extracted and plotted as in Figure 4. With the change of V_{gs} from 0 V to 0.3 V, the I_d decreased from 40 uA to 0.7 uA under constant drain-source voltage (V_{ds}) of -1 V. The NPs transistor showed a turn-off characteristic of P-channel device. The subthreshold swing (S-factor) is approximately 70 mV/decade. When the gate is negatively biased, the drain current increases from 40 uA 0 V to ~200 uA at –1 V.

These SiNPs were synthesized in a plasma without any addition of n- or p- dopant into precursors. Therefore, at equilibrium, all SiNPs should be chemically intrinsic and have equal concentration of carriers of electrons and holes. Because of the larger barrier height (0.84 eV) for electrons than that for holes (0.24 eV), the source/drain current is dominated by hole transport. The concentration of holes is suppressed and the drain/source current turned off with a positive gate to source bias. On the other hand, a negative bias of gate to source induces tunneling of holes from source as illustrated in Figure 1(b), and increases the drain current.

4. Conclusion

A vertical surround-gate MOSFET using ~40 nm Si nanoparticles were proposed and demonstrated. Electrical characterization showed a p-channel gate controlled the drain/source current. These results show promise for developing hyper integration and 3D IC using SiNPs in the future nano-systems.

5. Acknowledgements This work was supported by NSF GRANT # DMI-0304211

6. References

[1] Ren, Z.V., R. Datta, S. Lundstrom, M. Jovanovic, D. Fossum, J. *"The ballistic nanotransistor: A simulation study"*, in *International Electron Devices Meeting*. 2000: IEEE.

[2] Natori, K., *"Scaling limit of the MOS transistor - A ballistic MOSFET.* IEICE Transactions on Electronics",Vol.8, pp. 1029-1036. 2001.

[3] Li, R.Z., Y. Lu, Y. Daniel Sung Choi. Luo, M. Wang, K L. *"50 nm vertical surround gate MOSFET with S-factor of 75mV/dec"*, in *Annual Device Research Conference*. 2001.

[4] J. M. Hergenrother, S.H.O., T. Nigam, D. Monroe, F. P. Klemens, and A.Kornblit, *"The vertical replacement-gate (VRG) MOSFET"*, Solid-State Electronics, Vol.**46**(7), pp. 939-950.2002.

[5] Kranti, A.R.H., S. Gupta, R S., "*Design and optimization of thin film fully depleted vertical surrounding gate (VSG) MOSFETs for enhanced short channel immunity",* Solid-State Electronics, Vol. **46**(9), pp.1333-1338, 2002.
[6] Osburn, C.M.K., Indong. Han, Sungkee. De, Indranil. Yee, Kam F. Gannavaram, Shyam. Lee, SungJoo. Lee, Chung-Ho. Luo, Zhijiong J. Zhu, Wenjuan. Hauser, John R. Kwong, Dim-Lee. Lucovsky, and M.C.M. Gerald. Ozturk, T P., "*Vertically scaled MOSFET gate stacks and junctions: How far are we likely to go?",* IBM Journal of Research & Development, Vol. **46**(2-3), pp.299-315, 2002.
[7] Ohba, T., "*A study of current multilevel interconnect technologies for 90 nm nodes and beyond",* Fujitsu Scientific & Technical Journal, Vol. **38**(1), pp.13-21. 2002.
[8] S. R. Ohring, M.I., M. J. Kumar, and S. K. Das. "*Generalized fat trees*", in *IEEE Symposium on Parallel and Distributed Processing.* Los Alamitos, CA: IEEE. 1995.
[9] Masafumi TSUTSUI and Masahiro ASADA, "Dependence of Drain Current on Gate Oxide Thickness of P-Type Vertical PtSi Schottky Source/Drain Metal Oxide Semiconductor Field-Effect Transistors", Jpn. J. Appl. Phys., Vol.41, pp. 54-58, 2002.
[10] C. Wang, John P. Snyder, and J. R. Tucker, "Sub-40 nm PtSi Schottky Source/Drain Metal-Oxide-Semiconductor Field-Effect Transistors", Appl. Phys. Lett., Vol. 74, pp. 1174-1176, 1999.