

# NON-ROBOTIC FABRICATION OF PACKAGED MICROSYSTEMS BY SHAPE-AND-SOLDER-DIRECTED SELF-ASSEMBLY

*Wei Zheng, Jae-hoon Chung and Heiko O. Jacobs*  
Department of Electrical and Computer Engineering  
University of Minnesota, Minneapolis, Minnesota, USA

## ABSTRACT

The non-robotic fabrication of packaged microsystems that contain non-identical parts has been accomplished by a directed self-assembly process. The self-assembly process uses geometrical shape recognition to identify different components and subsequent bond formation between liquid solder and metal-coated areas to form mechanical and electrical connections. We applied this concept of shape recognition and subsequent formation of contacts to assemble and package microsystems that contained three building blocks: a silicon carrier, a semiconductor device segment, and a glass encapsulation unit. As semiconductor device segments, we tested 200 micrometer sized light-emitting diodes. The microsystems self-assembled by sequentially adding parts to the assembly solution. Six hundred AlGaInP/GaAs light-emitting diode segments self-assembled onto device carriers in 2 minutes without defects. Encapsulation units self-assembled onto the LED-carrier assemblies to form a three-dimensional circuit path to operate the final device.

## 1. INTRODUCTION

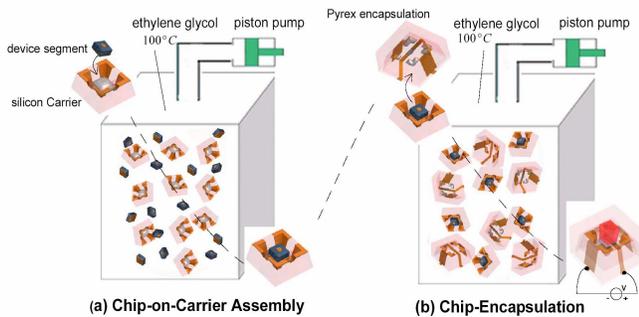
Traditional manufacturing technologies that focused on assembly include serial pick-and-place, serial wire-bonding, serial packaging, and parallel wafer-to-wafer transfer [1]. As components become smaller, following the trend in miniaturization, conventional robotic methods and assembly lines fail because of the difficulty in building machines that can economically manipulate components in three dimensions that are only micrometers in size. Methods of directed self-assembly have the potential to overcome the limitations of robotic assembly and enable multicomponent microsystems manufacturing in three-dimensions [2-7]. Previous demonstrations of directed self-assembly to generate functional electrical microsystems include a fluidic method that position electronic devices on planar surfaces using shape recognition and gravitational forces [2], liquid-solder based self-assemblies that use the surface-tension between pairs of molten solder drops to assemble three-dimensional electrical networks, ring oscillators, and shift registers [3], capillary force directed self-assembly that uses hydrophobic-hydrophilic surfaces patterns and photo curable polymers to integrate micro-optical components, micromirrors and micropump elements on silicon substrates [4-6], and solder-receptor directed self-assembly where metal contacts on segmented semiconductor devices bind to liquid-solder-based-receptors on planar and non-planar surfaces [7].

One of the grand challenges in self-assembly is the realization of heterogeneous systems [8]. While current methods allow the positioning of a large number of identical components in a massively parallel manner, systems that consist of more than one repeating unit are difficult to achieve. For example, in shape-directed fluidic self-assembly, small device components settle by mistake into the holes designed to match the shape of larger components. Similarly, in surface-tension driven self-assembly, the binding sites designed for one component will almost always find an overlap with the receptor for a different component. In general terms, the current procedures provide an insufficient power of recognition to correctly assemble heterogeneous systems.

Here we describe a directed self-assembly process for the fabrication of three-dimensional microsystems that contain non-identical parts. The self-assembly process uses geometrical shape recognition to identify different components and subsequent bond formation between liquid solder and metal-coated areas to form mechanical and electrical connections. This combination provides a greater flexibility in the design of self-assembling systems with minimum defects. Another new element is the use of sequential self-assembly [9]. We believe that it will never be possible to assemble complex heterogeneous systems in a single self-assembly step. Instead we suggest to use sequential self-assembly. Our idea is borrowed from chemical and biological systems that build heterodimers, trimers, and higher aggregates by sequentially adding different molecules. The concept is similar in the sense that every component type can be seen as a different molecule. In our case, however, each component provides a different functionality. We apply this combination of existing and new concepts to assemble and package microsystems that contain 200  $\mu\text{m}$  sized optoelectronic devices. The components are  $\sim 15$  times smaller than those used in current robotic assembly lines [10], 40 times smaller than those of previous solder-based self-assemblies [3], and about the same as those assembled by shape-directed fluidic procedures on planar surfaces [2]. Each microsystem is formed using three non-identical components: a semiconductor device segment, a carrier, and an encapsulation unit. We have demonstrated three dimensional assemblies, the registration and electrical contact formation, and the establishment of a three-dimensional circuit path that enables surface mount device operation.

## 2. METHODS

The experimental strategy to assemble and package microsystems is illustrated in Figure 1. Each microsystem consists of three parts—a semiconductor device segment, a silicon carrier, and a Pyrex encapsulation unit—with distinct complimentary three-dimensional shapes, circuits, solder patterns, and copper metallization. The assembly is formed by a two-step sequence of self-assembly and packaging: (i) chip-on-carrier assembly and (ii) chip-encapsulation. The device segments used in this study are unpackaged cubic AlGaInP/GaAs light-emitting diodes (LEDs) with a side length of 200  $\mu\text{m}$ . The LED has two contacts: a small circular anode on the front, and a large square cathode covering the back. Each silicon carrier provided a target site—a 200  $\mu\text{m}$  deep tapered opening—that fits one single LED chip at a time. We integrated a binding site—a 200  $\mu\text{m}$  wide square shaped solder-coated area—in the center of the opening for the attachment of the LED chips. During the first self-assembly step, the surface of the liquid solder wets and binds to the gold-coated cathode on the back side of the LEDs. The minimization of the free surface area of the liquid solder drives the assembly into a stable, aligned position. The solder also provides the electrical connection to operate the device and the mechanical bond required to hold the assembly together.



*Figure 1: Fabrication strategy to assemble and package microsystems by shape-and-solder directed self-assembly. Chip-on-carrier assembly (a) and chip-encapsulation (b) are performed in an ethylene glycol solution at a temperature of 100 °C where the solder is liquid*

Each encapsulation unit carried a 200  $\mu\text{m}$  deep tapered opening in the center to recognize the assembled LEDs during the encapsulation process and to distinguish between encapsulation units themselves. Each opening exposed five solder-coated areas to wet and bind to correspondingly-shaped gold-coated areas on the LED and carrier during the second self-assembly step.

In this study all self-assembly steps were performed in ethylene glycol at a temperature of 100 °C where the solder (Y-LMA-117, Small Parts, Miami Lakes, Florida) was molten. The ethylene glycol solution was made slightly acidic (pH 2.5) with sulfuric acid to remove metal oxides from the surface of the solder and copper binding sites. We built a turbulent pulsating flow system to provide a strong and reproducible form of agitation. We also tested agitation of the components by shaking the vial manually; however, the results were less reproducible. The turbulent pulsating

flow was created using a piston pump (PM6014, Fluid Metering, Inc., Syosset, New York) that expels and retracts liquid through a 2 mm diameter nozzle that is submerged in the assembly solution. The amount and frequency of liquid that is cycled back and forth can be adjusted between 1-1.5 mL, and 0-10 Hz, respectively. The assembly was carried out inside a rectangular glass container (12 mm on each side and 45 mm high) filled with 4.5 mL of ethylene glycol at a temperature of 100 °C.

### 3. FABRICATION

The procedures to fabricate the silicon carriers, Pyrex encapsulation unit, and patterned solder drops on the three-dimensionally-shaped units are described in Figure 2.

#### Fabrication of the silicon carriers

A p-type 280  $\mu\text{m}$ -thick Si wafer (Virginia Semiconductor, Fredericksburg, Virginia) was coated with LPCVD nitride to form a 100 nm thick layer. The substrate was primed with hexamethyldisilazane and spin-coated with photoresist (Microposit 1813, Shipley, Phoenix, Arizona). After a soft-bake at 105°C for 1 minute, the substrate was exposed to UV light through a dark field mask. The photoresist was developed in 1 MIF-351: 5 H<sub>2</sub>O developer for about 15 seconds. The exposed nitride area was etched in STS etcher for 2 minutes; the exposed silicon area was etched in KOH (45%) at 80 °C for 4.5 hours resulting in a 200  $\mu\text{m}$  deep tapered opening. After etching, the silicon wafer was coated with 25 nm Ti and 800 nm copper using e-beam evaporator. Shipley Eagle 2100 photoresist was electroplated on the wafer using a DC voltage (50V) for 30 seconds at 35°C. After a soft-bake at 80 °C for 2 minutes, the substrate was exposed to UV light through the second mask for 60 seconds. The Eagle 2100 photoresist was developed in 1 Eagle 2005 developer: 24 H<sub>2</sub>O at 38 °C for 2 minutes. The exposed copper was etched in an aqueous ferric chloride solution (1.4 g of FeCl<sub>3</sub> per milliliter of H<sub>2</sub>O, pH 1.3) and the Ti was etched in 10:1 buffered oxide etchant. After removing the Eagle 2100 photoresist in acetone, another layer of Eagle 2100 photoresist was electroplated using a DC voltage (50V) for 30 seconds at 35°C to form the solder-coated receptors. The photoresist was exposed and developed using the same conditions as described before. The exposed copper squares were coated with solder by immersing the substrate into a solder bath. Finally, the wafer was diced using an automated dicing saw to obtain the silicon carriers. The remaining photoresist was removed in acetone to expose the binding sites.

#### Fabrication of Pyrex encapsulation units

A 500  $\mu\text{m}$ -thick Corning 7740 wafer (Universitywafer, Boston, Massachusetts) was coated with 25 nm Cr and 250 nm Au using an e-beam evaporator. The substrate was primed with hexamethyldisilazane, and spin-coated with photoresist (Microposit 1813, Shipley, Phoenix, Arizona). After a soft-bake at 105 °C for 1 minute, the substrate was

exposed to UV light through a dark field mask. The photoresist was developed in MIF-351 1:5 developer for about 15 seconds. The metal layers were etched using 4 KI: 1 I<sub>2</sub>: 40 H<sub>2</sub>O for Au and 1 HCl: 1 Glycerol: 3 H<sub>2</sub>O for Cr. The exposed glass area was etched in 20 HF (49%): 14 NH<sub>3</sub> (69%): 66 H<sub>2</sub>O for 5 hours. After removing the metal layer, the glass wafer was coated with 25 nm Ti and 800 nm copper using an e-beam evaporator. The Shipley Eagle 2100 photoresist was electroplated on the wafer using a DC voltage (50V) for 30 seconds at 35 °C. After a soft-bake at 80 °C for 2 minutes, the substrate was exposed to UV light through the second mask for 60 seconds. The Eagle 2100 photoresist was developed in 1 Eagle 2005 developer: 24 H<sub>2</sub>O at 38 °C for 2 minutes. The exposed copper was etched in an aqueous ferric chloride solution (1.4 g of FeCl<sub>3</sub> per milliliter of H<sub>2</sub>O, pH 1.3) and the Ti was etched in 10:1 buffered oxide etchant. After removing the Eagle 2100 photoresist in acetone, the Shipley 1805 photoresist was spun on the substrate and patterned to expose the copper area for solder wetting. The opening area was coated with the low-melting point solder by immersing the substrate into a solder bath. Finally, the wafer was diced to obtain the Pyrex encapsulation units. The remaining photoresist was removed in acetone to expose the binding sites.

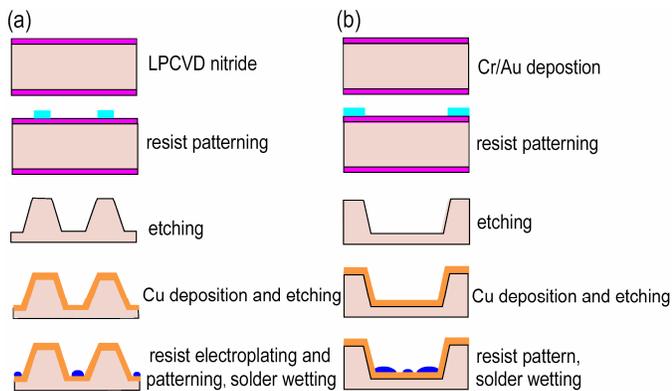


Figure 2: Micromachining procedure of the self-assembly components. (a) Fabrication of the silicon carriers; (b) Fabrication of Pyrex encapsulation units.

#### 4. RESULTS AND DISCUSSIONS

Figure 3 illustrates the experimental realization of the two-step: chip-on-carrier assembly and chip-encapsulation process. For the chip-on-carrier assembly (Fig. 3a), we added 3000 LED chips and 600 carrier units into the heated assembly solution and agitated the pieces using the turbulent liquid flow. We obtained a yield of 100% — that is, all 600 carriers had captured an LED device segment — in 2 minutes. To prepare for the encapsulation process (Fig. 3b), we removed the excess LEDs by filtration through a 500- $\mu$ m mesh filter and added 200 encapsulation units to the assembly container. The excess LEDs were reused in later experiments. The yield of the encapsulation process was 97%, which means that 3% of the devices did not function as expected. We reproduced the self-encapsulation process

several times and found that variations in the height of up to  $\sim 20$   $\mu$ m, and lateral misfits between the anode of the LEDs and the top electrode of up to  $\sim 40$   $\mu$ m, were tolerated; beyond those limits the devices would not function. Small deviations were compensated by the reflow of solder and the repositioning of the LED, carrier, and encapsulation units. Deviations from the permissible range of sizes and positions resulted from variations in the size of the LEDs ( $\sim 30$   $\mu$ m), and shape, thickness, and location of the solder-coated areas. In some cases we also found solder-based areas on the components that were only partially coated with solder, and components with partially detached metal areas as a source of defects. The overall yield of the process is currently 97% and can be increased by further removing the imperfection in the manufacturing of the components. These defects are not inherent to the self-assembly process itself, but were caused by imperfections in the manufacturing of the components.

Besides the AlGaInP/GaAs LED segments, we successfully assembled and packaged two terminal blue AlGaIn/GaN LEDs. The contacts on the blue LEDs were located on the same side of the  $375 \times 330$   $\mu$ m wide and 80  $\mu$ m tall device segments. The dimensions of the final assembly were 800  $\mu$ m x 800  $\mu$ m x 500  $\mu$ m. The procedure and yield ( $\sim 97\%$ ) of the assembly and packaging of these devices was similar to that described with the red emitting LED segments. We tested the functionality by hand mounting the devices on a printed circuit board as shown in Figure 4.

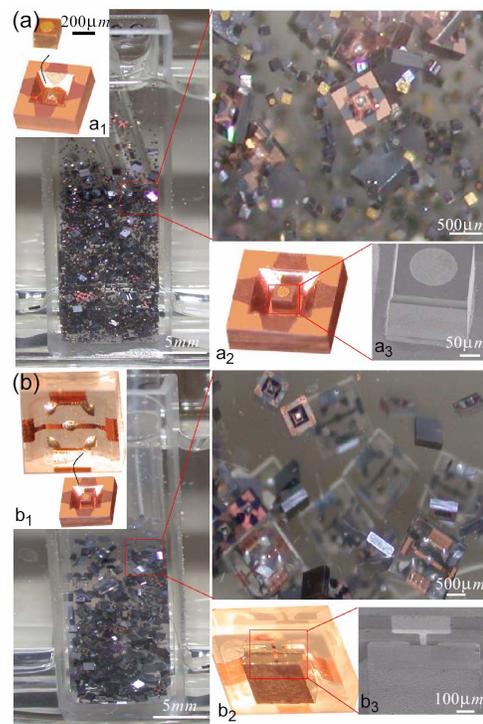


Figure 3: Experimental realization of LED chips that were assembled and packaged. The insets show device components before (*a*<sub>1</sub>, *b*<sub>1</sub>) and after (*a*<sub>2</sub>, *b*<sub>2</sub>) each assembly step. The scanning electron micrographs (*a*<sub>3</sub>, *b*<sub>3</sub>) illustrate the alignment between components.

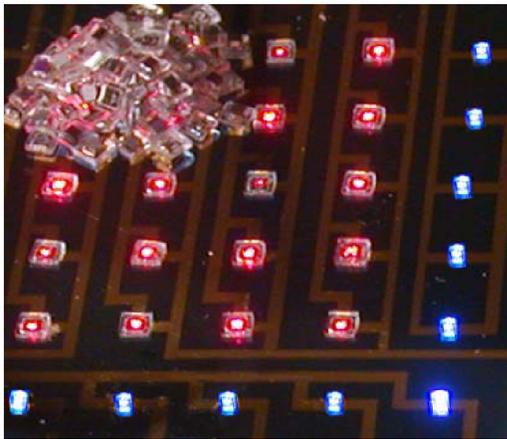


Figure 4: Testing of LED chips that have been assembled and packaged.

Defects inherent to self-assembly processes are most commonly related to local energy minima in the space of possible conformations or to an insufficient overall energy minimum representing a stable assembly under agitation. We were able to remove local energy minima and associated defects completely by introducing and optimizing the complimentary shapes. First carrier designs, for example, had truncated pyramidal openings that were three times as large as the LED device segments. As a result we found two device segments that assembled on a single receptor. We have removed such defects by reducing the size of the opening on the device carrier. We also optimized the overall energy minima by changing the size and shape of the solder-coated areas and the metallic binding sites on the device components. Early designs for the encapsulation units could not sustain high levels of agitation; defects were created by component impaction removing previously assembled LEDs and encapsulation units from the carriers. Fast and stable assemblies were accomplished by increasing the binding sites to cover more than 40% of the surface. The symmetry of the design influences the speed of the self-assembly process as well. The presented design has a four-fold symmetry and assembled faster than designs that presented a two-fold symmetry

## 5. CONCLUSIONS

We have demonstrated the self-assembly and packaging of microsystems using a directed three-dimensional self-assembly technique that combines existing concepts of geometrical shape recognition and site specific wetting and binding involving liquid solder with a new concept of sequential self-assembly. The technique is tailored to enable the realization of heterogeneous three-dimensional microsystems that contain non-identical parts, and of connecting them electrically, where the shape provides the ability to recognize different component, where the solder provides both the driving force, the electrical, and mechanical connections, and where the sequence provides the ability to build complex systems.

Assembling and packaging of light emitting diodes is conceptually interesting as it provides an example that has historically been realized with robotic assembly lines and wire bonders. It should be possible to extend this concept to systems where sensors or actuation elements are added to the assembly sequence. The use of non-conventional lithographic methods where the components can be patterned on all faces would provide even greater flexibility in the creation of three-dimensional systems that cannot be fabricated otherwise.

## 6. ACKNOWLEDGEMENTS

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