Self-Assembly and Self-Tiling: Integrating Active Dies Across Length Scales on Flexible Substrates

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***Abstract*—This paper reports on recent progress in the field of directed self-assembly, wherein discrete inorganic semiconductor device components are assembled on flexible substrates, and compares these results with prior work. The research aims to develop self-assembly-based chiplet assembly processes that can extend minimal die sizes and throughput beyond what is currently possible with robotic pick and place methods. This manuscript concentrates on self-assembly that is driven by the reduction of surface free energy between liquid solder-coated areas on a substrate and metal-coated contacts on semiconductor dies that act as binding sites. Scaling prior results to sub-100 micrometer-sized components has required a transition to a new self-assembly platform. Specifically, recent work has moved from a drum delivery concept to a new scheme that uses a stepwise reduction of interfacial free energy at a triple interface between oil, water, and a penetrating solder-patterned substrate to introduce components. Finally, this paper also discusses design rules to produce highly periodic "self-tiled" domains on rigid, flexible, and curved substrates. We describe discrete, self-tiled, and microconcentrator-augmented solar cell modules as applications that are fault tolerant and reduce the amount of Si material used by up to a factor of 22 when compared to conventional cells. [2011-0143]**

***Index Terms*—Flexible electronics, self-assembly, semiconductor device packaging, solar power generation.**

I. Introduction

PROGRESS in the fields of microelectronics and microoptics has traditionally been measured by the level of overall miniaturization: The construction of modern man-made artifacts such as cell phones and computers relies on robotic assembly lines that place, package, and interconnect a variety of increasingly small devices to build miniaturized and advanced products [1]. At the same time, the emerging fields of macro- and printable electronics have a different set of goals, which draw attention to new manufacturing methods that enable large-area integration, preferably on flexible, curved, and low-temperature plastic substrates. The key to the realization of both of these approaches is the ability to integrate/assemble components in 2-D/3-D as well as link/interconnect the components to transport materials, energy, and information. The difficulty is not the small parts' fabrication, but rather, their assembly and interconnect formation.

For components with dimensions less than 100 μm, adhesive capillary forces often dominate gravitational forces, making it difficult to release dies from a robotic manipulator, the tool typically used in modern system integration [2]. Other current manufacturing processes used to deliver active materials to target substrates include inkjet printing, parallel transfer, and self-assembly. Inkjet printing is most suited to producing low-performance organic semiconductors and hybrid organic/inorganic structures,[1] while parallel transfer [3]–[6] and self-assembly techniques [7]–[11] target the integration of higher performance inorganic devices on flexible, low-temperature substrates in a massively parallel fashion. Applications include flexible [12] and curved [10] displays [5], curved focal plane arrays [4], oscillators [5], RFID tags [13], vertical laser routing and RF microelectromechanical systems [14], living cell transportation [15], and solar cells [6]. ZnO [16], GaAs [9], [17], InP [18], GaN [19], [20], and Si [4], [5], [10], [21], [22] have been incorporated for these purposes. Transfer techniques, when compared to directed self-assembly methods, use a donor substrate/wafer and maintain its orientation and integration density. This is in stark contrast to directed self-assembly, which can redistribute components over large areas and order unorganized parts, regardless of source. For example, a container full of semiconductor dies/chiplets can be redistributed and assembled at precise locations on a substrate, at any desired pitch or required functional density, using methods of self-assembly [23]. Recent demonstrations of processes that can self-assemble nanometer to millimeter-sized components include: shape-directed methods that position electronic devices on planar surfaces using shape recognition and gravitational forces [8], [15], [24], [25], liquid-solder-based self-assembly that uses the surface tension between pairs of molten solder drops to assemble functional systems [10], [26]–[30], capillary force-directed self-assembly that uses hydrophilic/hydrophobic surface patterns and photocurable

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[1]To replace a silicon transistor that switches a current of a given magnitude with an organic pentacene transistor requires roughly $[(\rho_{\mathrm{Pent}}/\rho_{\mathrm{Si}})^3$, typ. $>$ 1000] more material occupying $[(\rho_{\mathrm{Pent}}/\rho_{\mathrm{Si}})$, typ. $> 100]$ more area. This estimate considers transistors with channel length l, width w, height h, and resistivity ρ whereby the proportions are $l = n \times w = k \times h$. Considering Si and pentacene, the resistance becomes $R_{\mathrm{Si}} = \rho_{\mathrm{Si}} \times l_{\mathrm{Si}}/[(l_{\mathrm{Si}}/n) \times (l_{\mathrm{Si}}/k)]$ and RPent $= \rho_{\mathrm{Pent}} \times l_{\mathrm{Pent}}/[(l_{\mathrm{Pent}}/n) \times (l_{\mathrm{Pent}}/k)]$ To handle the same current requires the same resistance which means that $l_{\mathrm{Si}}/l_{\mathrm{Pent}} = \rho_{\mathrm{Pent}}/\rho_{\mathrm{Si}}$. The required volume and material for the same task increases with $(\rho_{\mathrm{Pent}}/\rho_{\mathrm{Si}})$.

polymers to integrate micro-optical components, micromirrors, carbon nanotubes, ZnO nanowires, and semiconductor chips on silicon substrates [14], [31]–[35], and sequential shape-and-solder-directed self-assembly that uses shapes as chaperones to prevent defects and to direct site-specific binding with liquid solder. The sequential shape-and-solder-directed self-assembly process has been applied to flip-chip assembly with unique contact pad registration [11], as well as the packaging of light emitting diodes [9], [19], [36], [37] and transponders that can be interrogated remotely [37]. Comparing more recent concepts [11], [38], [39] with the pioneering work by Yeh and Smith [8], [24], there are a number of fundamental advances: Recent methods do not require the use of trapezoidal chips to prevent upside down assembly or uncommon asymmetric L- or T-shaped chip designs to gain angular orientation control. Instead, they use simple shapes and/or openings in combination with solder-coated areas to enable assembly in 2-D or 3-D, including flip-chip assembly with unique orientation and contact pad registration [11]. Some designs use openings that are bigger than their components, in such a manner that the openings act as chaperones where the solder directed self-assembly process takes place [9], [37]. It is the solder, however, that enables the assembly of parts into aligned, stable positions. The driving force is the reduction of the solder interfacial free energy, as opposed to gravity. Recent studies have also overcome the difficulty in assembling more than one component type through sequential methods that rely on either the activation of selected receptors [40]–[43] or differently sized openings [9], [11], [19].

While a number of self-assembly applications have been demonstrated, scaling to smaller dimensions remains an increasingly difficult challenge. Progress toward assembling smaller objects has been made by Stauth *et al.* [7], who successfully assembled 100 μm-sized objects, which were three times smaller than previously reported results. The assembly of still smaller chips cannot be accomplished using a linear extension of the above methods, since highly scaled components tend to stay in suspension during agitation, instead of settling down on a receptor. While the reduction of surface free energy will continue to drive assembly at small scales, further extension of scaling requires self-assembly system designs that eliminate the dependence on gravity and sedimentation as a component transport/introduction mechanism. This manuscript discusses a potential solution to the transportation of sub-100 μm objects problem, which invokes a liquid-liquid-solid interface to define a progressing linear front where self-assembly takes place in a conveyor belt-like fashion. Progress using this new type of transport mechanism, which confines components into a 2-D layer before transferring them onto a substrate, has recently been made in two independent studies [44]–[46]. In our particular design [44], as described here, the component delivery and assembly process has been engineered to include a stepwise reduction of interfacial free energy, providing an energy cascade to 1) transport, 2) pre-orient, and 3) assemble microscopic components at predefined surface areas. The process enables the assembly of even smaller components than were previously possible and achieves a higher throughput; 62 thousand components were assembled and electrically connected in 3 min. The approach was tested using 3 μm–1000 μm sized

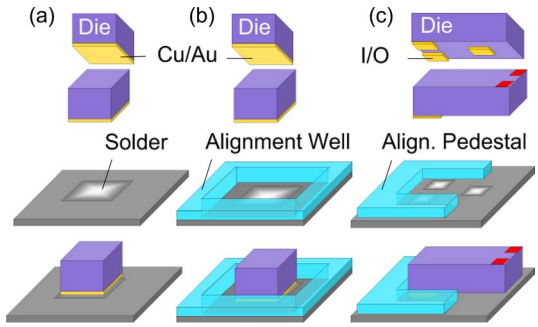


Fig. 1. Self-assembly of dies using (a) solder-based alignment alone, (b) alignment wells, and (c) alignment pedestals that allow for both single-angle orientation and flip-chip assembly with multiple I/O connectivity.

chiplets made of SU-8 and Si. Assembly yields ranged between 98% and 100%. In addition to the assembly of one component per receptor site, this report will also discuss design rules that enable the assembly of multiple dies per receptor domain.

Receptors are tested that have room for more than one component. This approach, in the case of increasingly large domains, is then best described as a self-tiling method. We successfully demonstrated the assembly of tiles of different sizes, shapes, and materials into closely packed, predetermined regions on a receiving substrate [45]. The largest domains contain over 6500 tiles that are close packed with less than 3% vacancies.

The first testbed application that will be discussed is the fabrication of a segmented flexible monocrystalline silicon solar cell using silicon dies that are 20 μm thin and reduce the required use of Si by a factor of 10 when compared to conventional 300 μm thick and rigid monocrystalline solar cells. Also, demonstrated are similar self-tiled flexible solar cells, and finally, a module combining the resulting self-tiled structure with an acrylic lenticular microconcentrator array (Edmund Optics), achieving a total Si material reduction factor of $\sim$22.

II. Results and Discussion

A. Solder-Directed Fluidic Self-Assembly

Fig. 1 shows the basic concepts of solder-directed self-assembly, introducing alignment pedestals and receptor layouts with increasing complexity. In Fig. 1(a), the reduction of surface free energy causes a component that is introduced to a receptor to become adhered and aligned to the receptor dimensions. The approach Fig. 1(b) prevents assembly of more than one component type onto a single receptor at a docking site, while the layout in Fig. 1(c) enables flip-chip assembly with single-angle orientation and contact pad registration, forming multiple contacts to the device at a single docking site. Components can only attach to the solder-coated areas if a correct angular pre-orientation condition is met: components that arrive at the docking sites (each containing a receptor pad) with an angular orientation that deviates by more than $\pm 90^{\circ}$ from the desired orientation will not find a sufficient overlap between their binding sites and the solder-coated receptors, and will not attach. Components that arrive with the correct

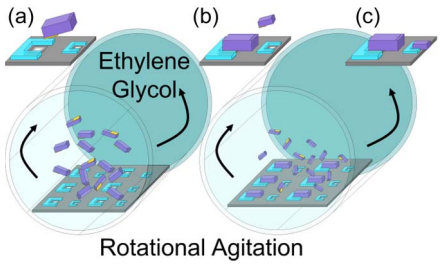


Fig. 2. Two-step component registration process for integrating multiple types of chiplets on a single substrate. Components are introduced to the substrate and assembled in a rotating vial that provides agitation and heat.

pre-orientation will be captured and aligned due to the reduction of the interfacial free energy, just as in (a).

B. Drum Assembly System

Fig. 2 shows a conventional drum assembly system [Fig. 2(a)] and a sequential self-assembly process [Fig. 2(a)–(c)] where different components are assembled flip-chip style with single-angle orientation in a two-step sequence. Component transport and mixing were provided by a modified mechanical shaker (BD-Clay Adams, Franklin Lakes, NJ) that both agitated and rotated the drum to introduce a tumbling motion of components across the surface. The drum is filled with ethylene glycol, which is maintained at 150 °C, so the solder remains molten. Ethylene glycol is used to accommodate higher melting point solder. We tested both low-(47 °C) and medium-(138 °C) melting-point (mp) solders (Y-LMA-117 and LMA-281, Small Parts, Miami Lakes, FL) that have been used in previous self-assembly experiments [10], [36], [47] and did not observe a notable difference between the two. The ethylene glycol solution was made acidic (pH ∼2.5) with hydrochloric acid to remove metal oxide from the surface of the solder drop; an oxide layer that—if sufficiently thick—blocks the wetting of the metal surface. This process, shown in Fig. 2, allows for multiple component types to be correctly assembled, but adds the complexity of requiring two-step assembly in combination with single-angle docking sites. Furthermore, unless multiple solders with differing melting points are used to activate the receptors, this system requires different-sized components for the first and second step as is illustrated.

This drum assembly system provides high assembly yields. We have tested the self-assembly of a number of different component types, including GaAlAs LEDs, Si, glass, and SU-8 blocks with different pad layouts using this method. Fig. 3 and Table I present a summary of the results. Fig. 3(a) shows ∼1560 silicon chiplets of size 300 μm × 300 μm × 400 μm that were assembled onto a flexible polyimide surface with 98% coverage. With ∼5000 components inside the vial, the assembly took about 90 s to reach steady state and was completed in 3 min. The lateral and angular precision was ∼15 μm and ∼3°, respectively, and limited by nonuniformity of the components that were fabricated using a dicing saw. Fig. 3(b) shows GaAs/GaAlAs light-emitting diodes that were assembled on a silicon substate. The insets show the LEDs in operation. Without alignment pedestals, two chiplets can occupy a single receptor at a docking site, which is considered a defect (Fig. 3(a), subset). This defect can be eliminated using alignment wells, as shown in Fig. 3(c). The entire assembly contained 360 interconnected LEDs, with side lengths of 280 μm. The chiplets assembled in four stable orientations: 0°, 90°, 180°, and 270°. It is possible, however, to remove the undesired angular orientations among these and achieve flip-chip assembly with unique angular orientation. Fig. 3(d) shows the results of a different experiment in which silicon components carrying alignment marks on their topsides were assembled into two-element docking sites. The component binding sites can only find an overlap with the receptors if they arrive at the

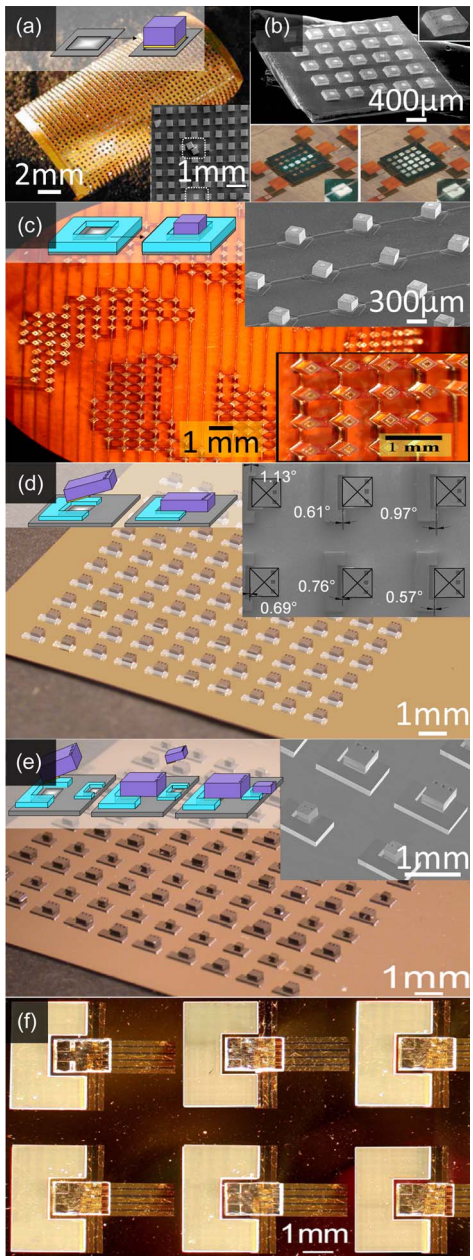
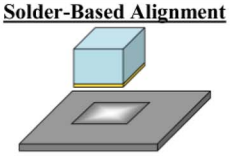
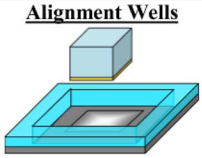
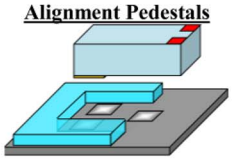
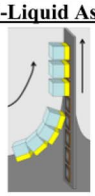
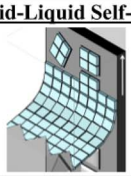


Fig. 3. Summary of self-assembly results using GaAlAs-LEDs, Si, Glass, and SU-8 blocks with varying docking site layouts, including solder-directed assembly of (a) silicon parts and (b) LEDs, (c) well assembly, (d) single-angle orientation assembly using "two-step" docking sites, (e), two-step contact pad registration, and (f) assembly of parts with multiple I/O connections.

TABLE I
SELF-ASSEMBLY APPROACH COMPARISON

Approach	(✓): Benefit (×): Disadvantage	Component Types	Demonstrated Metrics
Solder-Based Alignment 	✓ Defined up/down orientation ✓ Rapid introduction ✓ Very scalable ✓ Roll-to-roll compatible × Multiple components per receptor possible × Single I/O connection × Requires regular polygon-shaped components	• Suitable for regular polygon components (e.g. square, equilateral triangle) • Single I/O • Stable orientations 0°, 90°, 180°, 270°	• 1560 Si 300×300 µm chiplets • 98% yield • 3 min assembly time • ~15µm, ~3° precision
Alignment Wells 	✓ Simple design ✓ Single component per receptor ✓ Limited possible orientation angles ✓ Flexible substrates × Multiple stable angular orientations × Single I/O connection × Requires regular polygon-shaped components	• Suitable for regular polygon components (e.g. square, equilateral triangle) • Single I/O • Stable orientations 0°, 90°, 180°, 270°	• 360 GaAs/ GaAlAs 280×280 µm chiplets • 98% yield • 3 min assembly time • ~15µm, ~3° precision
Alignment Pedestals 	✓ Single possible component angle ✓ Single component per receptor ✓ Multiple I/O connections ✓ Non-regular polygon-shaped components allowed ✓ T or Δ shapes not required × Decreased introduction speed × Difficult to scale	• Allows sequential Assembly of differently sized components • Allows rectangular, non-square, components • Allows multiple I/O	• 100 Si 900×900 µm, 50 Si 900×900 µm, and 50 Si 500×500 µm chiplets • 98% yield • 3 min assembly time • 19µm, 0.8° precision
Liquid-Liquid Assembly 	✓ Scales to very small components ✓ Limited possible orientation angles ✓ Simple design ✓ Flexible substrates × Multiple components per receptor possible × Multiple stable angular orientations × Single I/O connection × Requires regular polygon-shaped components	• Suitable for regular polygon components (e.g. square, equilateral triangle) • Single I/O • Stable orientations 0°, 90°, 180°, 270°	• 400 SU-8 20×20 µm, 400 Si 60×60 µm chiplets • 99.3% yield • 1 min assembly time • 0.9µm, 0.14° precision • 3µm minimum chip size
Liquid-Liquid Self-tiling 	✓ Scales to very small components ✓ Very high surface coverage ✓ Simple design ✓ Flexible substrates ✓ Simple lattice design rules × Requires regular polygon-shaped components	• Suitable for regular polygon tiles (e.g. square, equilateral triangle) • Single I/O	• 6500 SU-8 20×20 µm, 4600 Si 60×60 µm tiles • >97% yield • 1 min assembly time • 1.1µm, 0.3° precision • 3µm minimum chip size

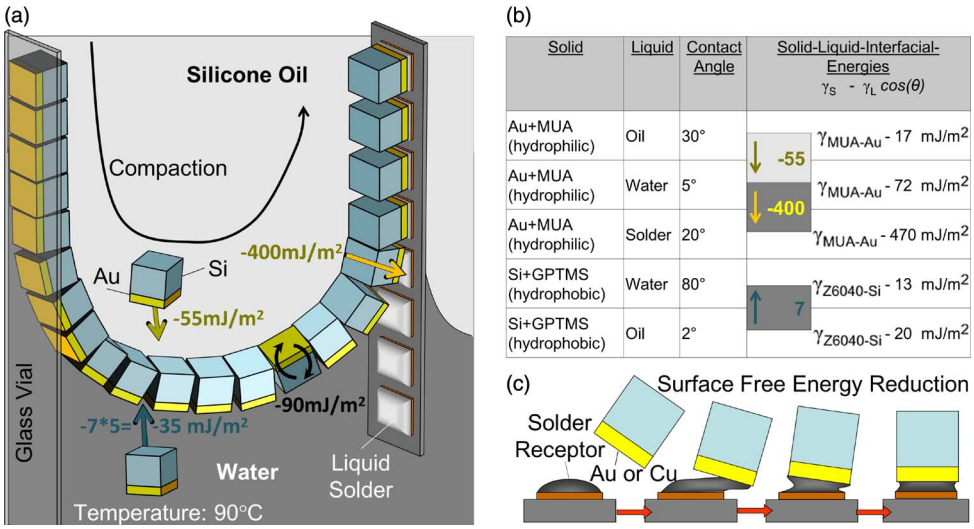
area with the single correct pre-orientation. As a result, components can only assemble with one primary angular orientation. The angular standard deviation was $\sim 0.3^\circ$ in this example with alignment pedestals that were fabricated using 300 μm tall SU-8.

Fig. 3(e) shows the results of sequential assembly with a 10×10 array that contains 900 μm- and 500 μm-sized dies that have been assembled using a two-step docking site self-assembly sequence with 300 μm tall Si pedestals, where the large components are filled in first and the smaller components are filled in second, as previously described in Fig. 2. This general idea can be developed further such that solder-directed self-assembly can be engineered to enable flip-chip assembly with contact pad registration, as shown in Fig. 3(f), which shows flip-chip assembled 2 mm $\times$ 1 mm $\times$ 1 mm glass blocks. The blocks assembled with unique orientation and multiple mechanical connections. Of the seven solder-coated receptors, five were electrically connected to external contact pads, and two were left isolated. All connections are visible through the glass blocks from the top.

The drum assembly system is reliable when the components fall into a 100 μm to 5000 μm size window. We anticipate that this window can be extended to smaller components, but tests with sub-100 μm components have not yet been successful in delivering the previous assembly yield rates, which exceeded 98%.

There are two important parameters that need to be considered when scaling the components.

1) Solder-directed assembly is sensitive to surface oxides that reduce the surface energy available to drive self-assembly and self-alignment. As a result, all metal surfaces, including the solder, need to be free of surface oxide. This is achieved by reducing the pH of the assembly solution to be slightly acidic, in this case, pH 2.0. Re-oxidation and oxide removal is typically a continuous process that results in volume loss and a change in the solder composition over time. This is the case for all self-assembly methods involving liquid solder as a driving mechanism, and it is therefore important to limit the total assembly time. This becomes particularly the case when using highly scaled components (< 100 μm). The solder volume is two to three orders of magnitude smaller in this case than for 300 μm components.



Solid	Liquid	Contact Angle	Solid-Liquid-Interfacial-Energies $\gamma_S - \gamma_L \cos(\theta)$
Au+MUA (hydrophilic)	Oil	30°	γ_{MUA-Au} - 17 mJ/m²
			-55
Au+MUA (hydrophilic)	Water	5°	γ_{MUA-Au} - 72 mJ/m²
			-400
Au+MUA (hydrophilic)	Solder	20°	γ_{MUA-Au} - 470 mJ/m²
Si+GPTMS (hydrophobic)	Water	80°	$\gamma_{Z6040-Si}$ - 13 mJ/m²
			7
Si+GPTMS (hydrophobic)	Oil	2°	$\gamma_{Z6040-Si}$ - 20 mJ/m²

Fig. 4. (a) Procedure of surface tension-directed self-assembly at a liquid-liquid-solid interface employing an energy cascade to (i) move components from a suspension to the interface (55 mJ/m^2), (ii) pre-orient the components within the interface to face in the right direction (90 mJ/m^2), and (iii) assemble the components on molten solder through dipping (400 mJ/m^2). The illustration depicts the situation for an oil-water interface and chiplets made out of Si (SU-8 is detailed in main body), which carry an Au contact on one face. (b) Depicted Au and Si surfaces are treated using hydrophilic MUA and hydrophobic GPTMS functional groups and yield the tabulated measured contact angles, calculated solid-liquid interfacial energies, and energy differences (gray boxes to the right) required to drive the assembly. The available area and curved shape of the interface cause the components to form a closely packed 2-D sheet. Upward motion of substrate yields a dynamic contact angle where the receding water layer becomes sufficiently thin for the gold to contact the solder. Patterned assembly on solder is favored by 400 mJ/m^2 within this layer. (c) At this point, the reduction of surface free energy causes the components to become well aligned.

2) Secondly, the assembly challenges at the sub-100 μm scale are compounded by the fact that highly scaled components (< 100 μm) stay suspended in solution under agitation, instead of settling onto the receptors. In other words, the use of gravity and sedimentation to transport the components to the surface in our drum design becomes less effective as the components become smaller, prolonging the assembly time. It is too early to make a definite judgment regarding the scaling limits within the drum design, but these points will have to be considered. Despite this known challenge, drum assembly provides the highest yields and self-alignment capabilities of the self-assembly methods we have tested so far. This continues to encourage the use of surface tension-driven self-assembly, since the liquid solder provides a very strong driving force.

C. Self-Assembly at a Triple Interface

A possible solution to the scaling challenge may be found in methods that assist in the transportation of highly scaled components to docking sites, eliminating the dependence on gravity and sedimentation as a transport mechanism. A first step in this direction is shown in Fig. 4.

The depicted strategy introduces a delivery and assembly concept that no longer takes place in a rotating vial/drum. Instead, the self-assembly of dies takes place at a triple liquid-liquid-solid interface. The process [Fig. 4(a)] uses a stepwise reduction of the interfacial energy to 1) move components from a suspension to the interface (55 mJ/m^2); 2) pre-orient the components within the interface to face in the right direction (90 mJ/m^2); and 3) assemble the components on molten solder, through dipping (400 mJ/m^2). To achieve this energy cascade, it is necessary to correctly choose and/or adjust the surface energies. We tested a silicone oil-water interface and components made of SU-8 and silicon (20 μm wide, 20 μm deep, 10 μm thick and 60 μm wide, 60 μm deep, 20 μm thick, respectively) with a gold-coated contact on a single face. The gold surface was treated with a mercaptoundecanoic acid (MUA) self-assembled monolayer (SAM) in a 10-mM (ethanol) solution for 15 min to render it hydrophilic, while the silicon faces were treated to become hydrophobic using 3-glycidoxypropyltrimethoxysilane (GPTMS, Dow Corning Z-6040) by soaking with 200-mM GPTMS in ethanol for 15 min followed by a dehydration bake at 115°C for 5 min. The SU-8 surface was hydrophobic and needed no adjustments. These treatments yield the measured tabulated [Fig. 4(b)] contact angles and interfacial energies between the solids and liquids as determined using Young's equation $\gamma_{s,l} = \gamma_s - \gamma_l \cos(\theta_{s,l})$ [48] where γ_s (unknown) represents the surface energy of the solids, γ_l (known) is the surface tension of the liquid, and $\theta_{s,l}$ is the measured contact angle (known). The surface tension of water, silicone oil, and solder (Y-LMA-117, mp. 47 °C, Small Parts, Miami Lakes, Florida) are 72, 20, $\sim$500 mJ/m^2, respectively, at a temperature of 95°C where the solder is molten. The surface energies of the solids γ_s are not needed, as this parameter cancels out when computing the tabulated energy differences. For example, considering the illustrated cubic component, the transition from being immersed in oil to the interface is favored because the hydrophilic gold surface prefers to be in contact with water instead of the oil; transfer to the liquid-liquid interface is favored by $55\ \text{mJ/m}^2 = \gamma_{\text{Au,water}} - \gamma_{\text{Au,oil}} = \gamma_{\text{oil}} \cos(\theta_{\text{Au,oil}}) - \gamma_{\text{water}} \cos(\theta_{\text{Au,water}})$. The components are confined to this interface since they face a $35\ \text{mJ/m}^2 = (\gamma_{\text{Si,oil}} - \gamma_{\text{Si,water}}) \times 5 = (\gamma_{\text{water}} \cos(\theta_{\text{Si,water}}) - \gamma_{\text{oil}} \cos(\theta_{\text{Si,oil}})) \times 5$ energy barrier

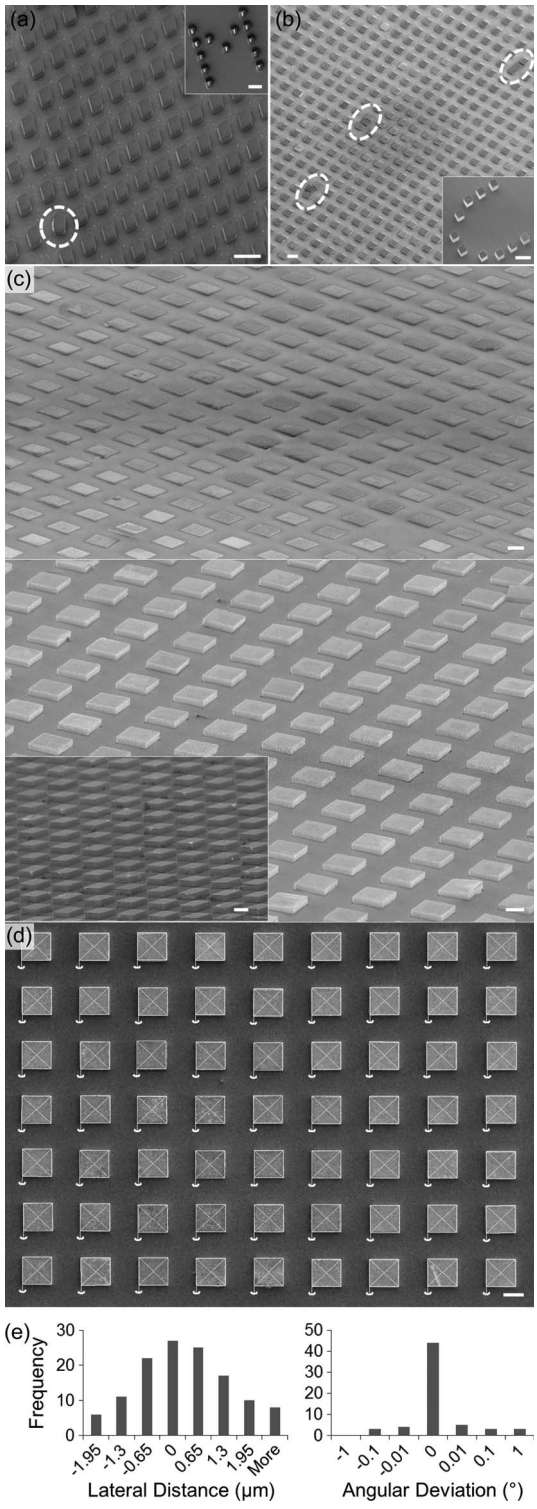


Fig. 5. Scanning electron micrographs (SEMs) of (a) SU-8 (20 μm side length) and (b, c, d) Si chiplets (20 μm and 60 μm side length) that have been assembled in regular arrays and arbitrary text patterns (insets) with example defects highlighted. The overlaid CAD guides visible (d, white lines) are used to measure variations in the center-to-center distance and angular-orientation. (e) Histogram of measured variations. 40 μm scale bars.

preventing them from completely entering the water, because the 5 hydrophobic Si sides prefer to remain in contact with oil rather than water. It would require the sum of 90 mJ/m^2 for a cube to be oriented upside down at the interface. Consequently, the components are introduced to the solder with the correct orientation, whereby the gold side faces the solder with a water layer in between. Solder has a higher affinity for wetting the gold contact than water, and attachment (assembly) is favored by 400 mJ/m^2.

The actual transfer and self-assembly on the substrate occurs as the sample is pulled upward through the interface [Fig. 4(a)]. Upward motion at a typical speed of 30 mm/s reduces the contact angle, forming a receding water layer that becomes sufficiently thin for the gold to contact the solder. At this point, the reduction of surface free energy leads the components to assemble, as shown in Fig. 4(c). The resulting stable orientations are 0°, 90 °, 180°, and 270°. Transfer onto the solder-coated substrate occurs within this thin progressing interface in a conveyor belt-like fashion. For the assembly to work well, the conditions that follow are essential. The temperature has to be maintained constant, which is achieved using a heated ethylene glycol bath that is kept at 95°C surrounding the glass assembly container. Metal surfaces, including the solder, need to be free of surface oxides, which is achieved by reducing the pH of the assembly solution to pH 2.0 with hydrochloric acid. It is possible to get good $>$ 90% coverage in a single pass; however, full coverage (99%–100%) required several passes through the interface. Assembly in this system occurs only during upward motion. Downward motion removes loose unassembled components, which then transition back to the liquid-liquid interface. Saturation is observed in five to ten passes, which takes less than 1 min. Rapid assembly is an important advantage over previous trials that took place in the drum assembly system.

Fig. 5 shows patterned self-assembly results of Si and SU-8 components with 20 μm and 60 μm side lengths using the new conveyer belt-like assembly system. Assembly with different area densities is tested using regular arrays [$\sim$25% area density; Fig. 5(a) and (b)] and arbitrary text ($<$ 5% area density; Fig. 5(a) and (b) (insets)). Defects, measured by the cumulative number of missing, misaligned, and excess components, were found to be independent of the area density, component type, and component size. For example, Fig. 5(a) shows 100 receptors, each carrying a single correctly aligned SU-8 component, where one is misaligned (circled), reducing the yield to 99%. Fig. 5(b) shows $\sim$400 receptors, each receptor carrying a Si chiplet; however, three additional components (circled) were found to be present reducing the yield to 99.3%. These pictures are representative images of assemblies that extend over larger areas, currently limited to 1 cm long and wide substrates. The present assembly system has a 1 cm^2 interfacial area/capacity, which limits the amount of dies per experiment at the interface to 250 000 20 μm $\times$ 20 μm-sized dies, and 40 000 50 μm $\times$ 50 μm dies, for example. Additionally, in a container of a given size and width, the assembly process exhibits a higher introduction rate for smaller dies: The rate scales inversely with the square of the die size. In other words, a 10$\times$ size reduction in the component yields a 100-fold increase in the rate of introduction. The number of dies that are introduced at the surface is generally larger than the number that assembles on the receptors. Actual assembly rates depend primarily on the product of the components' introduction rate to the solid interface and the fraction of the solder-coated receptors' area

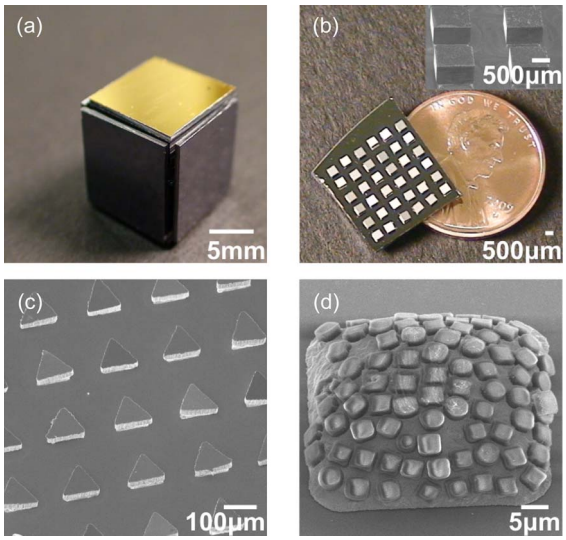


Fig. 6. Scaling limits testing of component assembly spanning three orders of magnitude in size including (a) 1 cm Si cubes (assembly not possible), (b) 1 mm Si blocks, (c) 100 μm Si triangles, and (d) 3 μm-sized SU-8 blocks and discs.

(in units of dies) covering the substrate. For example, for the intermediate 25% area density test structures [Fig. 5(a) and (b)] $\sim$62 500 components assemble onto the substrate in 45 s, which is a large number when compared to a state-of-the-art serial robotic chip assembly machine, where 100 times smaller rates (a few components per second) are difficult to achieve. Fig. 5(c) shows sample views of wide-area silicon self-assembly. These components assemble with good alignment accuracy, which can be determined using overlaid CAD measurement guides. For example, 60 μm sized high precision Si components [Fig. 5(d)] yield an average placement accuracy of 0.9 μm (STD) and angular orientation accuracy of 0.14° (STD) [Fig. 5(e)], which are, respectively, 21 and 2.2 times better than our previous results [11]. The observed accuracy does not represent the limits of the self-assembly process itself, since the recorded numbers fall within the precision of the lithography and etching methods used to produce the components and receptors—the lateral dimensions of the Si blocks varied by 1 μm, the SU-8 blocks varied by 1.5 μm, while receptors on Si varied by 1 μm and receptors on propylene terepthalate (PET) varied by as much as 2.5 μm. Additionally, SU-8 blocks had rounded corners with 2 μm radius of curvature, which was smaller than the observed 3–4 μm radius of curvature of the solder coated receptors.

The process is scalable toward both larger and smaller component dimensions. Gravity sets the scaling limit when considering macroscopic dimensions. Gravitational forces scale with the volume (x^3 for cubic components), yielding an energy gain over a distance x that is proportional to x^4. The energy gain due to the reduction of surface free energy scales with the area x^2 and becomes less important at macroscopic scales. For example, gravity causes a 1 cm^3 cube [Fig. 6(a)] of hydrophobic Si with a hydrophilic metal contact to drop through the oil-water interface, whereas 1 mm- (Fig. 6(b), square) and 100 μm- (Fig. 6(c), triangular) sized components are captured by the interface, transported, and assembled. The upper limit for the lateral dimensions can be pushed upwards by using components with reduced density or thickness. Considering an extension toward nanoscopic dimensions, the thermal energy (32 meV at 95 °C) provides a theoretical scaling limit. The interfacial energy gain (larger than 50 mJ/m^2) exceeds the Brownian energy by many orders of magnitude until the components reach submolecular (< 1 nm^2) dimensions, suggesting that a continued scaling is possible; the self-assembly of phospholipids into 2-D sheets at an oil-water interface can be seen as an analog, providing evidence that this might be possible. Experimentally, however, the process is challenged by the difficulty in realizing receptors that remain stable over time. As described before, solder-directed assembly is sensitive to surface oxides, which reduce the surface energies driving the self-assembly and self-alignment. While the solder oxidation is a challenge, the general process of surface tension-directed chip assembly using an energy cascade to transport and pre-orient the components should remain intact at much smaller scales. There is some experimental evidence supporting this statement. Fig. 6(d) shows a stable 20 μm $\times$ 20 μm $\times$ 10 μm solder bump used to capture 3 μm $\times$ 3 μm $\times$ 2 μm-sized SU-8 objects. Transport and assembly remains intact for these highly scaled components, and we anticipate scaling to continue if solutions are found to form highly scaled receptors that maintain stable over time.

Fig. 7 shows an application of the process realizing a segmented monocrystalline solar cell on a flexible PET substrate, while reducing the material use of Si by a factor of 10 when compared to conventional monocrystalline cell architectures. The material reduction was achieved by using 20 μm thin silicon chiplets instead of commonly used 200–300 μm thick Si wafers where most of the Si is used to provide a mechanical support. The difference between the Si chiplets in this figure and those that were assembled from the liquid-liquid test experiments previously (Fig. 5) is that they carry a $p-n$ junction that is fabricated using an LPCVD-deposited phosphosilicate glass (PSG) dopant layer and a high-temperature diffusion drive-in step prior to their assembly onto the flexible PET substrate; the Experimental Section provides further details. The 20 μm thin layer of Si adds little height to the 175 μm thick PET substrate. Another difference shown in Fig. 7(a) is that the PET substrate carries a common copper contact on the entire surface which is partially masked with chromium to prevent wetting of solder in undesired areas; solder does not wet chromium.

The process forming the solar cell modules uses an SU-8 isolation layer that is applied by spin coating before it is etched back in a reactive ion etcher to reveal the p-doped region of the chips. This layer is designed to be tolerant of assembly defects [Fig. 7(b)] such that SU-8 fills in voids and locations of missing dies (vacancies); when spin coated, polymers, including SU-8, form a thinner film over protruding objects when compared to valleys. This self-leveling behavior makes the cells tolerant against assembly defects; a missing Si diode [highlighted region, Fig. 7(b)] will not result in a short and failure of the cell, since these regions are coated with SU-8. Details of this strategy can be found in the Experimental Section. As a top contact we used a semitransparent 20-nm thin sputter-deposited film of Au [Fig. 7(c)] and adjusted the input power accordingly; however,

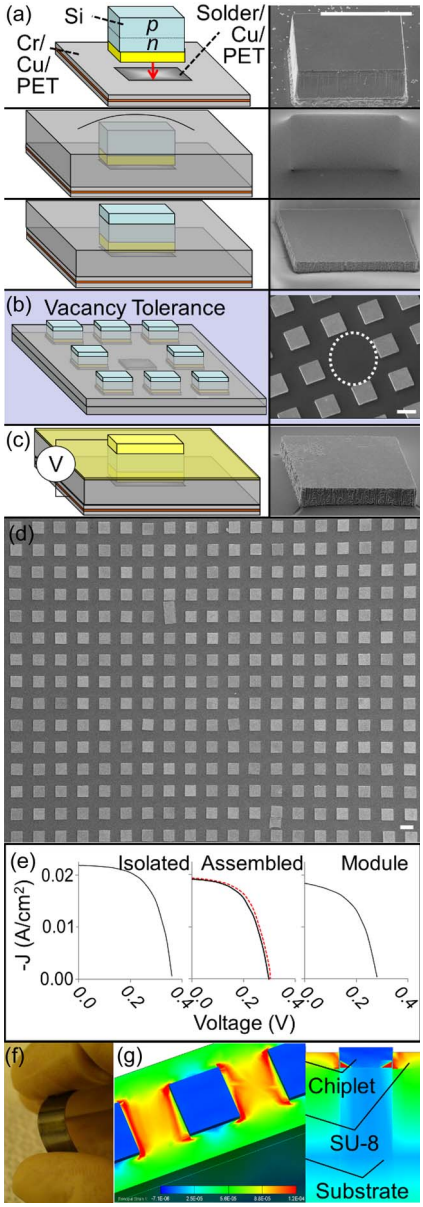


Fig. 7. Flexible segmented monocrystalline solar cell fabrication procedure, result, and characterization. (a) Isolation process and representative scanning electron micrographs (SEM) showing each step, first assembling, then spinning isolation SU-8 layer, and finally etching the isolation layer back to reveal the top of the components. (b) Defect-tolerant design strategy and result (SEM) where vacancies are covered with SU-8, preventing shorts to the substrate. (c) Top contact deposition process and representative SEM. (d) Micrograph of an assembled array. (e) I/V load curves of cells before (left) and after assembly in unbent (red curve, center) and bent configuration (1-cm radius of curvature, black curve, center); (e, right) I/V load curve of a module as depicted in (f); (g) Finite-element computer simulation (CoventorWare Suite) of the strain inside the composite flexed (1-cm radius of curvature) structure composed of a 175 μm PET layer holding a 20 μm thin film of Si cubes surrounded by SU-8 where the region of maximum strain is located at the top metal contact between silicon cells and at the chiplet edges. Perspective and side slice views are shown. 60 μm scale bars.

materials including transparent conducting oxides could be used as well.

Fig. 7(d) shows a representative, zoomed-in SEM image of the completed structure. We tested the cells before and after assembly and found very little difference in their electrical properties [Fig. 7(e)]. Individual cells that were released from the wafers had 4.4% power conversion efficiencies, 0.34-V open circuit voltage, and 0.67 filling factor at 0.7 suns (Philips PAR38 lamp, calibrated with an International Light Technologies 1400-A photometer), which could be improved to established levels by incorporating an intrinsic region and through optimization of doping levels/profiles, geometry, antireflection coatings, surface passivation layers, and contacts. This would be outside of the focus of this research, which centers on self-assembly. The cells retained their electrical properties when assembled (4.2% efficiency 0.30 V, 0.56 FF) (Fig. 7(e), red line), confirming that the assembly procedure and exposure to the oil-water interface does not alter the cells. Similarly, the electrical properties changed only slightly (3.8%, 0.31 V, 0.55 FF) (Fig. 7(e), black line) when bent as long as the radius of curvature remains above 1 cm. The change in the recorded I/V curve between bent and unbent structures is reversible, suggesting that a change in the local illumination angle is the likely cause. We repeated the assembly of multicomponent modules several times and found a slight reduction in the open circuit voltage and short circuit current when compared to the original isolated cells. For example, the module ["Module," Fig. 7(e)] had an efficiency that was 1% smaller than the original isolated cells (marked as "Isolated"). This decrease in efficiency when the components are connected in parallel is likely due to variances in component doping, top contact uniformity, and isolation layer thicknesses. A completed module can be seen in Fig. 7(f). We have not yet tested effects of fatigue and minimal possible radius of curvature of bent structures, but have observed situations where the top contact failed. The top contact and chiplet edges are the locations of highest strain, which is consistent with finite-element modeling (CoventorWare Suite (Coventor, Inc.)) of the structure shown in Fig. 7(g).

This process compares well with the best of the vial/drum-based assembly methods. The relative assembly precision in relation to the component size is about 1.5% of the component size, which is similar to what was previously observed. In absolute terms, the precision can exceed 0.8 μm for highly scaled (60 μm) objects. Moreover, since a larger number of microscopic components can be contained in the assembly container of a given size, it is possible to achieve much higher assembly rates compared to the drum-based delivery scheme, where the minimal component scaling has not yet exceeded 100 μm. Specifically, we observed assembly rates that were two orders of magnitude faster: 80 000 per minute. Drawbacks include a scaling limitation, in which the maximum component size is limited by gravity that pulls very large components through the interface, and the fact that surface engineering is required to correctly suspend and orient components at the interface.

D. Self-Tiling

A separate limitation of the assembly processes that have been described thus far can be found in their respective maximum achievable area coverage. Our illustrations (Figs. 1–7) each depict spaces between individual assembled components. This unused space results directly from the receptor pad design.

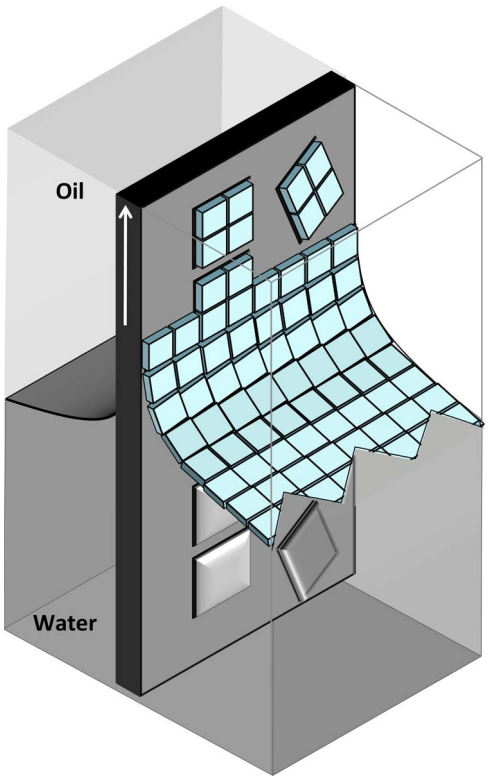


Fig. 8. Transfer and self-tiling procedure for Si tiles at a liquid-liquid-solid interface. The available area and curved shape of the interface cause the components to form a closely packed 2-D raft. Upward motion of the substrate yields a dynamic contact angle where the receding water layer becomes sufficiently thin for the gold to contact the solder domain allowing the sections of the raft to transfer to the solder domain.

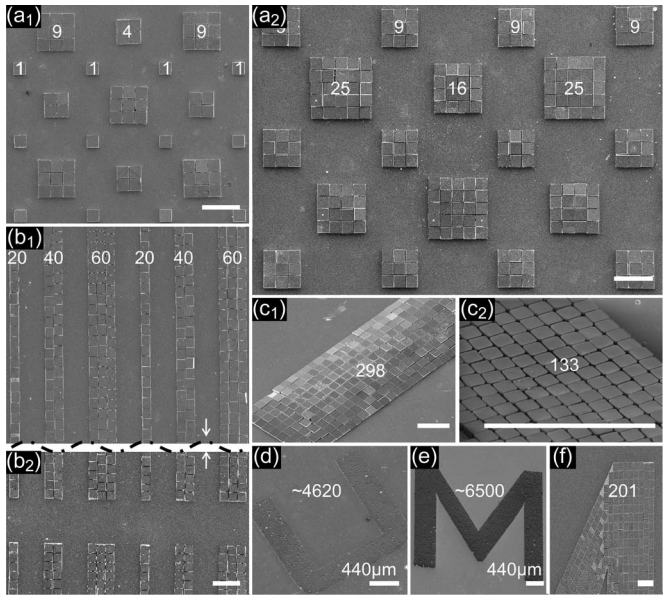


Fig. 9. Scanning electron micrographs of tiled domains of different sizes. (a) Square domains with room for 1, 4, 9, 16, and 25 silicon tiles, 60 μm on a side. (b1) Center and (b2) end region of 5 mm long linear domains measuring 1, 2, and 3 component widths wide. (c1) Rectangular domains with room for 300 Si-tiles and (c2) 133 SU-8-tiles. (d, e) Large letter-shaped domains with room for thousands of 20 μm wide SU-8 tiles which cover $> 97\%$ of the area. (f) Close-up view of a typical grain boundary in asymmetric elbow sections of letter-shaped regions. Scale bars are 180 μm with the exception of large area domains (d, e) where 440 μm is used (indicated).

Fig. 8 shows a strategy we refer to as self-tiling that aims to eliminate these spaces by removing the space between the receptors on the substrate. While this concept can be demonstrated in the barrel assembly chamber, we describe it here within the context of self-assembly from the liquid-liquid interface. Once again, the process relies on a stepwise reduction of interfacial energy, as previously described in Fig. 4; however, in this process, the rafted tiles are now transferred to molten solder domains of sizes larger than one component. Unlike in the previous procedure (Fig. 4), the position of multiple components can be determined and controlled by a single, larger receptor domain. Pre-oriented and self-packed Si components within the liquid-liquid interface are transferred to the molten solder domains of tailored sizes such that the number of transferred components is determined by the available areas made up of the solder domains, as well as the number of defects at the interface. The reduction of surface free energy then continues to drive the components to self-tile, thereby minimizing the amount of exposed solder, as well as the impact of interface defects. Self-tiling shares some similarities with dip coating self-assembly that has widely been used to arrange nanoscale objects at a three-phase line that commonly recedes due to controlled evaporation [49]. However, the self-tiling process described here is different, since it allows us to control the upside-down orientation of the parts as well as the location of their attachment using a reduction of the surface free energy; moreover it forms a well-defined raft at the liquid-liquid interface.

Fig. 9 shows self-tiling results where the size of the receiving solder domains has been increased to make room for an increasing number of microscopic tiles. Defect-free tiling is possible at predetermined locations if the side length of the domain is an integer multiple of the tile size, as illustrated using domains with space for 1, 4, 9, 16, or 25 60 μm-wide silicon tiles [Fig. 9(a)]. Fig. 9(b) shows an example of linear domains of various widths, where perfect arrangement is possible over millimeter-long distances. Limits of the tiling process begin to appear when the individual domains have room for several hundred tiles. For example, the domain shown in Fig. 9(c) has room for 300 tiles but only 298 tiles are assembled onto the surface, as two can be seen missing. On increasingly large domains with room for many thousands of tiles, grain boundaries will finally emerge. The letters U and M in Fig. 9(d) and (e) provide examples where we used domains with footprints that violate the crystallographic symmetry of the square-shaped components. These domains have room for 4600–6500 microscopic SU-8 tiles (20 μm side length), and $> 97\%$ of the area is covered with tiles. In these types of structures, most of the imperfections occur in rounded regions and in elbows where crystal fronts merge [Fig. 9(f)]. Well-ordered "single" crystal domains with 200–500 tiles are commonly observed. Note that assembly in this system is still limited to the number of components that can fit at the interface. Insufficient components or defects within the interface during assembly will slow the tiling process.

Fig. 10 shows self-tiling images resulting from testing various domain and tile sizes and shapes. In Fig. 10(a), the width

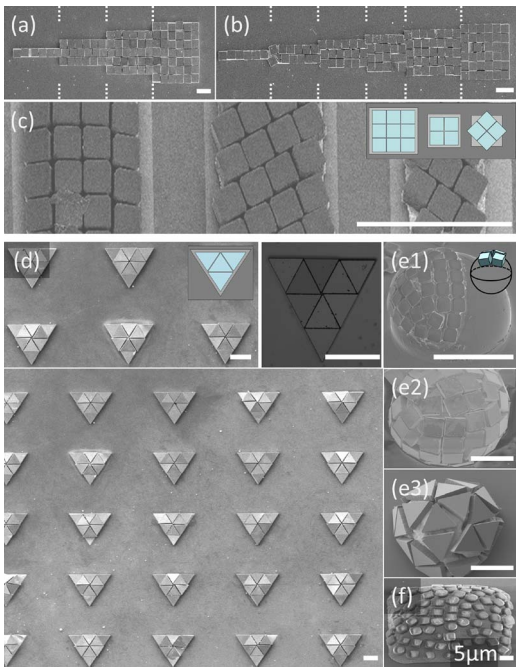


Fig. 10. Micrographs demonstrating self-tiling behavior and design rules. (a, b) Micrographs of domains that allow (a, no defects) and hinder (b, one defect) lateral sliding/annealing across the dotted lines; domain (b) does not support lateral sliding and one out of 126 tiles is misaligned. (c) Domains where the width is reduced from 4 to 3.5 to 2.5 and violate the integer multiple widths requirement, which leads to new arrangements that maximize area coverage. (d) Micrographs of triangular domains that are tiled with 270 triangular Si tiles showing one defect. (e) Spherical domains with at least 100 μm radius of curvature using tiles of (e1) 20 μm square SU-8, (e2) 60 μm square silicon, and (e3) 100 μm triangular Si. (f) 3 μm-sized ultra-small SU-8 tiles. 120 μm scale bars unless otherwise indicated.

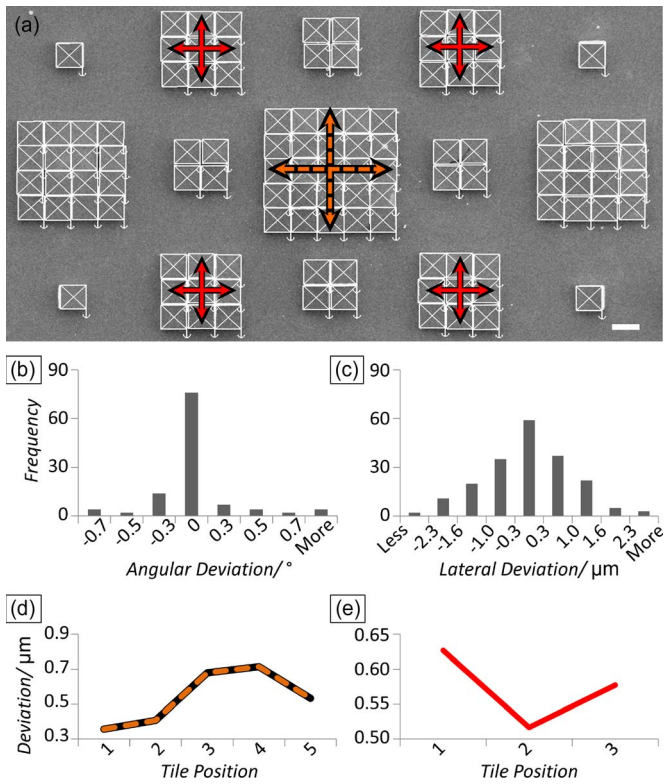


Fig. 11. Measurement to determine the lateral and angular alignment precision. (a) Scanning electron micrograph overlaid with CAD measurement guides. (b) Histogram of the recorded angular deviations with a calculated STD of 0.3°. (c) Histogram of the lateral deviations with a calculated STD of 1.1 μm. (d) Lateral deviations of tiles along the highlighted center row and column of the 5 × 5 tile region showing improved accuracy at the region boundaries. (e) Lateral deviations of tiles along the highlighted center rows and columns of the depicted 3 × 3 tile regions, wherein the center tiles have better alignment. 60 μm scale bar.

of the domain is adjusted to receive 1, 3, 5, and 7 rows of Si tiles, a design that maintains the array's periodicity (rows can slide from left to right), with defects tending to be less likely. The domain shown in Fig. 10(b) violates this design rule. Here, the domain received 1, 2, 3, 4, 5, and 6 rows of Si tiles. The rows cannot slide from left to right, and the lattice periodicity breaks down. A crystal boundary is forced to form at each transition, and a slightly reduced ordering is observed due to the reduction in the extent of sliding motion that is allowed. Another design rule for the domains suggest the use of dimensions that are integer multiples of component lengths; violating this rule causes tiles to be arranged in a somewhat less predictable way to maximize coverage. Fig. 10(c) shows this behavior in a solder domain where the width is decreased from 4 to 3.5 to 2.5 component widths, resulting in lattices of 20 μm-wide SU-8 components with positive and negative slopes that cannot be predetermined.

This process is not limited to specific tile and domain geometries, as other regular polygons can be used as well. Fig. 10(d) shows equilateral (100 μm side length) triangle silicon tiles covering an array of triangular domains where each domain size was chosen to provide space for nine tiles. Assembly yields and area coverage in these types of assemblies exceed 99%.

Fig. 10(e), meanwhile, tests an instance where the rules of matching tile and target domain geometry are violated. The depicted spheroids are $\sim$ 200 μm (diameter) silica beads with a receptor domain on top to receive (e1) 20 μm square SU-8 blocks, (e2) 60 μm square silicon tiles, and (e3) 100 μm triangular silicon tiles using the previously described assembly mechanism. $>$ 99% coverage can no longer be sustained, since the tiles are not optimized to match the surface, and pleating occurs [50]. It should be noted that the process can be scaled to smaller and thinner components. For example, Fig. 10(f) shows the results of the assembly of 3 μm-sized SU-8 parts that are 2 μm thick. These components, however, are not homogenously shaped. The image shows a reduction in area coverage that can be explained by the larger variation in size and shape, emphasizing the importance of component uniformity.

Fig. 11 provides a statistical analysis of the alignment accuracy of the given assemblies. We overlaid computer-aided design measurement guides as shown in Fig. 11(a) to take accurate location and angular deviation measurements on a variety of tiled regions. By first averaging the row and column x and y values, we were able to calculate each tile's lateral deviation from the average. Fig. 11(b) and (c) provide histograms of the recorded lateral and angular deviations across the image, which exhibit standard deviations of 0.3° and 1.1 μm, respectively. We also looked at the lateral deviation as a function of the position within tiled domains, since we noticed that the positional (lateral) accuracy of the components varies slightly with domain size. Fig. 11(d) shows the average displacement along the row and column highlighted in the 5 × 5 tile region. Fig. 11(e)

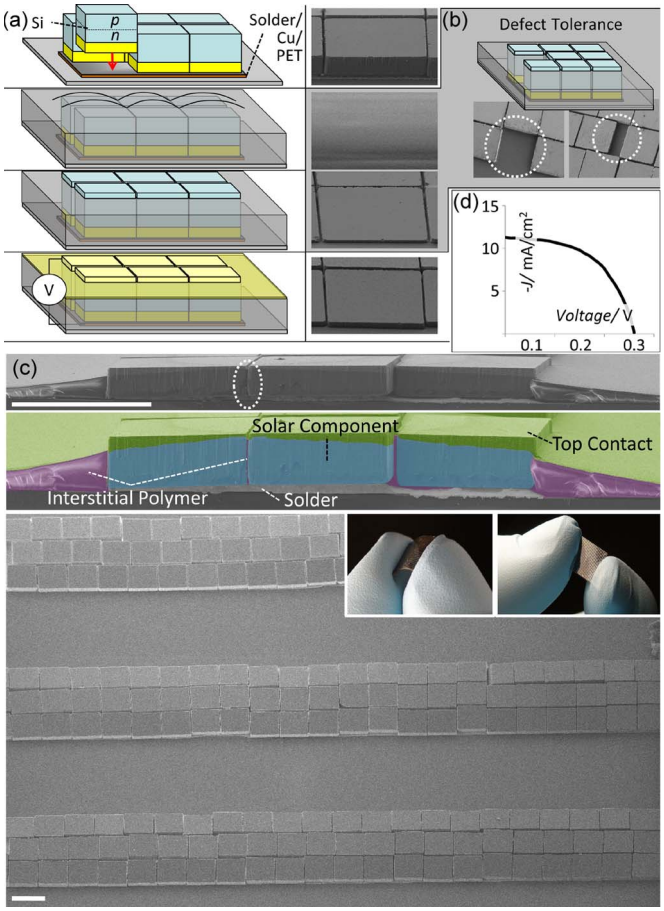


Fig. 12. Flexible, segmented, self-tiled monocrystalline Si solar cell fabrication procedure, result, and characterization. (a) Assembly and isolation process with scanning electron micrographs (SEM) representative of each step. (b) Defect-tolerant design strategy and result (SEM) where vacancies and lattice mismatches are filled in with SU-8, preventing short circuiting to the substrate. (c) Cross section, colorized cross section, top view, and photographs of the device. (d) Resulting I/V curve. 60 μm scale bars.

shows a similar plot for the four 3 $\times$ 3 regions. As a general trend, we observed that, for larger regions, the best positional accuracy is observed at the edges of the pattern. The trend is reversed for very small domains, where imperfections in the domain boundary are isolated and tend not to propagate to the inner components. Overall, however, these variations are very small, and the alignment accuracy that we observed is presently limited by the precision of the fabrication steps. The observed alignment accuracy using the etching techniques that we have used is commonly between 1% and 2% of the component size.

Fig. 12 shows an application of the self-tiling process combined with the above solar cell chiplets (Fig. 7) realizing a segmented monocrystalline solar cell on a flexible PET substrate, while reducing the material use of Si by a factor of 10 when compared to conventional monocrystalline cell architectures. Just as before, the architecture is designed to be tolerant of vacancies, but is also tolerant of tiling-specific defects [Fig. 12(b)]. Connecting the top contact to the conducting solder domain below completes the electric circuit. Fig. 12(d) shows the resulting solar cell module I/V curve under 45 mW/cm^2 solar radiation, producing a fill factor of 0.54 and an efficiency of 4.18%, once again using a solar simulator. The

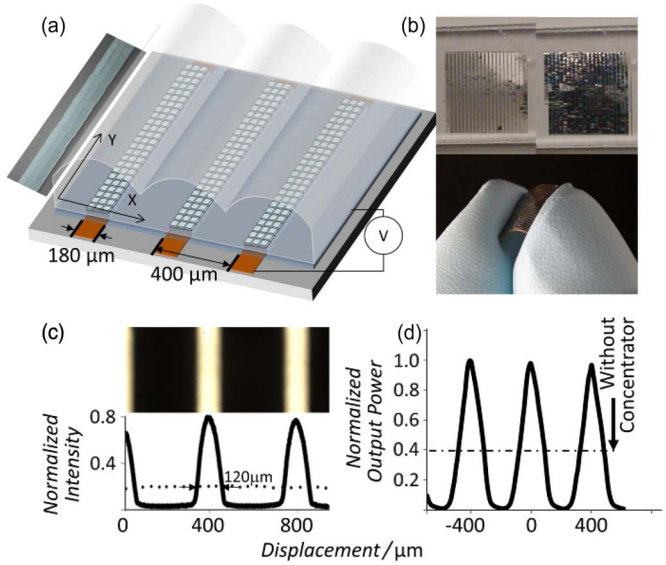


Fig. 13. Photovoltaic concentrator module—schematic, result, and characterization. (a) Schematic showing lenticular concentrator array, tiled chiplets, and dimensions. (b) Optical images of the completed module with applied concentrator array misaligned (left), aligned correctly (right), and removed. (c) Optical image and intensity profile of the concentrated light observed through a microscope. The dotted line represents the case when no concentrator is present. (d) Normalized power observed when the concentrator array is shifted in x direction.

20 μm thin layer of Si adds little thickness to the 130 μm thick PET substrate, and the cells retained the electrical properties when bent as long as the radius of curvature remains above 1 cm, which is similar to previous results above.

Fig. 13 details how the silicon tiles form parallel, 180 μm wide stripes of Si that are compatible with an acrylic lenticular concentrator array that is used to form a microconcentrator-enhanced solar cell sandwich structure. The lenticular array we used is fairly thick ($\sim$2.2 mm), which resulted in a final structure that was no longer flexible. Specifically, we used a commercially available concentrator array (Edmund Optics, P/N NT43-028), which was placed on top of the solar cell module such that incident light was focused onto the parallel stripes of tiled Si [Fig. 13(a)]. The radius of curvature of the cylindrical microlenses is $\sim$0.83 mm, corresponding to a focal length of $\sim$2.2 mm. In our experiments, we used collimated light and observed the width of the focused lines of light (full-width passing 80% of the light) to be $\sim$120 μm [Fig. 13(c)]; the dotted line represents the intensity level without the lenticular array. Fig. 13(b) shows optical photographs of the solar cell module underneath the concentrator array. The left depicts the instance when the lens array is poorly aligned. The white paper underneath the structure becomes visible in this case. The dark specks are excess tiles that have not been completely washed away. These tiles are not electrically connected. The image to the right shows the instance when the lens array is correctly aligned to funnel the light to the electrically connected tiles; the paper background is no longer visible, and the structure appears dark. To test the efficacy of the microconcentrator, a micromanipulator was used to shift the lens array perpendicular to the tiled lines. The resulting normalized power plot is shown in Fig. 13(d), where the dotted line provides the reference

output power of the structure without the concentrator. For a constant illumination of 45 mW/cm^2 solar radiation, the 4× concentrator array provided a 2.5-fold increase in output power. The discrepancy can be explained by losses due to the added concentrator material and interfaces and due to nonuniformities in the shape of the intensity profile. From a Si material reduction point of view, the concentrator array, in combination with the 20 μm thin silicon tiles, reduces the amount of Si by a factor of 22 (20 μm thin, 180 μm wide Si strip on a 400 μm pitch) when compared to a conventional 200 μm thick and rigid monocrystalline Si solar cell modules.

Much like discrete self-assembly at the liquid-liquid interface, the self-tiling process allows for greater scaling toward smaller components when compared to drum-based assembly. The smallest self-tiled components demonstrated were 3 μm square tiles [Fig. 10(f)]. One drawback is that the process requires the surfaces to be functionalized, which, in our view, is not a serious disadvantage, considering the minimal effort that is required to adjust the hydrophobicity/hydrophilicity of a surface. Compared to discrete self-assembly at the liquid-liquid interface, self-tiling allows for greater substrate area coverage and self-organization.

E. Self-Assembly Methods Comparison

Table I summarizes the benefits and results of the current state of the art. Solder-based alignment allows for simple design and rapid assembly. Well-based alignment reduces a specific defect: Multiple components per receptor are not allowed. Pedestal-based alignment allows for the use of standard rectangular component with multiple I/Os, sequential size-based multiple component type assembly, and unique angular alignment. Drum assembly has not yet been successful in assembling very small dies, as it relies on gravity to transport components, which is less effective for highly scaled components. The use of the triple interface has led to some improvement in scaling to smaller component sizes. In this scheme, components arrive at the surface in a compacted pre-oriented fashion, much like in a Langmuir-Blodgett trough.

III. Conclusion

Self-assembly processes produce well-ordered assembled structures with yields that approach those of deterministic pick and place assembly processes. They are massively parallel and can, in principle, lead to much higher component assembly throughput than possible in a robotic die/handling machine, where 600 pick and place operations per minute is a challenge. As an example, we were able to arrange disordered chips with an assembly rate that exceeded 60 000 chips per minute in some cases (Fig. 5). Moreover, self-assembly can be scaled to enable the assembly and interconnection of microscopic chiplets that are at least one order of magnitude smaller, considering linear dimensions, and three orders of magnitudes smaller, considering volume/weight, than what is possible using robotic pick and place machines at reasonable rates. A challenge going forward can be found in the automation and scaling up of fluidic self-assembly substrates and throughput, which remains an area where little investment has been made. This is the unfortunate reality that has prevented this emerging technology from maturing. Applications are plentiful and should not be limited to solar cells. Integration and distribution of solid-state lighting LEDs, microscopic lab on a chip LED light sources, signal processing units, and energy producing elements are equally interesting. The demonstration of high volume and wide area assembly, maintaining current yield and alignment accuracy metrics, however, will be a key area to concentrate research.

IV. Experiment

A. Fabrication of the Large Silicon and Glass Components

The silicon blocks and glass components were made using standard photolithography and surface micromachining from p-type silicon wafers and borofloat glass wafers (University-wafer, Boston, MA), respectively. Alignment marks on the top were formed by spin-coating Shipley 1075 photoresist (Shipley, Phoenix, AZ) at 3000 rpm onto the wafer, UV exposure through a shadow mask for 80 s, development in MIF-351 1:5 developer for 2 min, and etching in a deep-trench etcher (SLR-770, Plasmatherm, North St. Petersburg, FL) for 1 h. The contact pad on the back was formed by coating 25 nm of Cr and 500 nm of Au using an electron-beam evaporator. Shipley 1813 photoresist (Shipley, Phoenix, AZ) was spin coated at 4000 rpm, exposed through a shadow mask for 7 s, and developed in MIF-351 1:5 developer for 15 s to expose the underlying metal areas that were subsequently removed by etching using 4 KI:1 I2:40H2O (gold) and 1 HCl:1 Glycerol:3H2O (chromium). Finally, we diced the wafers to obtain the components. The glass components carry contact pads on a single side, and no alignment marks on the front. The contact pads were made of gold, and five of them were protected with Shipley 1813 photoresist that was later rinsed away. The protection was necessary to ensure correct angular orientation.

B. Fabrication of the Silicon and SU-8 Pedestals and Solder-Coated Areas

The pedestals were fabricated either by deep-trench etching silicon or photopolymerizing SU-8 photoresist. The etched silicon pedestals were formed by spin-coating Shipley 1075 photoresist (Shipley, Phoenix, AZ) at 3000 rpm onto a 500 μm thick p-silicon wafer, followed by UV exposure through a mask for 80 s, development in MIF-351 1:5 developer for 2 min, and etching in a deep-trench etcher for 3 h. The patterned protective photoresist was removed in acetone to expose 300 μm tall silicon pedestals underneath. The pedestals made of SU-8 were formed by spin-coating SU-8 2001 photoresist (Microchem, Newton, MA) at 1000 rpm onto a 500 μm thick p-type silicon wafer, followed by a two-step soft bake at 65 °C for 7 min and 95 °C for 60 min on a hotplate, a UV exposure through a mask for 60 s, a postexposure bake (PEB) at 65 °C for 1 min and 95 °C for 15 min on a hotplate, and a development step in propylene glycol methyl ether acetate (PGMEA) for 60 min. Following the fabrication of the pedestals, the wafers

were coated with 25-nm titanium and 500-nm copper using an electron-beam evaporator. Shipley 1805 photoresist (Shipley, Phoenix, AZ) was spin coated at 1000 rpm, exposed through a mask for 30 s, and developed in MIF-351 1:5 developer for 60 s to expose the underlying metal areas that were subsequently removed by a 15 s etch using a ferric chloride solution (1.4 g of FeCl3 per milliliter of H2O, pH 1.3, 20 s) for copper and 40% NH4F/49% HF 10:1 buffered oxide etchant for titanium. The remaining copper squares were coated with solder by removing the protective photoresist in acetone and by immersing the wafer into a solder bath until each copper square was coated with solder.

C. SU-8 Component Fabrication

SU-8 components were fabricated on a 500 μm thick p-type silicon handling wafer (Ultrasil, Hayward, CA). A 13-nm release layer of Omnicoat (Microchem, Newton, MA) was spun on the wafer at 3000 RPM for 30 s and baked for 1 min at 200 °C. SU-8 2010 (MicroChem, Newton, MA) was then spin coated at 3000 RPM for 30 s and baked at 65 °C for 1 min and 95 °C for 2 min. The 20 μm components were defined by an 132 mJ/cm^2 UV exposure and cured with a PEB of 65 °C for 1 min and 95 °C for 2 min. The SU-8 was developed for 4 min in PGMEA. Next the Omnicoat layer surrounding the newly revealed SU-8 blocks was removed by a 40 second oxygen plasma reactive ion etch clean (O2-100 sccm-100 W-100 mTorr). A 200 Å adhesion layer of chromium and a 3000 Å thick gold binding site were then deposited by e-beam evaporation, and the sacrificial Omnicoat layer was underetched by Microposit MF-319 developer (Shipley), releasing the SU-8 components. These completed blocks were finally rinsed in isopropyl alcohol by pipette and were then introduced to a 10-mM solution of MUA in ethanol for 15 min to apply a hydrophilic SAM to the gold. After one more rinse step by pipette in isopropyl alcohol, the SU-8 component fabrication was complete.

D. Solar Cell Fabrication

The silicon solar cell components were fabricated on a p-type silicon on insulator wafer (SOI, 20 μm device layer, 0.095–1 Ω/cm^2, Ultrasil, Hayward, CA) that was first cleaned using an RCA cleaning standard: 1:1:5 solution of NH4OH + H2O2 + H2O at 80 °C for 15 min, 1:50 solution of HF + H2O at 25 °C for 15 s, 1:1:6 solution of HCl + H2O2 + H2O at 80 °C for 15 min, and finally HF + H2O at 25 °C for 15 more seconds with a DI water rinse after each step. Following the cleaning, the surface p-type device layer was doped n-type using 3500 Å of LPCVD-deposited PSG as a source. The phosphorus dopant was diffused into the silicon in a nitrogen ambient at 1150 °C for 3 h in a furnace, and the remaining PSG was stripped in a 1-min BOE etch. The wafer was once again cleaned with the RCA process before being immediately inserted in an e-beam evaporation deposition system and coated with a 200 Å adhesion layer of chromium and a 2000 Å thick binding site pad of gold. The wafer was then photolithographically patterned by exposing spin-coated photoresist (Microposit 1813, Shipley, Phoenix, Arizona) with 96 mJ/m^2 UV light. After a 25-s developing step in 1 MIF-351: 5 H2O developer, the patterned wafer was ready to be etched. First, the gold surrounding the component pads was removed in GE-6 (1:10) (Acton Technologies, inc., Pittson, PA) for 9 min. Second, the chromium was etched in Cr-12S (1:4) (Cyantek, Corp, Fremont, CA) for 80 s. Finally, the field silicon was etched using a Bosch process in a DRIE with the SOI buried oxide acting as the etch stop. The sacrificial buried oxide layer was etched in 49% HF for 7 min to release the completed monocrystalline silicon solar cells. The released cells were treated with a 10-mM MUA in ethanol solution for 15 min to to render the gold surface hydrophilic, and rinsed in isopropyl alcohol, and treated with 200 mM hydrophobic glycidoxy functional methoxy silane, Dow Corning Z-6040, in ethanol for 15 min, followed by a dehydration bake at 115 °C for 5 min to render the Si surface hydrophobic.

E. Silicon Substrate Fabrication

A 500 μm thick p-type silicon wafer (Ultrasil, Hayward, CA) was patterned by liftoff to serve as the self-assembly substrate. The wafer was first cleaned in a sulfuric acid and hydrogen peroxide solution at 115 °C for 15 min before being rinsed, etched in HF (1:10), and dump rinsed again. Photoresist (Microposit 1813, Shipley, Phoenix, Arizona) was then spin coated at 2500 rpm for 30 s. After a soft-bake at 105 °C for 1 min, the substrate was patterned with 96 mJ/m^2 UV light and developed in 1 Microposit 351: 5 H2O developer for 25 s. A 15-s descum in an oxygen RIE next ensured subsequent metal adhesion. The 200 Å Cr and 3000 Å Cu pads were then deposited in an e-beam evaporator. Acetone was used as a solvent to lift off the metal and leave behind the patterned pads on silicon. Finally, the pads were dip-coated with solder (Y-LMA-117, mp. 47 °C, Small Parts, Miami Lakes, Florida).

F. Conductive Flexible PET Substrate Fabrication

A 170 μm thick sheet of PET used to create a self-assembly substrate that featured a conductive backplane. The PET surface was cleaned by soaking in isopropyl alcohol for 10 min and then treated in a 100 W reactive ion etch ammonia plasma for 30 min. Immediately following the plasma surface treatment, the PET was sputter-coated with 3000 Å (11 min, 250 W) of copper, followed by 200 Å (2 min, 250 W) of chromium. AP-300 (Silicon Resources, Chandler, AZ) adhesion promoter was applied by spin coating at 3000 rpm for 30 s. A spin on glass (SOG, Accuglass 111, Honeywell) etch mask was applied at 3000 rpm for 30 s, soft baked for 2 min at 80° on a hotplate, and 1 h at 100 °C in an oven. Adhesion promoter hexamethyldisilazane (HMDS) was introduced in vapor form for 2 min. Photoresist (Microposit 1813, Shipley, Phoenix, Arizona) was applied by spin coating and exposed with 96 mJ/cm^2 UV light. After a 25-s developing step in 1 MIF-315: 5 H2O developer, the SOG etch mask was etched in a reactive ion etcher (150 W, 75 mTorr, Ar: 50 sccm, CF4: 25 sccm, CHF3: 50 sccm) forming windows down to the chromium layer. Acetone was used to remove the surrounding photoresist, and the chromium was etched using Chromium Cermet Etchant

TFE (Transene Company, inc, Danvers, MA) in 2 min revealing the copper squares. The SOG mask is easily removed with a 30-s HF dip. Finally, the solder was applied to the copper squares by dip coating the substrate in a bath of molten solder (Y-LMA-117, mp. 47 °C, Small Parts, Miami Lakes, Florida).

Self-Leveling Polymeric Isolation Process: Following self-assembly, SU-8 2010 was spin coated at 2500 RPM for 30 s over the sample surface and soft baked at 65 °C for 10 min. It was then flood exposed with 200 mJ/cm^2 UV light, postexposure baked for 10 min at 65 °C, washed in PGMEA for 4 min, and etched back using a reactive ion etcher (CF4: 20 sccm, O2: 80 sccm, 200 W, 100 mT). Finally, 20 nm of Au was sputtered by a dc magnetron sputterer.

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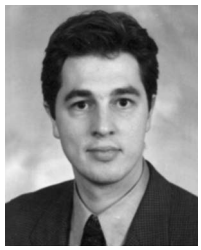

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