

A First Implementation of an Automated Reel-to-Reel Fluidic Self-Assembly Machine

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Macroelectronics is a field or research to extend the application range of electronic and optoelectronic devices. In macroelectronics “larger” is considered better which is in stark contrast to the conventional field of microelectronics where “smaller” and a high function density was the most important driver. The field of macroelectronics requires novel solutions to spread functional materials and electronic or optoelectronic devices over increasingly large areas, on curved, flexible or even stretchable substrates. Most prominent methods use inkjet printing, parallel transfer,^[1–4] robotic pick-and-place,^[38,39] and fluidic self-assembly.^[5–9] Inkjet printing^[26] is most suited to deposit low performance organic semiconductors and hybrid organic/inorganic structures while parallel transfer and self-assembly techniques target the integration of higher performance inorganic devices in a massively parallel fashion. Parallel transfer^[1–4] and self-assembly techniques^[5–10] have been used to fabricate flexible^[11] and curved displays,^[8] curved focal plane arrays,^[2] oscillators,^[3] RF ID tags^[12] and PV modules^[4] spreading ZnO,^[13] GaAs,^[7,14] InP,^[15] GaN,^[16,17] and Si^[2,3,8,18,19] over large and unconventional substrates. Transfer techniques, when compared to engineered self-assembly methods, use a donor substrate/wafer and maintain orientation and integration density which is in stark contrast to directed self-assembly which can redistribute components over large areas and order unorganized parts. For example, a binned container full of semiconductor dies/chiplets of a certain type and quality can be redistributed and assembled at precise locations on a substrate at any desired pitch or required functional density using methods of template directed self-assembly.

The field of template directed self-assembly continues to grow rapidly. However, when it comes to yield and assembly of semiconductor dies/chiplets only two methods are known to approach assembly yields of 100%. The first method uses gravity in combination with complementary 3D shapes to assemble trapezoidal Si dies onto plastic substrates.^[20–22] The second uses gravity in combination with

surface-tension-directed-self-assembly either using hydrophilic/hydrophobic surface patterns^[23–25] or using solder-patterned surfaces to assemble and electrically connect semiconductor dies/chiplets on surfaces with similar yields.^[7–9,16,27,36] Among all the methods that have been published the method first referenced in [22] remains the only method that has been scaled to be used in an industrial manufacturing process; the blueprints of the “self-assembly machine”, however, has never been disclosed. Unfortunately, all published reports describe assemblies over small areas typically less than 1 cm² and in small discontinuous batch like self-assembly experiments involving manual agitation and an experienced scientist. Scaling to large areas appears to be a “hard problem” where there are fewer low hanging fruits, yet it appears absolutely necessary for the research community to demonstrate first blueprints to aid technology adaptation.

In this communication, we report on recent progress towards a first implementation of a self-assembly machine that is based on surface-tension-directed-self-assembly. The reported assembly process is no longer a discontinuous small-batch hand-operated process but resembles an automated machine like process involving a conveyor belt and a reel-to-reel (RTR) type assembly approach with automated agitation. As a comparison, the assembly rate of conventional chip level pick-and-place machines depends on the cost of the system and number of assembly heads that are used. For example, a high-end FCM 10000 (Muehlbauer AG) flip chip assembly system can assemble approximately 8000 chips per hour achieving a placement accuracy of 30 μm. Our current design achieves 15 k chips per hour using a 2.5 cm wide assembly region which is only a factor of 2 better than one of the faster pick-and-place machines; scaling to 150 k chips per hour, however, would be possible using a 25 cm wide web, which would be a factor of 20 faster. In principle, scaling to any throughput should be possible considering the parallel nature of self-assembly. In terms of placement accuracy our precision increase with a reduction of chip and solder bump size.^[9] Generally, it exceeds the 30 μm limits for the components that have been used. Under optimized operational conditions, we achieved an assembly yield of 99.8% using the self-assembly process. As an application the assembly machine is applied to the realization of area lighting panels incorporating distributed inorganic light emitting diodes (LEDs).

Figure 1A describes the layout of the automated RTR fluidic self-assembly platform used in the experiments. The system has two main parts: (i) RTR assembly unit (shaded in gray) consisting of a servo motor, vibrator, rollers, and polyimide web to precisely control relevant parameters such as agitation,

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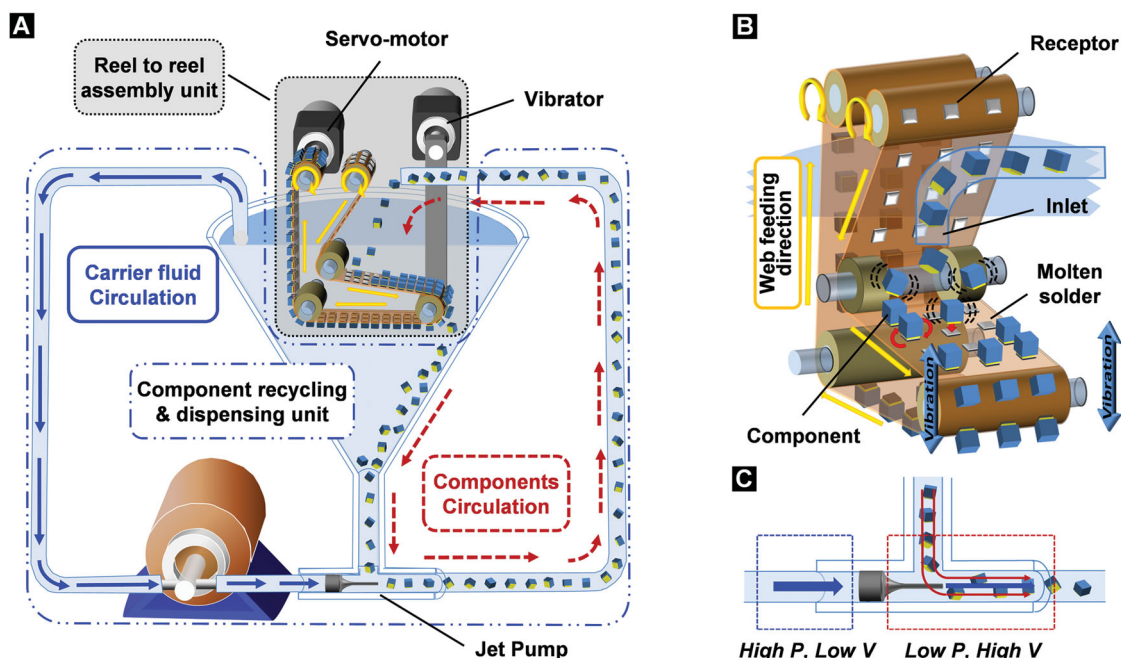


Figure 1. Automated RTR fluidic self-assembly scheme. (A) Overview depicting (i) component dispensing on the basis of liquid flow and gravity which transports the components to empty self-assembly sites (receptors) on a continuously advancing web, (ii) where the components attach at predetermined locations on the basis of surface tension directed self-assembly, and (iii) where recycling of access components is achieved on the basis of gravity at the turning point of the web before they are transported upward on the basis of a fluid drag inside a sufficiently small diameter channel. Mechanical up and down motion of the web is used to induce liquid flow and shear forces to dispense and agitate the components as well as to aid in the removal of access component in the region of the upside-down oriented web. (B) Schematic depicting the details of surface tension directed self-assembly using molten-solder-bump-based-receptors to capture and connect to the metal contacts on the chips. (C) A jet pump based principle is used to achieve recirculation of the chips without passing the components through a mechanical pump where they would get damaged. A preferred location of the jet pump is at the bottom of the slanted funnel where access components arrive on the basis of gravity to be picked up by a high velocity directional jet.

web moving speed, and tension of web as well as a (ii) component recycling and dispensing unit (shaded in blue) which uses the principle of a jet pump to transport unassembled components upward in a confined fluid channel to be released above the substrate to tumble down on the basis of gravity. The system is designed to test various conditions including gentle component introduction to the receptors primarily on the basis of gravity providing the option to minimize the influence of liquid flow induced drag forces inside the large liquid filled funnel which was determined to be an issue in other unsuccessful designs. The components are transported to the inlet using a narrow channel (5 mm inner diameter tubing) which is placed 5 cm away from the polyimide web (50 μm thick, 5 cm wide) typically pointing not directly at the web. As the components enter the large volume the velocity reduces and the components drop down on the basis of gravity transitioning into a vertical trajectory which is the point where the web is located; assembly too close to the nozzle reduces capture rates due to excessive component speeds and drag forces of the injected liquid.

Figure 1B describes the attachment process of the chips on the advancing substrate. The substrates are based on conventional photolithographically patterned copper clad polyimide (50 μm thick, Pyralux LF series, DuPont, NC) films whereby the copper squares (dimensions visible in the results) are coated with a low melting point solder through dip-coating. The solder coating is required for the self-assembly process.

The self-assembly takes place in water which is heated to 80 $^{\circ}\text{C}$ using a controlled immersion heat exchanger to melt the solder (Indalloy #117, MP. 47 $^{\circ}\text{C}$, Indium Corp., NY); higher melting point solder can also be used but requires a different higher boiling point liquid such as ethylene glycol.^[28] The metal contact (Au or Cu) on the chips adhere to the molten solder based receptors on the surface. This adhesion is driven by the minimization of the surface free energy of the liquid solder (400 mJ m^{-2} in water) yielding a stable, aligned, and electrically connected position. The process works particularly well if the pH of the water is adjusted to 2.0 (few drops of hydrochloric acid added) as this removes metal oxides from the surface of the solder drop; an oxide layer — if sufficiently thick — can block the wetting of the metal contact pads.

A typical web velocity using a single component deliver nozzle/zone is presently 10 meters per hour; higher velocities would require the use of multiple dispensing nozzles. As the components arrive at the inclined web a uniform distribution and sampling of the receptors is desired. The depicted process depends primarily on gravity driven sedimentation causing sliding and tumbling along the inclined web which can be adjusted using the inclination angle, typically 10 degree was favorable for the chip size used in the reported experiments. In addition, the web can be vibrated at a desired amplitude and frequency through an up-and-down motion of the lower roller which is one of the parameters that will be discussed in the results section. This additional gentle vibration aids in the

spreading of the components and the removal of access components at the turning point of the web.

Reintroduction of access component at the top of the web requires either a pumping or conveyor belt type approach. The use of a normal mechanical pump such as rotary pump or diaphragm pump located in between the collection point and the dispensing nozzle failed as it led to mechanical damage to the semiconductor chips. The working alternative required the coupling of a mechanical pump (QV variable speed pump, Fluid metering, Inc., NY) with the illustrated custom made jet pump (Figure 1C). The jet pump approach uses a smaller diameter nozzle (1.48 mm^2 in our design) to accelerate the carrier fluid into a desired direction; we typically use a velocity of 25 cm s^{-1} in the upward passage (20 mm^2 tubing) to drag the fairly dense semiconductor chips (density of 2.33 g cm^{-3} , versus 1.0 g cm^{-3} of water) upward to the dispensing head. Beyond this point the previously described gravity based sedimentation takes over again to determine the transport of the components finishing the cycle.

Figure 2 represents the self-assembly results testing a single component size and various receptor designs. The goal was to find out if (i) the location of the receptors on the substrate with respect to the edge of the substrate would present a challenge and cause an increase in the number of defects, (ii) if the orientation with respect to the component flow would matter, or (iii) if the self-assembly process would only support a certain pitch. In general terms we did not see a clear trend suggesting that the self-assembly process would prefer a certain pattern which means that the process is fairly robust enabling arbitrary and ordered assemblies at a desired pitch. In terms of yield the following numbers were found: Figure 2A shows 820 assembly sites, there were no missing and no excess chips present but 6 misaligned components reducing the yield to 99.3%; the misalignment was mainly due to an error in the solder bump height on 6 out of the 820 sites which is a limitation of manual dip-coating process that is currently used to fabricate the solder bumps.^[37] An excessive solder height will lead to captured chips with variation in the tilt angle. In our experiments we used solder bumps that were $70 \text{ }\mu\text{m}$ tall as measured in the center of the bump leading to a tilt angle variations of approximately 0.7° . A lower thickness can reduce the tilt angle variations but would require a more involved process to apply the solder bumps.

This implies that the observed misalignments are not an integral part of the assembly system itself. Figure 2B depicts assembly results using arbitrary test patterns – a skeleton (left top), a walking person (left bottom), space invaders (right), and characters (bottom). The digitized patterns maintain the same pitch/or gap between nearest neighbors but have fewer numbers of assembled parts per area, specifically 29.8%, 41.9%, 49.1%, and 52.9% of the parts per area in (A). The question was to test if an irregular population would be somewhat more fragile than a regular population which was not the case. No defects were present in these assemblies. Figure 2C (upper half) represents a test using a hexagonal lattice where the spacing ($340 \text{ }\mu\text{m}$) to the nearest neighbor/chip becomes smaller than the chip size ($500 \text{ }\mu\text{m}$); this condition has been a challenge in previous reports^[28] where an increase in chip entrapment in between such closely spaced receptors was reported; previous

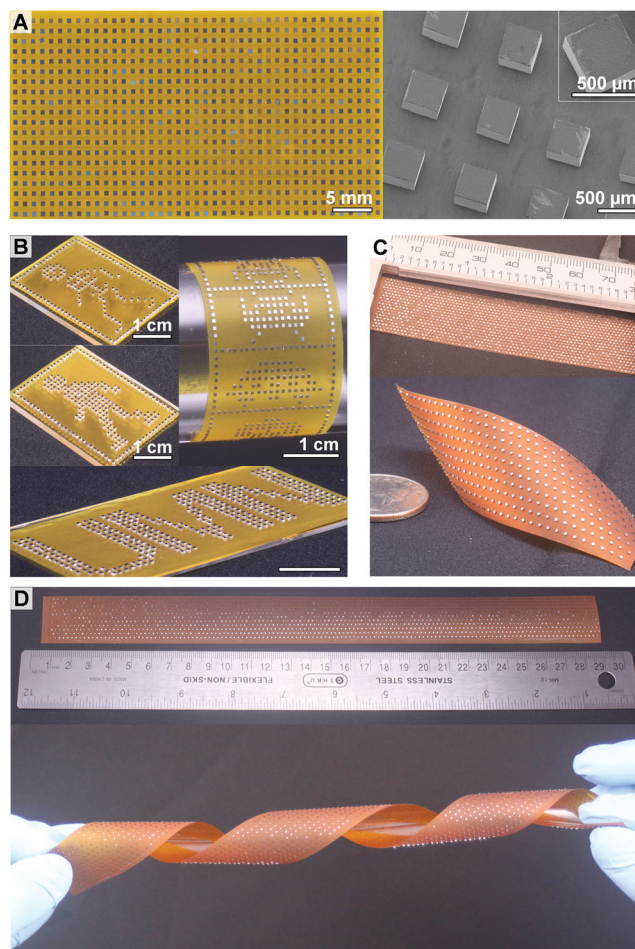


Figure 2. Micrographs depicting assemblies of $500 \text{ }\mu\text{m}$ wide Si chips testing periodic and arbitrary chip assemblies with different densities. (A) Periodic assembly onto 1.1 mm pitched square lattice points, 820 chips, 6 defects. (B) Arbitrary assemblies representing a skeleton, a walking person, space invaders, and letters; in total 1163 chips no defects. (C) Periodic assemblies onto hexagonally located lattice points on a 1.05 mm (top, 1396 chips, 7 defects) and 4.2 mm pitch (bottom, 365 chips, 1 defect). (D) Overview depicting continuous assembly onto a 2 cm wide and 29 cm long assembly region.

reports used a hand agitated drum like assembly approach and a slurry of access components which slid along the surface causing stronger shear forces and entrapment in between closely spaced receptors; this is no longer the case in the automated RTR assembly system where only a desired fraction of the chips interact with the assembly region causing less disturbance and defects (Figure 2C top shows 1396 assembly sites, 6 misalignments and 1 missing chip, representing a yield of 99.5%); Figure 2C bottom is the lower density counterpart with 365 assembly sites, one misaligned chip, 99.7% yield. In terms of overall numbers we are encouraged by the high yield since this begins to exceed deterministic robotic pick-and-place-like assembly methods that manipulate individual chips and that are at least an order of magnitude slower. Figure 2D depicts a 29 cm long and 2 cm wide assembly region with 1524 chips which took 6 minutes to assemble, 2 missing and 4 misaligned components were found in this sample representing a yield of

99.6%. We did not observe a variance of the reported yield numbers across the areas which suggest that a single nozzle is sufficient to disperse the components across a 2 cm wide assembly zone. However, much wider webs are likely going to require an array of nozzles. We have not yet established the limits of the self-assembly process in terms of chip sizes that can be assembled. At this point we have done a few experiments that suggest that the process is capable to assemble 300 to 1000 μm sized chips with a thickness in the range of 200 to 500 μm . Preliminary tests assembling 500, 700, and 1000 μm sized Si chips are shown in Figure S1.

The results presented previously (Figure 2) were based on optimized operational conditions of the system considering component spreading on the web, component attachment on the web, and removal of access components. The operational conditions were carefully determined through the calculation of the relevant forces and experimental validations as summarized in Figure 3. Substrates with a constant 1.1 mm pitch (defined as the center-to-center distance between chips) were used in our experimental validation of the theory and optimization of the process parameters.

Figure 3A depicts the relevant force components, specifically (i) The Surface-tension-based-restoring-force of a molten solder ($F_{s,t} = 2 * Sx$); the equation is valid if the chip is pulled

out of alignment in the tangential direction to a point where the amount of misalignment exceeds the solder thickness.^[29] The tangential restoring force is approximately 400 μN considering the 0.5 mm cube and 400 mN m^{-1} surface tension (S) of the solder; the chips in the illustrations are pulled out of alignment due to a gravitational force or drag force; actual misalignments are much smaller than what is illustrated. (ii) The tangential gravitational forces ($F_{t,g} = g(\rho_{\text{chip}} - \rho_{\text{liq}})x^3 \sin \theta$) on angled web is approximately 1.7 $\mu\text{N} \cdot \sin \theta$ for a 0.5 mm Si cube (0.3 μN for 10° tilted web). (iii) The non-specific adhesion forces ($F_{\text{non-specific adhesion}} = g(\rho_{\text{chip}} - \rho_{\text{liq}})x^3 \sin \theta_{\text{crit}}$) due to static friction, surface tension, Van-der-Waals forces of the semiconductor chips on the polyimide web is important since these forces impacts the amount of spreading of the chips. For a 0.5 mm Si cube, this non-specific adhesion forces is 1.5 μN with critical angle ($\theta_{\text{crit}} = 60^\circ$, experimentally observed) which is the required angle to cause siding motion of previously static chips on the web; at this angle, the gravitational forces start to exceed the non-specific-adhesion. (iv) The inertial force due to the harmonic web oscillation with amplitude A and frequency f ($F_{n,i} = (\rho_{\text{chip}} - \rho_{\text{liq}})x^3 A(2\pi f)^2$); this equation is valid in the regime where the chips remain in contact with the web. (v) The fluid drag forces ($F_D = 0.5\rho_{\text{liq}}x^2 C_D V^2$) due to the oscillating shear flow originated from up-and-down vibrational motion of the web;

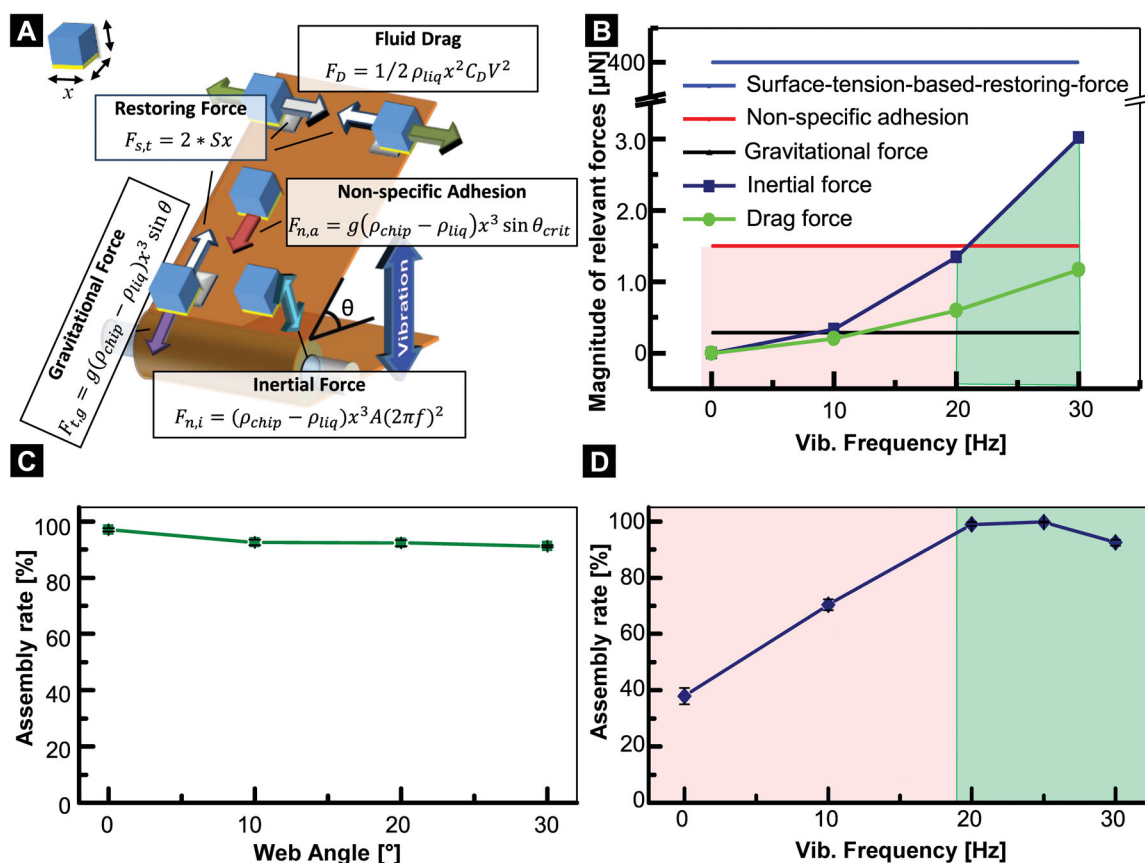


Figure 3. Optimization of the relevant forces and experimental validations. (A) Relevant forces due to surface tension, gravity, non-specific adhesion, inertia and fluid drag; the inertia and fluid drag are a result of an up-and-down vibrational web motion. (B) Comparisons of relevant force components with different vibration conditions. Experimental validation and optimization scheme studying the (C) assembly rate as a function of web angles, (D) assembly rate as a function of vibrational frequency.

the quadratic drag equation^[30] needs to be used rather than Stoke's drag since the calculated Reynolds number exceeds 100 considering a 0.5 mm Si cube in water. To calculate the drag force, we assumed that the shear flow velocity (V) is comparable to oscillating speed of web ($A \cdot 2\pi f$). For example, a 0.5 mm 30 Hz vibration represents a peak velocity of 100 mm s^{-1} and a drag force of approximately $1.3 \text{ }\mu\text{N}$.

Figure 3B compares the relevant force components that act onto the chips in our system as the vibration frequency is increased from 0 to 30 Hz; all calculations assume a Si cube with a side length $x = 0.5 \text{ mm}$, an optimized 10° tilt angle, and an optimized 0.5 mm vibration amplitude. The horizontal lines represent non-specific-adhesion, gravity, and surface tension based restoring force; the green and blue lines represent fluid drag and inertial force which both increase with web vibration frequency. At low frequencies (red regime), the chips are predicted to remain in contact with the web since the non-specific-adhesion (a few μN) and the gravitational force push the components in contact ($1.7 \text{ }\mu\text{N} \cdot \cos(\theta)$), this condition is not desired since the chips reside in one point and do not move around to participate in the self-assembly; this general behavior is observed in the experiments. At 20 Hz (green regime begins) the inertial force that acts on the components is predicted to become sufficiently strong to overcome gravity; separation and hopping of components should begin to occur. The actual hopping is difficult to observe in the experiments, however, the onset of a collective downward sliding motion that leads to a sampling of the receptors occurs once the 20 Hz is reached in our experiments. Once the downward motion takes place the chips show a small sideways oscillatory motion which can be explained by the pulsating liquid drag. The calculated dependencies have clear implications on the assembly rate and yield which can now be directly measured and understood:

First, we recorded the effect of gravity on the assembly rate (Figure 3C) testing various tilt angles. In each consecutive experiment (5 experiments per data point) we recorded the number of captured components for a constant assembly time of 3 minutes using a constant level of web vibration (0.5 mm amplitude and 30 Hz frequency). A depicted value of 98% means that 98% of the receptors captured a chip within 3 minutes leaving 2% of the receptors vacant. The capture rate decreases slightly towards higher tilt angle since the chips begin to slide too fast; some slide over a solder bump and are not immediately captured.

Second, and in analogy to the predictions made in Figure 3B we recorded the effect of vibration frequency (0–30 Hz) (Figure 3D) in consecutive experiments (5 experiments per data point) maintaining constant vibration amplitude (0.5 mm) and tilt angle (10°). The green and red regimes can be found again. As predicted at low vibration frequency (0–10 Hz, red regime), the progression of the self-assembly was slow and non-uniform. A portion of the chips remains stationary because the agitation is insufficiently strong to overcome non-specific-adhesion and gravity; most of the assembly takes place towards the center of the web due to an insufficient spreading. At 20 to 25 Hz the progression of the self-assembly reaches an optimized value (green regime), the chips are distributed uniformly across the surface and slide slowly in one direction is supported by the calculations made above.

We have also adjusted the tilt angle and vibration amplitudes. Without going into the details we would like to point out that 10° represents an optimized tilt angle. Higher values lead to a faster sliding motion which in turn reduced the capturing rate since more chips slid over a solder bump before being captured. This should be investigated further in the future. Equally the 0.5 mm vibration amplitudes represented an optimized value for the chip size used in this study. Higher amplitudes lead to lateral oscillatory motion of the chips which exceeded the size of the solder bumps which in turn reduced the capturing rate. We think that more research is required. However, the goal so far was to demonstrate that perfect functional assemblies can be produced and that processes of self-assembly can exceed the yield of conventional deterministic manufacturing such as serial robotic pick and place. This goal has been reached using the presented parameters and we are convinced that the process can be tailored to various applications. Of particular interest are applications where low cost and assembly of objects in large quantities is desired. One example is briefly discussed below.

Figure 4 provides one example where the process is applied to the assembly of GaN LEDs targeting an application in the cost effective production of area lighting modules on the basis of distributed solid state light sources. We used LEDs, unpackaged n-GaN/p-GaN thin LEDs with a side length of $500 \text{ }\mu\text{m}$ and a height of $190 \text{ }\mu\text{m}$ (F4142L, OSRAM) as device segments. As shown in Figure 4A, the area lighting modules are fabricated in three steps: (i) assembly of LEDs on the bottom electrode using the RTR system, (ii) isolation and passivation of assembled LEDs with UV curable polymer, and (iii) lamination of top conductive layer to complete the electrical connections.

First, for the successful assembly of the LEDs (Figure 4B, top) the following conditions were used. The substrates were identical to the ones used above with the exception that each pad is connected to an interconnecting line. The interconnecting lines are protected with a dry film to prevent solder wetting and assembly of LEDs in this region; see materials and methods sections for more details. A higher vibrational amplitude (2–3 mm) was required when compared to the Si components; the reason is that the LED has a gold top contact; the gold top contact is 25 times smaller than the bottom contact; however, attachment with the wrong orientation can occur under the wrong conditions. This was prevented using a higher vibrational amplitude.

Second, after assembly a UV curable polymer (NOA 73, Norland Optical Adhesive, NJ) is used as a separation layer between the top and bottom contact (Figure 4B, bottom). To apply this isolation layer we first place a polydimethylsiloxane (PDMS, Sylgard 184, Dow Corning Co.) block on the assembled LEDs to protect the topside of the LEDs. The matrix in between is subsequently filled using a UV curable polymer through capillary action. Unfortunately, this process is not perfect and polymer residues can be present on the top of the LEDs which need to be removed using O_2 plasma cleaning step (60 seconds). More details are described in materials and method sections.

The third step of the fabrication procedure is a lamination step whereby the top conductive layer is applied. The third step is a new approach which has not yet been optimized. The goal was not to use an evaporation step or wire-bonding but to find

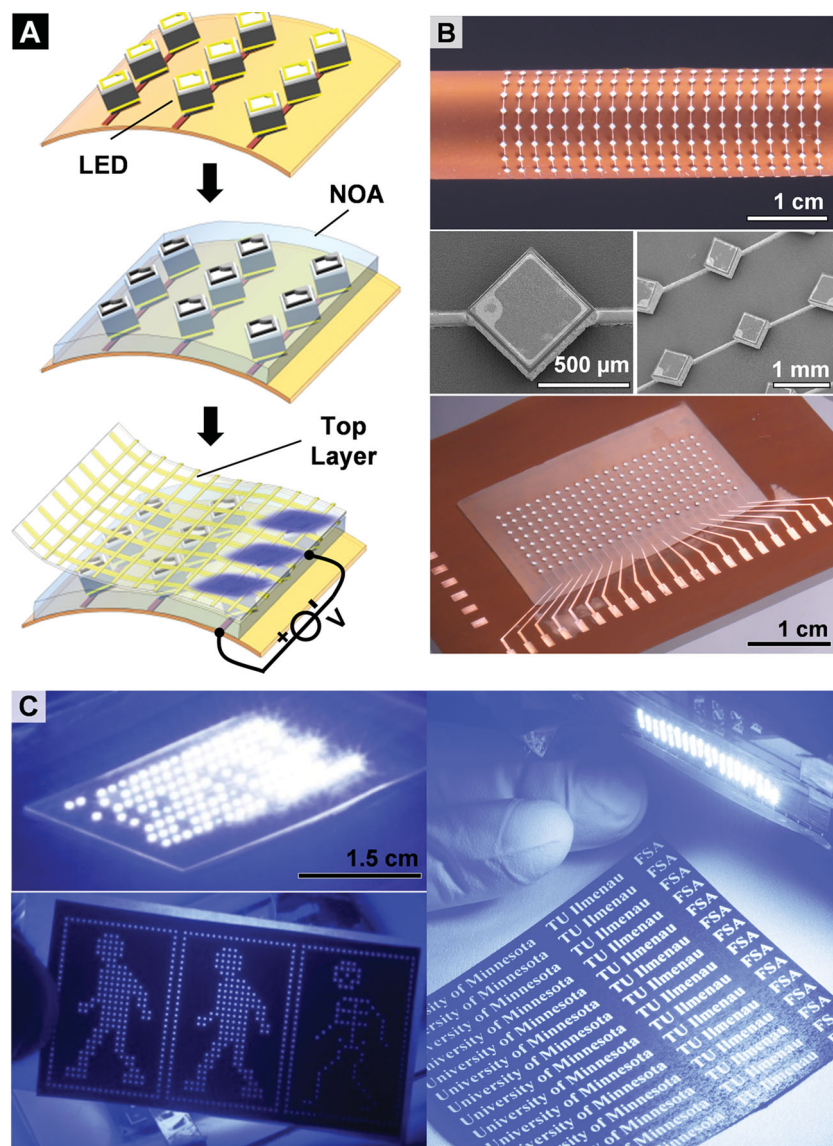


Figure 4. RTR fluidic self-assembly system applied to the fabrication of area lighting modules. (A) Fabrication procedure: assembly of LED using the RTR fluidic self-assembly system, area isolation and passivation of assembled LEDs with UV curable polymer (NOA), and lamination of top conductive layer. (B) Optical photograph of assembled LEDs wrapped onto a cylinder (top), SEM close-ups (middle), and optical photograph after isolation using UV curable polymer (bottom). (C) Application as lighting panel (left, top), backlighting unit (left, bottom), and area illumination unit (right).

an alternative contacting method that would not require any vacuum processing in the long run. The approach was in part inspired by the ability to form a conformal electrical contact by simply placing a metal coated polymeric material (for example a gold-coated PDMS stamp with correct thickness) onto the surface that needs to be electrically contacted; we demonstrated that this is possible in the past,^[31] and the approach has later been used in a modified form by others to contact and transfer metal contacts on secondary surfaces.^[1,2,32] A problem with the original method is that the adhesive force is primarily based on Van-der-Waals adhesion which cannot be tailored to be as large as one would like in certain applications. Instead of transferring

a metal contact onto the surface we decided to test a two-phase-material approach where portions of the surface are adhesive (and less conductive) and other portions are conductive (and less adhesive) to tailor the properties to desired levels. In the simplest form, the approach can be described to make use of a metallic mesh (Figure 4A, bottom) which is surrounded by an adhesive surface whereby the adhesive is used to maintain a close contact to the surface of the LEDs; once attached the conducting traces remain fixed in place through the surrounding adhesive. The problem of alignment can be circumvented by choosing a mesh periodicity which is smaller than the widths of the contact pad on the top of the LEDs (100 μm in our design). To test this new contacting scheme a 7 cm \times 7 cm wide gold mesh is fabricated using standard photolithography involving evaporation of 250 nm thick layer of gold without adhesion layer on a bare Si wafer, wet chemical etching, and final transferred to a clear commercially available tape (3 M Scotch tape, 3 M). The resulting conducting tape is then applied to contact the top of the LEDs. Figure 4C provides images of functional arrays that have been produced so far. The approach has not yet been optimized and the results are not perfect as a consequence; most LEDs light up (~90%) but some can be found where no contact was made (Figure 4C). The optimization of the top contact is outside of the focus of the sponsored research project dealing with self-assembly. Anyway it would be interesting to test various pitches and metal thicknesses. In the long term it would be required to have a simple contacting scheme to provide a more cost effective alternative to conventional serial wire-bonding. Nevertheless, we have also tested standard wire-bonding and were able to produce defect free lighting modules Figure S2.

This publication provides the blueprints and operational parameters of a first RTR fluidic self-assembly platform to assemble and electrically connect semiconductor chips with a yield clearly exceeding a 99% benchmark set by robotic pick and place machines. At present the installed apparatus supports an assembly rate of ~15 k chips per hour using a 2.5 cm wide web testing standard square shaped dies 500 μm in size; scaling to 150 k chips per hour would require a 25 cm wide web. The technology is completely different from conventional deterministic robotic assembly and the industry that develop around it. Most importantly the fluidic self-assembly approach is entirely parallel and does not require any pick and place operations. This means that it is fairly straightforward to scale this technology to any desired assembly rate by increasing the substrate width

and number of nozzles. We are convinced that the key to the high yield and high alignment accuracy is inherently related with the high restoring force of liquid solder bumps that we continue to use in our experiments. Over many years we have experimented with other forces including Coulomb forces,^[33] hydrophobic and hydrophilic forces,^[34] magnetic (not published), gravity and shape recognition and we have yet to find another approach that achieves a similar yield and alignment accuracy. The approach can be extended using shape recognition concepts to enable unique angular alignment and contact pad registration^[5,9,27] or using sequential batch assembly processes^[7,35] to assemble more than one component type on the substrate if desired. Moreover, it is possible to transfer the chip onto other flexible or stretchable substrates. It should also be possible to extend this scheme towards smaller chips sizes in the future.

Experimental Section

Si components: 500 μm in lateral size Si components were fabricated using 200 μm thick Si wafers (University Wafers, Boston, MA) that were first cleaned using a standard RCA clean: 1:1:5 solution of $\text{NH}_4\text{OH} + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$ at 80 $^\circ\text{C}$ for 15 min; 1:50 solution of $\text{HF} + \text{H}_2\text{O}$ at 25 $^\circ\text{C}$ for 15 s; 1:1:6 solution of $\text{HCl} + \text{H}_2\text{O}_2 + \text{H}_2\text{O}$ at 80 $^\circ\text{C}$ for 15 min with a DI water rinse after each step. Following the clean, 10 nm Cr and 200 nm Au layers was deposited using an e-beam evaporator. Photoresist (Microposit 1813, Shipley) was then spin coated at 3000 rpm for 30 s. After a soft-bake at 105 $^\circ\text{C}$ for 1 min, the substrate was exposed with 90 mJ/cm^2 UV light and developed in 1 Microposit 351 : 5 H_2O developer for 25 s. The Au and Cr layers were subsequently wet-etched using a gold etchant (GE-6, Transene Inc, MA) for 45 s and a chromium etchant (CR-12S, Cyantek Corp., CA) for 5 s, respectively. The photoresist was removed using a reactive ion etch (O_2 , 100 sccm, 100 W, 100 mTorr). Finally, the wafer was diced using a fully automated dicing machine. To prevent damage and contaminations, the gold contact was protected with a photoresist (Microposit 1813, Shipley) during the dicing step.

Self-Assembly Substrate: A copper clad conventional flexible printed circuit board material is the starting material (Pyrulux LF series, DuPont, NC). The 20 μm thick Cu cladding is cleaned with a 1 HCl : 10 DI water solution, DI water, methanol, acetone, isopropyl alcohol. Dry film (Optical resist, Alpha 300, Megauk, UK) is laminated on the top using a tension controlled laminator at 95 $^\circ\text{C}$ with 250 kPa, exposed with 55 mJ/cm^2 UV light through a transparency mask, and developed in 2% K_2CO_3 in room temperature for 50 s. Following the development, the unprotected copper is removed through etching in a 30% FeCl_3 solution in 5 min. The dry film is stripped in a 4% KOH solution at 40 $^\circ\text{C}$ leaving bare copper squares (receptors) on the substrates. The substrate is rinsed in DI water. Finally, the copper pads are coated using a low melting point solder (Indalloy #117, MP. 47 $^\circ\text{C}$, Indium Corp., NY) through dip coating in a preheated solder bath in order to realize the predefined receptors; the solder bath contains a layer of water on top of the heavier solder to prevent oxidation of the solder. Drops of HCl can be added to the water covering the liquid solder to remove any surface oxides on the solder if present. The surface of the liquid solder should be mirror like.

SSL application – Bottom electrode: The fabrication of the bottom electrode follows the lithographic procedure above with the exception that a second layer of dry film and lithography is used to protect the electrical interconnection line from being coated with solder during the dip coating process.

SSL application – Isolation using NOA: Following self-assembly of LEDs, a fully cured PDMS (Sylgard 184, Dow Corning Co.) stamp was placed on the top of assembled LED array under moderated pressure. UV curable polymer (NOA 73, Norland Optical Adhesive, NJ) was

dispensed on the side of PDMS stamp to fill the gap on the basis of capillary action. The NOA was cured under UV light. NOA residues were found on some of the LEDs which required a de-scum using a reactive ion etcher for 60 s (CF_4 : 20 sccm, O_2 : 80 sccm, 200 W).

SSL application – Top Electrode Lamination Layer: 250 nm Au was deposited using an e-beam evaporator onto a bare Si wafers (University Wafers, Boston, MA) that was previously cleaned in a solution of $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$ for 15 min and rinsed with DI water. No adhesion promoter was used. Photoresist (Microposit 1813 Shipley) is applied (4000 RPM), exposed, and developed in Microposit 351 : 5 H_2O developer (25 s). The Au layer is etched in a gold etchant (GE-6, Transene Inc, MA) for 50 s, washed in isopropyl alcohol, and carefully dried. The patterned Au mesh is transfer printed onto a clear adhesive tape (3M scotch tape) which is then used to contact the top of the LEDs through lamination.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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