Curriculum Vitae:

Kiarash (Kia) Bazargan

Department of Electrical and Computer Engineering
University of Minnesota
4-178 Keller Hall
200 Union Street SE
Minneapolis, MN 55455
(612) 625-4588
kia@umn.edu
http://umn.edu/~kia

Professional Preparation

- **2000, PhD**, Electrical and Computer Engineering, Northwestern University, Evanston, IL.
  Thesis title: "Designing CAD Tools for Reconfigurable Computing Systems",
  Advisor: Prof. Majid Sarrafzadeh.
- **1998, MSc**, Electrical and Computer Engineering, Northwestern University, Evanston, IL.
  Thesis title: "Floorplanning in Deep Submicron Under Uncertainty",
  Advisor: Prof. Majid Sarrafzadeh.
- **1996, BS**, Computer Science, Sharif University of Technology, Tehran, Iran.

Appointments

- **September 2006 – present**: Associate Professor, Department of Electrical and Computer Engineering, University of Minnesota.
- **Aug 2000 – Aug 2006**: Assistant Professor, Department of Electrical and Computer Engineering, University of Minnesota.
- **Jan. 1997 -- July 2000** Research Assistant, Northwestern University, Evanston, IL.
- **June 1998 -- Sep. 1998** Summer intern, Monterey Design Systems, Sunnyvale, CA. Developed a timing-driven hierarchical floorplanning algorithm that utilizes simulated annealing as its core engine.

Publications

Journal Publications

(Kia's students are marked with an asterisk*)

J1. Peng Li, David Lilja, Weikang Qian, Marc D. Riedel, Kia Bazargan, "Logical Computation on Stochastic Bit Streams with Linear Finite State Machines" , in IEEE Transactions on Computers, Vol. 63, No. 6, pp. 1473-1485, June 2014.

J2. Peng Li, David J. Lilja, Weikang Qian, Marc Riedel and Kia Bazargan, "Computation on Stochastic Bit Streams: Digital Image Processing Case Studies", IEEE Transactions on Very Large Scale Integration Systems, Vol 22, No 3, pp. 449-462, 2014.

J3. Weikang Qian, Xin Li, Marc D. Riedel, Kia Bazargan, and David J. Lilja, "An architecture for fault-tolerant computation with stochastic logic," in IEEE Transactions on Computers, vol. 60, no. 1, pp. 93-105, 2011.

J4. Pongstorn Maidee* and Kia Bazargan, "Improvements on Efficiency and Efficacy of SPFD-Based Rewiring for LUT-Based Circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 29 (12), pp. 1870 - 1883, 2010.

J5. Hushrav D Mogal*, Haifeng Qian, Sachin S Sapatnekar and Kia Bazargan, "Fast and Accurate Statistical Criticality Computation under Process Variations", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 28(3): 350-363, 2009

J6. Satish Sivaswamy* and Kia Bazargan, "Statistical Analysis and Process Variation-Aware Routing and Skew Assignment for FPGAs", ACM Transactions on Reconfigurable Technology and Systems, Mar 2008

J7. Gang Wang, Satish Sivaswamy*, Cristinel Ababei*, Kia Bazargan, Ryan Kastner and Eli Bozorgzadeh, “Statistical Analysis and Design of HARP Routing Pattern FPGAs”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, pp. 2088-2102, Vol. 25, No. 10, October 2006. [contribution: major]

J8. Cristinel Ababei*, Yan Feng, Brent Goplen, Hushrav Mogal*, Tianpei Zhang, Kia Bazargan, and Sachin S. Sapatnekar, “Placement and Routing in 3D Integrated Circuits”, IEEE Design & Test of Computers, to appear. [contribution: equal]

J9. Jinghuan Chen, Kia Bazargan, and Jaekyun Moon, “A Reconfigurable FPGA-Based Readback Signal Generator for Hard-Disk Read Channel Simulator”, IEEE Transactions on Very Large Scale Integration Systems, under review. [contribution: major]

J10. Ying Chen, Karthik Ranganathan*, Vasudev V Pai*, David J. Lilja, and Kia Bazargan, "A Novel Memory Structure for Embedded Systems: Flexible Sequential and Random Access Memory", Journal of Computer Science and Technology (JCST), 2005. [contribution: minor]

J11. Cristinel Ababei*, Hushrav Mogal*, and Kia Bazargan, "Three-dimensional Place and Route for FPGAs", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, to appear.

J12. P. Maidee*, C. Ababei* and K. Bazargan, “Timing-driven Partitioning-based Placement for Island Style FPGAs”, IEEE Transactions on Computer Aided Design, Vol. 4, No. 3, pp. 1744 - 1750, Mar 2005.

J13. C. Ababei* and K. Bazargan, "Non-Contiguous Linear Placement for Reconfigurable Fabrics", International Journal of Embedded Systems, esp. issue on Reconfigurable Architectures Workshop (RAW), Inderscience Publishers, 2004.

J14. J. Chen, J. Moon and K. Bazargan, “FPGA-based Reconfigurable Generation of Readback Signals”, IEEE Transactions on Magnetics, Vol. 4, No. 3, pp. 1744 - 1750, May 2004. [contribution: equal]

J15. A. Ranjan, K. Bazargan, S. Ogrenci and M. Sarrafzadeh, "Fast Floorplanning for Effective Prediction and Construction ", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 9, Issue 2, pp. 341-351, April 2001.

J16. K. Bazargan, R. Kastner and M. Sarrafzadeh, "3-D Floorplanning: Simulated Annealing and Greedy Placement Methods for Reconfigurable Computing Systems", *Design Automation for Embedded Systems (DAfES) - RSP'99 Special Issue*, April 2000.

J17. K. Bazargan, R. Kastner and M. Sarrafzadeh, "Fast Template Placement for Reconfigurable Computing Systems", *IEEE Design and Test - Special Issue on Reconfigurable Computing*, pp. 68-83, January-March 2000.

J18. K. Bazargan, S. Kim and M. Sarrafzadeh, "Nostradamus: A Floorplanner of Uncertain Designs", *IEEE Transactions on Computer-Aided Design (TCAD)*, pp. 389-397, April 1999.

Book Chapters

B1. Weikang Qian, Marc D. Riedel, Kia Bazargan, and David J. Lilja, "Synthesizing combinational logic to generate probabilities: theories and algorithms," in *Advanced Techniques in Logic Synthesis, Optimizations and Applications*, Sunil Khatri and Kanupriya Gulati editors, Springer Publishing, 2011.

B2. Kia Bazargan, "Chapter 10.2: FPGA Technology Mapping, Placement, and Routing", in *The Handbook of Algorithms for VLSI Physical Design Automation*, Charles J. Alpert, Dinesh P. Mehta, and Sachin S. Sapatnekar, CRC Press.

B3. Sachin Sapatnekar, Kia Bazargan, "Chapter 10.4: 3D Design", in *The Handbook of Algorithms for VLSI Physical Design Automation*, Charles J. Alpert, Dinesh P. Mehta, and Sachin S. Sapatnekar, CRC Press.

Refereed Conference Publications

(Presenter's name is underlined, Kia's students are marked with an asterisk*)

C1. Naman Saraf*, Kia Bazargan, David Lilja and Marc Riedel, "IIR Filters Using Stochastic Arithmetic", Design, Automation and Test in Europe (DATE), 2014.

C2. Yanzi Zhu*, Peiran Suo* and Kia Bazargan, "Binary Stochastic Implementation of Digital Logic", International Symposium on Field-Programmable Gate Arrays (FPGA), 2014. *Full paper acceptance rate: 17.4%*.

C3. Naman Saraf*, and Kia Bazargan, "Sequential Logic to Transform Probabilities", International Conference on Computer-Aided Design (ICCAD), 2013.

C4. Naman Saraf*, Kia Bazargan, David Lilja, and Marc Riedel, "Stochastic Functions Using Sequential Logic", International Conference on Computer Design (ICCD), 2013.

C5. Peng Li, David J. Lilja, Weikang Qian, Kia Bazargan and Marc Riedel, "The Synthesis of Complex Arithmetic Computation on Stochastic Bit Streams Using Sequential Logic", *International Conference on Computer-Aided Design (ICCAD)*, 2012.

C6. Weikang Qian, Chen Wang, Peng Li, David J. Lilja, Kia Bazargan, and Marc D. Riedel, "An Efficient Implementation of Numerical Integration Using Logical Computation on Stochastic Bit Streams", International Conference on Computer-Aided Design (ICCAD), 2012.

C7. Peng Li, David J. Lilja, Weikang Qian, Kia Bazargan, and Marc Riedel, "Using Two-Dimensional Finite State Machine for Stochastic Computation", IWLS, 2012.

C8. Peng Li, Weikang Qian, Marc D. Riedel, Kia Bazargan, and David J. Lilja, "The Synthesis of Linear Finite State Machine-Based Stochastic Computational Elements", Asia and South Pacific Design Automation Conference (ASP-DAC), 2012.

C9. Peng Li, Weikang Qian, David J. Lilja, Kia Bazargan, and Marc D. Riedel, "Case Studies of Logical Computation on Stochastic Bit Streams", PATOMAs, invited.

C10. Pongstorn Maidee* and Kia Bazargan, "A Fast SPFD-based Rewiring Technique", *Asia South-Pacific Design Automation Conference (ASPDAC)*, 2010.

C11. Weikang Qian*, Marc Riedel, Kia Bazargan, and David Lilja, "The Synthesis of Combinational Logic to Generate Probabilities", *International Conference on Computer-Aided Design (ICCAD)*, San Jose, 2009.

C12. Xin Li, Weikang Qian, Marc D. Riedel*, Kia Bazargan, and David J. Lilja, "A Reconfigurable Stochastic Architecture for Highly Reliable Computing", Great Lakes Symposium (GLSVLSI), 2009.

C13. Hamid Safizadeh, Mohammad Tahghighi, Ehsan Ardestani, Gholamhossein Tavassoli, and Kia Bazargan, "Paradigm Shift: Using Randomized Algorithms to Cope with Circuit Uncertainty", Design Automation & Test in Europe (DATE), 2009.

C14. Satish Sivaswamy*, Kia Bazargan, and Marc Riedel"Estimation and Optimization of Reliability of Noisy Digital Circuits", International Symposium on Quality Electronic Design (ISQED), 2009.

C15. Hushrav Mogal*, and Kia Bazargan, "Thermal-Aware Floorplanning for Task Migration Enabled Active Sub-threshold Leakage Reduction", International Conference on Computer-Aided Design (ICCAD), 2008.

C16. Pongstorn Maidee*, Nagib Hakim and Kia Bazargan, "FPGA Family Composition and Effects of Specialized Blocks", International Conference on Field Programmable Logic and Applications (FPL), 2008.

C17. Hushrav Mogal*, Haifeng Qian, Sachin Sapatnekar and Kia Bazargan, "Clustering Based Pruning for Statistical Criticality Computation under Process Variations", *International Conference on Computer-Aided Design (ICCAD)*, 2007.

C18. Pongstorn Maidee* and Kia Bazargan, "A Generalized and Unified SPFD-based Rewiring Technique", *17th International Conference on Field Programmable Logic and Applications (FPL)*, 2007

C19. Satish Sivaswamy* and Kia Bazargan, "Statistical Generic And Chip-Specific Skew Assignment for Improving Timing Yield of FPGAs", *17th International Conference on Field Programmable Logic and Applications (FPL)*, 2007

C20. Satish Sivaswamy* and Kia Bazargan, "Variation-AwareRoutingforFPGAs", *International Symposium on Field Programmable Gate Arrays (FPGA)*, 2007.

C21. Hushrav Mogal* and Kia Bazargan, "Microarchitecture Floorplanning for Sub-threshold Leakage Reduction", Design and Test in Europe (DATE), 2007.

C22. Pongstorn Maidee* and Kia Bazargan, "Defect-tolerant FPGA Architecture Exploration" , 16th International Conference on Field Programmable Logic and Applications (FPL), 2006.

C23. Satish Sivaswamy*, Gang Wang, Cristinel Ababei*, Kia Bazargan, Ryan Kastner, Eli Bozorgzadeh, "HARP: Hardwired Routing Pattern FPGAs", International Symposium on Field Programmable Gate Arrays (FPGA), 2005.
[full paper acceptance rate: 24 out of 97] [contribution: major]

C24. C. Ababei*, H. Mogal*, and K. Bazargan, "3D FPGAs: Placement, Routing and Architecture Evaluation", International Symposium on Field Programmable Gate Arrays (FPGA), (poster), 2005.

C25. C. Ababei*, H. Mogal*, and K. Bazargan, "Three-dimensional Place and Route for FPGAs", Asia South-Pacific Design Automation Conference (ASPDAC), 2005.
[full paper acceptance rate: 14%]

C26. C. Ababei*, and K. Bazargan, "Exploring Potential Benefits of 3D FPGA Integration", Field-Programmable Logic and its Applications (FPL), 2004.

C27. Y. Chen, K. Ranganathan*, V. V. Pai*, D. Lilja and K. Bazargan, "Enhancing the Memory Performance of Embedded Systems with the Flexible Sequential and Random Access Memory", Asia-Pacific Computer Systems Architecture Conference (ACSAC), 2004.
[contribution: major]

C28. W. Choi* and K. Bazargan, "Incremental Placement for Timing Optimization", *International Conference on Computer-Aided Design (ICCAD)*, 2003.
[acceptance rate: 26.32% [1]]

C29. C. Ababei* and K. Bazargan, "Placement Method Targeting Predictability, Robustness and Performance", *International Conference on Computer-Aided Design (ICCAD)*, p., 2003.
[acceptance rate: 26.32% [1]]

C30. P. Maidee*, C. Ababei* and K. Bazargan, ***(nominated for the best paper award)***
"Fast Timing-driven Partitioning-based Placement for Island Style FPGAs", *Design Automation Conference (DAC),* pp. 598-603, 2003.
[acceptance rate: 24% [2]]

C31. K. Bhasyam* and K. Bazargan, "HW/SW Codesign Incorporating Edge Delays Using Dynamic Programming", *Euromirco Symposium on Digital Systems Design*, p., 2003.

[1] According to: http://www.cs.binghamton.edu/~oguz/acceptance_rates.html
[2] According to: http://portal.acm.org/browse_dl.cfm?idx=SERIES380

C32. V. K. Marreddy*, S. Noorbaloochi* and and K. Bazargan, "Linear Placement for Static / Dynamic Reconfiguration in JBits", IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), p., 2003. (poster)

C33. W. Choi* and K. Bazargan, "Hierarchical Global Floorplacement Using Simulated Annealing and Network Flow Area Migration", *Design Automation and Test in Europe (DATE)*, p., 2003. (short paper) [acceptance rate: 25.76%]

C34. C. Ababei* and K. Bazargan, "Timing Minimization by Statistical Timing hMetis-based Partitioning", VLSI Design, pp. 58-63, 2003.

C35. C. Ababei*, N. Selva, K. Bazargan and G. Karypis, "Multi-objective Circuit Partitioning for Cutsize and Path-Based Delay Minimization", *International Conference on Computer-Aided Design (ICCAD)*, 2002.
[acceptance rate: 27.55% [2]] [contribution: major]

C36. J. Chen, J. Moon and K. Bazargan, ***(nominated for the best paper award)***
"A Reconfigurable FPGA-Based Readback Signal Generator For Hard-Drive Read Channel Simulator", *Design Automation Conference (DAC)*, pp. 349-354, 2002.
[acceptance rate: 30% [2]] [contribution: major]

C37. C. Ababei* and K. Bazargan, "Statistical Timing Driven Partitioning for VLSI Circuits", Design Automation and Test in Europe (DATE), p. 1109, 2002. (poster)

C38. K. Bazargan, S. Ogrenci and M. Sarrafzadeh, ***(nominated for the best paper award)***
"Integrating Scheduling and Physical Design into a Coherent Compilation Cycle for Reconfigurable Computing Architectures", *Design Automation Conference (DAC),* pp. 635-640, 2000. [contribution: major]

C39. A. Ranjan, K. Bazargan and M. Sarrafzadeh, "Fast Hierarchical Floorplanning with Congestion and Timing Control", *IEEE International Conference on Computer Design (ICCD)*, pp. 357-362, September 2000. [contribution: major]

C40. K. Bazargan, R. Kastner, S. Ogrenci and M. Sarrafzadeh, "A C to Hardware/Software Compiler", IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), pp. 331-332, 2000. (poster) [contribution: major]

C41. K. Bazargan, A. Ranjan and M. Sarrafzadeh, "Fast and Accurate Estimation of Floorplans in Logic/High-level Synthesis", *Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 95-100, March 2000. [contribution: equal]

C42. A. Ranjan, K. Bazargan and M. Sarrafzadeh, "Floorplanner 1000 Times Faster: A Good Predictor and Constructor", in *System-Level Interconnection Prediction (SLIP)*, pp. 115-120, 1999. [contribution: major]

C43. K. Bazargan and M. Sarrafzadeh, "Fast Online Placement for Reconfigurable Computing Systems", *IEEE Symposium on FPGAs for Custom Computing Machines (FCCM)*, pp. 300-302, 1999. (poster)

C44. K. Bazargan, S. Kim and M. Sarrafzadeh, "Nostradamus: A Floorplanner of Uncertain Designs", *International Symposium on Physical Design (ISPD)*, pp. 18-23, 1998.
[contribution: major]

Workshops

(All except SPIE and 3DIC are **peer reviewed**. Presenter's name is underlined, Kia's students are marked with an asterisk*)

W1. Naman Saraf*, and Kia Bazargan, "Design of Sequential Logic to Generate Probabilities", International Workshop on Logic and Synthesis (IWLS), 2013.

W2. Seyyed Ahmad Razavi, Morteza Saheb Zamani, Kia Bazargan, “A Tileable Switch Module Architecture for Homogeneous 3D FPGAs”, IEEE International Conference on 3D System Integration (3D IC), 2009 (poster).

W3. C. Ababei* and K. Bazargan, "Non-Contiguous Linear Placement for Reconfigurable Fabrics", Reconfigurable Architectures Workshop (RAW), p., 2004.

W4. S. Ogrenci, K. Bazargan and M. Sarrafzadeh, "Image analysis and partitioning for FPGA implementation of image restoration", in *Proceedings of the IEEE Workshop on Signal Processing Systems*, pp. 346-355, 2000. [contribution: minor]

W5. K. Bazargan and M. Sarrafzadeh, "Fast Scheduling and Placement Methods for C to Hardware/Software Compilation", SPIE International Symposium on Information Technologies, Vol. 4212, November 2000.

W6. R. Kastner, K. Bazargan and M. Sarrafzadeh, "Physical Design for Reconfigurable Computing Systems using Firm Templates", *Workshop on Reconfigurable Computing (WoRC)*, pp. 19-26, 1999. [contribution: major]

W7. K. Bazargan, R. Kastner and M. Sarrafzadeh, "3-D Floorplanning: Simulated Annealing and Greedy Placement Methods for Reconfigurable Computing Systems", *10th IEEE International Workshop on Rapid System Prototyping (RSP' 99)*, pp. 38-43, 1999. [contribution: major]

Invited Talks

I1. Kia Bazargan, “Beyond Silicon: Randomized Algorithms, Architectures and CAD”, Intel, Santa Clara, CA, Feb 2007.

I2. Satish Sivaswamy, Kia Bazargan, “Pre-routed Patterns for Structured ASIC Designs”, LSI Logic, Bloomington, MN, June 2005.

I3. Kia Bazargan, “3D CAD for FPGAs”, IBM T.J. Watson, NY, Apr 2005.

I4. Kia Bazargan, “Better Field Programmable Gate Arrays (FPGAs)? CAD and Architectural Innovations Will Do the Trick!”, ECE Dept., University of Minnesota, Apr 2005.

I5. Kia Bazargan, "HARP: Hardwired Routing Pattern FPGAs", Xilinx Corporation, San Jose, CA, Feb 2005.

I6. Kia Bazargan, “Partitioning-Based Timing-Driven Placement for 2D and 3D FPGAs”, ECE Dept., Northwestern University, Dec 2003.

Awards

- Recipient of the NSF CAREER award, 2003.
- Best paper award nominee, Design Automation Conference, 2000, 2002, 2003.

Synergistic Activities

- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Dec 2004-2011
- Guest Editor (with John Lach of U of Virginia), ACM Transactions on Embedded Computing Systems (ACM TECS), 2003.
- Member of the Technical Program Committee:
  - ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), 2006-2014
  - Design Automation Conference (DAC), 2007- 2009.
  - Field Programmable Technology (FPT) 2012-2013.
  - Field-programmable Logic and Applications (FPL) 2008-2009.
  - International Conference on Computer Aided Design (ICCAD), 2004, 2003 (and session chair), 2002 (and session chair).

- Asia South-Pacific Design Automation Conference (ASP-DAC), 2005 (and session chair)
- Great Lakes Symposium, 2003, 2002.
- Engineering of Reconfigurable Systems and Algorithms, 2003.
- International Symposium on Physical Design (ISPD), 2002 (and session chair).

- Organizer (2007, 2009) and presenter (2006) of TechTuneup, a 3-day short course at the Electrical and Computer Engineering Dept, University of Minnesota.
- Organizer and presenter of a tutorial in ICCAD'02 titled "FPGAs: Computer-Aided Design, Applications and Future Architectures"
- Participant in "NSF Workshop on Nanocomputing", Carnegie Mellon University. (http://www-2.cs.cmu.edu/~phoenix/nanocomputing/), 2002. The purpose of the workshop was to come up with recommendations for NSF on the best directions the nano technology research should take to get Computer Scientists more involved in research related to nano-technology.
- Participant in various NSF review panels. (CAREER, Physical Design) 2004-2012
- Reviewer of UC Micro proposals 2003, 2005
- *Journal Referee:* Reviewer for:
  - ACM Transactions on Reconfigurable Technology and Systems, 2007-2009, 2013-2014.
  - IEEE Transactions on Computer Aided Design (TCAD) 1999-2014.
  - IEEE Transactions on VLSI Systems (TVLSI) 2003-2009
  - IEEE Transactions on Parallel and Distributed Systems (TPDS) 2000
  - IEEE Transactions on Design Automation of Electronic Systems (TODAES) 2003-2006, 2012-2013
  - IEEE Design and Test of Computers (D&T) 2005
  - IEEE Transactions on Computers (TC) 2005
  - Integration, The VLSI Journal 2004
  - IEEE Transactions on Circuits and Systems (TCAS) 2004-2005
  - ASP Journal of Low Power Electronics (JOLPE) 2005
- *Conference Referee*:
  - Design Automation Conference (DAC) 1998-2005
  - International Symposium on Physical Design (ISPD) 2000, 2001
  - International Conference on Computer-Aided Design (ICCAD) 2002-2004
  - ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA) 2005
  - Engineering of Reconfigurable System Architectures (ERSA) 2003
  - Great Lakes Symposium on VLSI (GLSVLSI) 2001-2003
  - International Symposium on Circuits and Systems (ISCAS) 2000
  - Asia South-Pacific Design Automation Conference (ASP-DAC) 2005
  - International Symposium on Circuits and Systems (ISCAS) 2004

Funded Projects

- SHF: Medium: Back to the Future with Printed, Flexible Electronics Design in a Post-CMOS Era when Transistor Counts Matter Again, NSF, $800,000, 8/1/2014-7/31/2017 (CoPIs: Marc Riedel, David Lilja, Ramesh Harjani, Dan C Frisbie).
- EAGER: Digital Yet Deliberately Random -- Synthesizing Logical Computation on Stochastic Bit Streams, NSF, $299,999.00, 05/16/2012 – 05/15/2014 (coPIs: Marc Riedel, David Lilja, Ramesh Harjani)

- Sachin Sapatnekar, Kia Bazargan, Ramesh Harjani, Jaijeet Roychowdhury, "Phase 2: 3D-ADOPT: 3D-Analysis, Design and Optimization of Mixed Digital/Analog/RF Circuits", DARPA, duration: 18 months (02/01/05 – 06/1/06), amount: $928,000.
- Sachin Sapatnekar, Kia Bazargan, Ramesh Harjani, Jaijeet Roychowdhury, "3D-ADOPT: 3D-Analysis, Design and Optimization of Mixed Digital/Analog/RF Circuits", DARPA, duration: 18 months (06/01/04 – 12/1/05), amount: $792,999.
- Kia Bazargan , "CAREER: Computer-Aided Design of Mixed ASIC / Reconfigurable Fabrics of the Nanometer Era", NSF, duration: 5 years (02/01/04- 01/31/09), amount: $400,000 total.
- E. Ebbini, K. Bazargan, "QB-Mode Ultrasonic Imaging: A New Method for Imaging Quadratic Signal Components", NIH, duration: 2 years (09/01/2005 -08/31/2007), amount: $396,890.
- Ramesh Harjani, Kia Bazargan, "3D Mixed Analog / Digital Prototype Design", SRC, unrestricted research grant, $40,000, 2003.
- Kia Bazargan, "Scholarships to support graduate research and study", DAC conference, 2001. Amount: $24,000. Expired.
- Kia Bazargan, "HARP: Hard-wired Routing Pattern FPGAs", Altera Corporation, Unrestricted research grant, amount: $5,000, 5/2005.
- Kia Bazargan, "Memory Binding and Placement for Reconfigurable Computing Systems", University of Minnesota Grant-in-aid, duration: 9 months (1/1/01 – 6/30/02). Amount: $16,192. Expired
- Kia Bazargan, "Integrated and Incremental Partitioning and Placement", University of Minnesota Grant-in-aid, duration: 9 months (7/1/02 – 1/15/04). Amount: $18,041. Expired

Education Activities and Accomplishments

Course Development and Teaching

- EE2361: "Intro to Microcontrollers", ECE Dept., Univ of Minnesota.
  - Course description: PIC24 micro-controllers are used in this course to teach the basics of interrupts, timers, wave form generation (e.g., pulse-width modulation), A/D and D/A conversion, serial interfaces such as USART and SPI. The course has a heavy lab components in which students work on 8-9 projects during the semester, wiring up bread boards and write code to perform various tasks.
- EE8950: "Advanced Topics in ECE: Reconfigurable Computing", ECE Dept., Univ. of Minnesota, (http://umn.edu/~kia/Courses).
  - *Course description*: This course covers the concept, hardware platforms and software support systems for reconfigurable computing (RC) using field programmable gate arrays (FPGAs). Reconfigurable computing takes advantage of the programmability of FPGAs and modifies the configuration of the logic blocks and switches on the FPGA to build new functional units that better match application hardware requirements. Topics covered in the course include computer aided design tools for FPGAs (compiler, high-level synthesis and physical design), the basic concept of reconfigurable computing and its modes of operation (static vs. dynamic reconfiguration), examples of successful RC applications, existing architectures, operating system (OS) support, new architectures and future trends.
- EE5324: "VLSI Design II", ECE Dept., Univ. of Minnesota, (http://umn.edu/~kia/Courses).
  - *Course description:* This course is the continuation of EE5323, and focuses mainly on digital design at the system level. Optimization of VLSI circuits at various levels of abstraction (algorithmic, numeric encoding, structural and device) is the main thrust of the course. Topics covered include CMOS high-speed carry chains, fast CMOS multipliers, floating point computations, high-speed parallel shifters, CMOS memory cells, array

structures, read/write circuits, design for testability, including scan design and built-in self test, system-level timing and power optimization.

- EE5301: "VLSI Design Automation I", ECE Dept., Univ. of Minnesota, (http://umn.edu/~kia/Courses).
  - *Course Description:* This course covers algorithms for computer-aided design of VLSI circuits. Students learn and develop algorithms for basic graph problems, partitioning of VLSI circuits, floorplanning, placement and routing. Recent papers are studied and discussed in class, and each student presents at least one paper on the topics covered in class. Four programming projects are completed by the students, giving them the required skills to work in the EDA companies.

Students Supervised

Graduated Research Advisees

- **PhD**

1. Cristinel Ababei, thesis title: "Design Automation for Physical Synthesis of VLSI Circuits and FPGAs", Dec 2004, now with Magma Design Automation.
2. Wonjoon Choi, thesis title: "Performance Driven Optimization of VLSI Layout", Sep 2005, now with Sun Microsystems, Texas, Austin.
3. Satish Sivaswamy. Thesis Topic: "Architecture and CAD Techniques for Optimizing FPGAs and Reliability of Integrated Circuits", Aug 2009 (now with Xilinx).
4. Pongstorn Maidee. Thesis Topic: "Methodologies and tools for yield improvement of programmable logics", Expected graduation: Dec 2009, Now with Xilinx.
5. Hushrav Mogal. Thesis Topic: "CAD Algorithms Dealing with Process and Temperature Effects in Digital Integrated Circuits". Expected Graduation: Dec 2009. Now with Synopsys.

- **M.S.**

1. Akhilesh jaiswal, Atomistic Modeling of Novel 2D Devices, expected Spring 2014.
2. Darshak Gandhi, Approximate Computing, expected fall 2014.
3. Peiran Suo, "Binary Stochastic Sequential Logic", 2013.
4. Harish N. Mallapragada, GPU implementation of VPR's placement algorithm, 2011.
5. Ram R Varma, GPU Implementation of VPR's routing algorithm, 2011.
6. Zhen Chen, Thesis Topic: Parallel implementation of a second-order implementation of the Volterra filter. Graduation: 2006.
7. Dereje Yilma, MS Plan B, "Implementing the 'Separable' Second Order Volterra Filter In Xilinx Virtex-E FPGA", June 2005, now with IBM Rochester.
8. Vinil Sharma, MS Plan B, "Flexible Sequential Random Access Memory", Dec 2004.
9. Anatoli Glagolev, MS Plan B, "Floating-Point Division and Square Root on Xilinx Virtex-E FPGA", Dec 2004, now with Microsoft.
10. Girish Venkatraman, MS Plan B, " FPGA based Implementation and Analysis of Flexible Sequential Access Memory", May 2004.
11. Ranjit Eswaran, MS Plan B, "Legalization of Placement of Mixed-Sized Macros", 2003, now with Intel.
12. Karthikeyan Bhasyam, MS Plan B, "Algorithms for Resource Assignment and Scheduling in High-Level Synthesis", May 2003, now with Qualcom.

13. Karthik Ranganathan, MSEE, “Flexible Sequential Access Memory”, May 2003, now with Cypress Semiconductor.
14. Paul Kern, MS Plan B, “A Microcontroller-Based Heating and Cooling Control System”, May 2003, now with Honeywell.
15. Vamsi-Krishna Reddy Mareddy, MS Plan B, “A fast Run-Time Placement algorithm for Partial & Dynamically Reconfigurable FPGAs”, July 2003, now with Pfizer.
16. Pongstorn Maidee, “Timing-Driven Partitioning-Based Placement for Island Style FPGAs”, Oct 2003.
17. Michael A. Hinterberg, MS Plan B, “Reconfigurable Graphics Pipeline on Annapolis Firebird”, Summer 2002, now with HP.
18. Varun Kharbanda, MS Plan B, “Implementing a Signal Processing Algorithm on the Annapolis FireBird FPGA Board”, May 2002.
19. Cristinel Ababei, MS Plan A, “Statistical Timing Driven Partitioning”, May 2002.
20. SeongHo Song, MS Plan B, “GOST Algorithms implementation using VHDL”, Summer 2002.
21. Joseph S. Mollen, MS Plan B, “Hardware Independent Delay and Power Calculation Modules”, Dec 2001, now with IBM Rochester.
22. Saed Wadi, “High Speed Phase-Locked Loop Used in VCSEL Driver Chip”, May 2001, with Honeywell (after which he opened the Saffron Restaurant in downtown Minneapolis ☺).

Undergraduate Student Researchers

1. (Senior Honors Program, REU) Yanzi Zhu, “Binary Stochastic Computing”, 2013-14.
2. (Senior Honors Program) Zhiheng Wang, “Hardware Implementation of Dynamical Systems using Stochastic Computing”, 2013-14.
3. (REU) Nicholas B. VanDeusen, “Modeling Dynamical Systems using Stochastic Computing”, Summer 2013.
4. (Senior Honors Program) Xiaonan Zhang, “Implementing addition and multiplication in base Phi”, 2012-13.
5. (Senior Honors Program) Kevin Krile, “Hybrid binary stochastic computing: encoding, addition and multiplication”, 2012-13.
6. (Senior Honors Program) Dan Schoppe, “Implementing a Randomized Partitioning Algorithm on an FPGA”, 2009.
7. (Senior Honors Program) John Engleman, “Hardware Operating System Support for Reconfigurable Computing”, Academic year 2005-2006.
8. (Senior Honors Program) Joe Strommen, “Steiner Routing for FPGA Circuits”, Academic year 2004-2005.
9. (NSF REU) James D. Foltz, “PRGUI: A Visual Tool For Displaying Placement and Routing”, Summer 2004.
10. (UMN UROP) Sharareh Noorbaloochi, “Compiling Datapath Expressions to JBits Compatible Hardware Implementation”, 2002.
11. (Summer REU) Seth Sweep, “Using JBits as an Interface for Field Programmable Gate Arrays (FPGAs)”, 2002.
12. (Senior Honors Program) Matthew Tilstra, “Developing a Hardware Cache Manager for Reconfigurable Computing Platforms”, 2001.