Buffering Global Interconnects in Structured ASIC Design

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Abstract

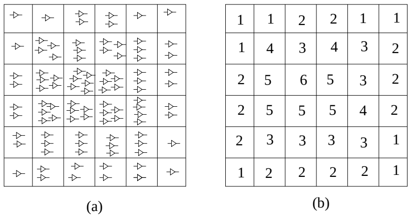
Structured ASICs present an attractive alternative to reducing design costs and turnaround times in nanometer designs. As with conventional ASICs, such designs require global wires to be buffered. However, via-programmable designs must prefabricate and preplace buffers in the layout. This paper proposes a novel and accurate statistical estimation technique for distributing prefabricated buffers through a layout. It employs Rent's rule to estimate the buffer distribution required for the layout, so that an appropriate structured ASIC may be selected for the design. Experimental results show that the estimation for a uniform buffer distribution is accurate and economic.

1 Introduction

In the nanometer regime, structured ASIC design has emerged as a promising new design style to fill the gap between cell-based ASIC designs and field programmable gate arrays (FPGAs). They are composed of regular arrays of prefabricated standard building blocks, with fixed mask structures. One paradigm that is used involves *via-configurability*, where the building blocks and interconnect skeletons are prefabricated and then both can be custom configured by the appropriate via connections. This programmability involves only a small number of masks [1–5]. This strategy provides a low NRE (non-recurring engineering) cost, and yet with relatively high-performance solutions. Additionally, the regularity from the well-characterized logic blocks and fixed interconnect structures helps to combat problems associated with manufacturability, yield, noise, or crosstalk.

However, many of the other problems of nanometer design continue to plague structured ASICs, prominent among them is the interconnect performance. A key issue in overcoming this is through the use of buffer insertion along global wires. Buffer insertion can not only improve timing performance, but can also effectively reduce noise. The number of buffers needed in design continues to rise with decreasing feature sizes, and it is projected that at the 32nm technology node, a very large proportion of cells will be buffers [6]. Although interconnects are generally buffered in the later phases of physical design, buffer resources must be planned earlier in the design process, so that enough resources are available for the later insertion. This problem is more acute for via-programmable structured ASICs, where, in addition to the basic standard building blocks, buffers must be prefabricated and distributed in the layout. Although it is possible to reconfigure the basic building blocks to work as buffers, this is not an economical approach since (a) the number of buffers can be very large, (b) configuring a large and general standard building blocks as buffers is an inefficient use of resources, and (c) these blocks do not have the driving ability of dedicated buffers. Therefore, it is essential to distribute dedicated buffers in structured ASICs, and to plan for them well, prior to the fabrication of the chip.

The buffer insertion problem for structured ASIC design has not been fully addressed so far. The only work we know of that considers this issue is [9], where it is assumed that a uniform distribution of dedicated buffers throughout the circuit with logic cell/buffer ratio of 2:1. However, this does not recognize that the demand for buffers depends on the interconnect complexity of circuits, and a single ratio for all kinds of circuits may result in a large waste of buffer resources. This paper proposes a distributed buffer insertion methodology for the use of dedicated buffers in structured ASIC design. A statistical estimate of buffer distribution is derived, based on Rent's rule. For each range of (p, k) values, where p is the Rent's exponent and k the Rent's coefficient, our algorithm (described in section 3.3) finds a buffer distribution for circuits falling in that range. Thus for each range, we can prefabricate an off-the-shelf structured ASIC chip with buffers preplaced according to the estimated buffer distribution of that (p, k) range. In the implementation phase, a designer may choose the appropriate prefabricated chip for implementing custom design according to values of p and k for the design. Experimental results show that the buffer resource estimation is accurate and adequate for interconnect buffering purpose.



1	1	2	2	1	1
1	4	3	4	3	2
2	5	6	5	3	2
2	5	5	5	4	2
2	3	3	3	3	1
1	2	2	2	2	1

Figure 1: (a)A schematic shows a chip tessellated into tiles with buffers dispersed within (VCCs not shown). (b)The corresponding tessellation with the buffer capacity listed.

2 Buffer Insertion for Structured ASIC Design

In cell-based ASIC design, distributed buffer insertion approach [8] has shown advantage over the buffer block approach [7]. For structured ASIC design, in the same spirit of interspersing buffers with logic units across the circuit, we adopt a buffer insertion model in which the prefabricated buffers are scattered throughout the structured ASIC, and the distribution of buffers should be adequate enough for buffering global wires. We also refer to this as a distributed buffer insertion model to capture the distributed nature of this scheme, although unlike [8], the buffers are actually prefabricated in structured ASICs. We define the structured ASIC to be a two dimensional array composed of via-configurable standard building blocks, denoted as *via-configurable cells* (VCC), which are connected by via-configurable interconnect wires. To facilitate the distributed buffering model, we divide the circuit into an array of *tiles*, and each tile is a square area containing $m \times m$ VCCs as well as a predetermined number of dedicated buffers for interconnect buffering usage. For a tile positioned at (i, j), we refer to this number as the *buffer capacity*, denoted as $B_{i,j}$. If $B_{i,j}$ is uniform for all (i, j), we refer to this as a *uniform* buffer distribution; otherwise it is said to be *nonuniform*. In a routing solution, the actual number of utilized buffers in tile (i, j) is referred to as the *buffer usage*, denoted as $b_{i,j}$. If $b_{i,j} > B_{i,j}$, the routing solution is invalid, and we refer to this situation as *buffer overflow*. Figure 1(a) shows a 6×6 tile graph for a structured ASIC design, with buffers distributed within tiles. The corresponding buffer capacity of each tile in the circuit with a nonuniform buffer distribution is shown in Figure 1(b).

In this paradigm, buffers are prefabricated into the layout but are connected to the global lines that require buffering only in the later phases of physical design. To enable this, we utilize a via-defined buffer insertion (VDBI) scheme, which allows a buffer in a tile to be inserted along any interconnect wire traversing the tile, by means of a via configuration. Figure 2(a) shows a representative buffer in a tile: its input and output are connected to horizontal and vertical wires that go across the tile. Figure 2(b) shows that any wire that crosses the tile can choose to be via-configurably connected to either this buffer through "insertion vias," or through "jumping vias" to a metal strip that can skip the buffer entirely. Our model uses a simple yet effective distance-based criterion for buffer insertion. As noted in [7], the delay of a wire is relatively insensitive to the precise location of a buffer, and a buffer can be inserted within a feasible region instead of at a specific location without greatly affecting the timing performance. Our distance-based model is similar to that used in [8, 10]: the maximum length of interconnect can be driven by a gate (buffer) is L, and this is referred to as the *critical length*. For a two-pin net, this implies that the separation distance between two buffers is at most L.

3 Statistical Buffer Distribution Estimation

3.1 Rent's Rule

The basic VCCs, buffers and interconnects in structured ASIC must be prefabricated, and this necessitates early and accurate buffer distribution estimation without knowing the details of circuit. We must determine the buffer capacity of each tile prior to fabrication, and this estimation has to be accurate, so that enough buffers are allocated to satisfy the buffering usage, but not too pessimistic to waste silicon area. Also this estimate should be based on basic circuit properties instead of circuit implementation details, so that these base chips can be used to implement

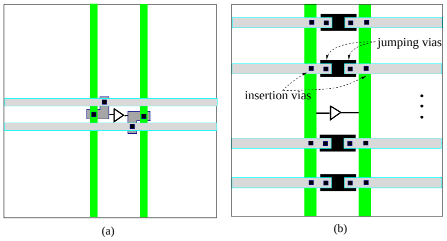


Figure 2: (a) The input and output of a buffer are each connected to two wires that stretch across the tile, in the horizontal and vertical direction respectively. (b) Buffer insertion on a wire crossing the tile is carried out by means of via definition. An "insertion via" connects a buffer; a "jumping via" is an electrical short circuit.

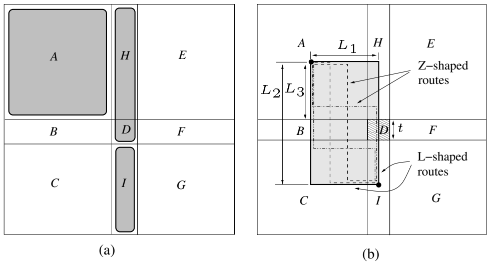


Figure 3: (a) We divide the circuit into 9 blocks, A through I, and for estimation, we merge two blocks H and D into a larger block HD. (b) Estimation of the length of interconnect wires passing tile D.

a variety of designs, and may work with various physical design tools. With these considerations, our buffer distribution estimation is based on Rent's rule, which is an empirical relationship that correlates the number of signal input and output (I/O) terminals T, to the number of gates, N, in a random logic network [11], and it takes the form:

$$T = kN^p \tag{1}$$

where k and p are called the *Rent's coefficient* and the *Rent's exponent*, respectively. These parameters reflect the complexity of a circuit, and can be derived in the process of partitioning the circuit netlist. Our work assumes that these parameters have been computed for the circuit to be mapped to the structured ASIC. When N exceeds some critical size N_{crit}, the relationship between T and N deviates from the exponential curve and enters region II of Rent's rule [11]; T will keep constant or drop while N increases.

3.2 Estimating the Statistics of Buffer Distribution

The number of buffers required in a tile is highly correlated to the total length of external interconnect wires crossing this tile. If a larger number of wires traverse a given tile, it is likely that a larger number of buffers will have to be inserted in the tile. From the Rent's exponent p and Rent's coefficient k for a circuit, we can apply Rent's rule to statistically estimate the length of interconnect wires crossing a specific tile D, and further, to estimate the number of buffers required in the tile.

A schematic of a circuit layout is shown in Figure 3(a). The layout is a square consisting of $n \times n$ tiles[1]. Each tile is a square consisting of $m \times m$ VCCs, and the geometrical size of a tile is $t \times t$ units. While considering the estimation for a tile D, we divide the circuit, for convenience, into 9 blocks, labeled A through I, as shown in the figure, with block D in the center. Block A consists of all tiles northwest of D; block B is composed of all tiles to the east of D, and so on. We will use (i, j) to refer to the coordinates of tile D in the $n \times n$ tiling. For estimation purposes, it is reasonable to assume that the routing will remain within the bounding box set by the pins of a net. Under this assumption, the interconnect wires that cross block D consist of the contributions of the wires connecting block pairs in set S defined as: *S* = {*(A, F), (A, G), (A, I), (B, E), (B, F), (B, G),(B, H), (B, I), (C, E), (C, F), (C, H), (E, I), (F, H), (F, I), (G, H), (H, I)*} . The total wire length passing through tile D, W_D, is given by

$$W_D = \sum_{all\ block\ pairs\ (x,y) \in S} W_{x,y}, \tag{2}$$

where $W_{x,y}$ is the total wirelength of all interconnects crossing tile D, connecting VCCs in blocks x and y, where $(x, y) \in S$. Since the tile dimension t is generally much smaller than the critical length L, the interconnects originating from tile D will not be likely to consume buffer resources at D, and we only consider the contribution from those wires *passing* D. Knowing W_D, if the maximum interconnect length driven by any buffer is length L units from the insertion model described in section 2, then a *unit length* interconnect segment in a wire crossing tile D will have a probability of $1/L$ of requiring a buffer to be inserted in tile D. This implies that an external wire passing a tile of dimension t horizontally will probabilistically insert t/L buffers from this tile. We can use this idea to estimate the buffer capacity, B_D, required for tile D as the probabilistic usage of buffers in the tile. In other words,

$$B_D = \frac{W_D}{L} \tag{3}$$

The $W_{x,y}$ components of W_D can be estimated by using Rent's rule. As an example, we now illustrate how the value of $W_{A,I}$ may be estimated; other $W_{x,y}$ components may be estimated in a similar way.

As in [12], we merge two neighboring blocks H and D into a larger block HD as shown in Figure 3(a), and apply the I/O terminal conservation rules to the three blocks A, HD and I, which are shown as shaded regions in Figure 3(a). We have the number of I/Os connecting blocks A and I, denoted as $T_{A\_to\_I}$, to be

$$T_{A\_to\_I} = T_{AHD} + T_{HDI} - T_{HD} - T_{AHDI} \tag{4}$$

in which the $T_{block}, block \in \{AHD, HDI, HD, AHDI\}$ is the number of I/Os of the combinational blocks, and they can be estimated using Rent's rule (1). However, in applying this formula, we may find that the estimate moves into region II of Rent's rule as described in section 3.1. We use a simplified approach to handle this deviation: when the number of VCCs in the combinational block exceeds N_{crit}, we substitute this number with N_{crit}. Experimental curves show that N_{crit} is between 150 to 200 for various circuits, and we simplify it by taking $N_{crit} = 175$ for all experimental circuits. Experimental results also show that small variation in the choice of N_{crit} does not affect estimation results much.

To calculate the number of interconnects between blocks A and I, we define a variable α that is the fraction of terminals that are sinks. Thus we can obtain the number of point-to-point interconnects between block A and block I, $I_{A\_to\_I}$ as:

$$I_{A\_to\_I} = \alpha T_{A\_to\_I} \tag{5}$$

and α can be expressed as the average fanout of the system, as $\alpha = \frac{fanout}{fanout+1}$. Using equation (5) to obtain the number of interconnects between blocks A and I, we can further combine it with a simplified L-Z shaped routing model to estimate the wire length crossing tile D due to interconnects between A and I, $W_{A,I}$. Figure 3(b) shows a set of possible L-shaped and Z-shaped connections between the blocks A and I. Probabilistically, we can assume that the average position of the terminals of the interconnects are at the center of blocks A and I. Thus the routing of interconnects will follow the bounding-box path, and falls in the dotted box in Figure 3 (b). We denote the distance between the centers of A and H by L_1; the distance between the centers of A and C by L_2; and the distance between the center of A and the northern edge of D as L_3. The parameters L_1, L_2 and L_3 are pictorially illustrated in Figure 3, and these can be expressed in terms of i, j, n and t.

In practice, it is observed that a router will route the bulk of the nets with simple L-shaped and Z-shaped patterns [13]. Hence, we can assume that the routing of an interconnect will utilize one of these two patterns, and the probability of using an L-shaped and Z-shaped route are P_L and $P_Z = 1 - P_L$, respectively. As in [13], we assume $P_L = 0.7$ in the estimation. Under this routing model, we can estimate the wirelength crossing tile D due to L-shaped routes as:

$$W_{L,(A,I)} = \frac{1}{2} \cdot t \cdot I_{A\_to\_I} \cdot P_L \tag{6}$$

The factor "1/2" in the above equation is due to the fact that there are two possible L-shaped routes, and only the upper-L route will pass the D tile.

Similarly, there are two kinds of Z-shaped routes, type I: with two horizontal segments, and type II: with two vertical segments. If every Z-shaped route has an equal probability of being taken, the type I Z-shaped routes will have a probability of $P_I = L_1/(L_1 + L_2)$ of being taken, while the type II Z-shaped routes have a probability of $P_{II} = L_2/(L_1 + L_2)$. Both types of routes can pass tile D, and we can probabilistically estimate the wirelength of Z-shaped routes crossing tile D as:

$$W_{Z,(A,I)} = (P_I \cdot \frac{t/2}{L_1} + P_{II} \cdot \frac{(L_3 + t)}{L_2}) \cdot t \cdot I_{A\_to\_I} \cdot (1 - P_L) \tag{7}$$

Finally, we can compute the total interconnect wire length from A to I that traverses D as $W_{A,I} = W_{L,(A,I)} + W_{Z,(A,I)}$. The wirelength contribution from other block pairs in set S can be computed in a similar way as $W_{A,I}$, and their values can be substituted into equation (2) and (3) to yield the estimated buffer capacity B_D for tile D at position (i, j).

[1] For a general circuit of rectangular form, the analysis is very similar.

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Algorithm: Estimate_buffer_distribution_for_circuits_in_a_range
Input: Tile array of size $n \times n$; range of Rent's exponent $[p_i, p_{i+1}]$; range of Rent's coefficient $[k_j, k_{j+1}]$.
Output: A buffer capacity estimation that can meet the buffer insertion requirements of all circuits falling in the above ranges.
begin
  $k = k_{j+1};$
  for each tile $D$ in the tile array
    max_num_buffer($D$) = 0;
    for $p = p_i; p \leq p_{i+1}; p = p + \delta$
      Estimate buffer usage at $D$, i.e., num_buffer($D$), using the method in section 3.2
      with Rent's exponent and coefficient $p$ and $k$;
      if (max_num_buffer($D$) $<$ num_buffer($D$))
        max_num_buffer($D$) = num_buffer($D$);
    end for
    set buffer capacity at $D$ to be max_num_buffer($D$);
  end for
end
```

Figure 4: Estimation of buffer distribution for a range of circuits.

3.3 Application to Structured ASICs

3.3.1 Classification of Structured ASICs

Structured ASICs consist of predetermined regular architectures, and the buffer resource planning must be addressed at the prefabrication phase. However, due to the unavailability of specific circuit information at this phase, we must preallocate buffers so that it can satisfy the buffer insertion requirements of a range of circuits. As stated earlier, our approach determines the buffer distribution that is necessary for a circuit, based on its basic characteristics, namely, the Rent's exponent p and Rent's coefficient k. The practical way of employing structured ASICs in design is that they are prefabricated with other hard Intellectual Property (IP) blocks, which are embedded processors, I/O controllers, etc. The structured ASIC part can be used to implement users' specific logic, and we can assume that there is only one Rent's exponent p and one Rent's coefficient k associated with this logic.

We now describe how the buffer distribution determined in section 3.2 is used to design off-the-shelf structured ASIC parts that can be used for a specific circuit. We divide the spectrum of Rent's exponent values, p, and Rent's coefficient values, k, into a set of ranges: $R_p = \{[p_1, p_2], [p_2, p_3], [p_3, p_4], ...\}$, $R_k = \{[k_1, k_2], [k_2, k_3], [k_3, k_4], ...\}$. For the circuits of tile array size $n \times n$ in a specific range pair $[p_i, p_{i+1}]$ and $[k_j, k_{j+1}]$, we can predetermine the maximum number of buffers required in each tile for these circuits with the algorithm shown in Figure 4. Using this estimation technique, a set of structured ASIC chips can be prefabricated. When a given circuit is to be mapped on to this fabric, its Rent's parameters are first computed. Based on their values, the appropriate prefabricated structured ASIC chip is chosen, and the circuit is mapped on to that chip. If the Rent's parameter is exactly at the boundary between two ranges, we choose the structured ASIC representing the lower range to avoid waste of buffer resource.

To find a buffer distribution fitting the requirements of all circuits in the range $[k_j, k_{j+1}]$ and $[p_i, p_{i+1}]$ as in Figure 4, we must find the maximum estimated buffers in each tile.

Theorem 1. *The estimated number of buffers is a monotonically increasing function of the Rent's coefficient, k.*

Theorem 1 can be easily proved from the linear dependence on k in Rent's rule. From Theorem 1, we can set k to be at the upper limit of the range, i.e., k_{j+1} to find the maximum buffers in each tile. However, it is easy to experimentally show that the dependence between the estimated number of buffers and p is not monotonic, and therefore, we apply an enumeration of p with a step size of δ to find the maximum number of estimated buffers in each tile for that range. In our experiments, we find $\delta = 0.01$ is an appropriate choice of the step size. With this estimated buffer capacity for circuits that lie within a range of Rent's parameter values, we can predetermine a single buffer distribution to satisfy the interconnect buffering requirement of all of these circuits, thus creating only one structured ASIC chip that can meet the requirements of all of these circuits. The finer the granularity of these ranges, the more accurate the buffer distribution will be, but the trade-off is that larger number of base chips have to be prefabricated. The size of the structured ASICs is determined at the prefabrication phase and it may be larger than the circuit to be implemented. However, for the same p, k range, it can be proved that the estimated buffer usage for a larger prefabricated structured ASIC will be greater than the estimated buffer usage for a smaller circuit, if we place the smaller circuit at the center of the structured ASIC. Thus if we estimate and distribute buffers aiming at a larger base structured ASIC, it will always satisfy the requirement of smaller implemented circuits.

3.3.2 Uniform Buffer Distribution

The buffer distribution estimation obtained above is a non-uniform one, i.e., the number of buffers at different tile locations are different. An important feature of structured ASICs is the regularity in design, which helps much in improving the manufacturability and reducing the design complexity. So an alternative to the above *nonuniform* estimated buffer distribution is a *uniform* buffer distribution. We set the number of buffers each tile in the uniform distribution as the *average* buffer number over all the tiles in the nonuniform distribution, which is obtained from the algorithm in Figure 4. This uniform buffer distribution allocates the same amount of total buffers as the nonuniform distribution in the prefabrication phase, and more importantly, it maintains the regularity of the structured ASICs. Since its buffer level is based on the average buffer number from our estimation, it could still satisfy the requirement of interconnect buffering under our flexible buffer insertion model, and this is verified in experimental part.

4 Experimental Results and Conclusion

Our experiments are performed on 18 of the largest MCNC benchmarks, ranging from 1047 to 8383 logic blocks. These circuits have been technology-mapped to 4-LUTs and flip flops using Flowmap [14], and then the 4-LUTs and flip flops are combined into basic logic blocks with VPACK tools [15]. The benchmarks are then placed and routed with Versatile Place and Route (VPR) tools [15] under a $0.09\mu m$ technology. In placement and routing, the VCC block used is the same as the VPGA based 4-LUT CLB designed in [1], and the routing architecture is the switch block architecture also from [1]. The technology parameters of $0.09\mu m$ technology used in physical design are derived from the scaling of parameters in [1] as well as from [16] and [17].

For the buffer-related parameters, we take each tile to include $8 \times 8 = 64$ VCCs, and compute the critical length L for buffer insertion using the estimation from [10], which results in $L \approx 500\mu$m. We divide the Rent's exponent and coefficient spectrum into range sets $R_p = \{[0.3, 0.4],$ $[0.4, 0.5]$, $[0.5, 0.6]$,$[0.6, 0.7]\}$, and $R_k = \{[3.0, 4.0], [4.0, 5.0]\}$, corresponding to a total of $|R_p| \times |R_n| = 8$ different types of structured ASICs to be fabricated. For each benchmark circuit, we can derive the Rent's exponent p and coefficient k in a recursive partitioning process using hMetis [18]. We then select the corresponding range in R_p and R_k for each circuit. Assuming the prefabricated base structured ASIC has the same tile array size as the actual circuit implementation, we can apply the estimation algorithm in Figure 4 to find the *estimated* number of buffers in each tile. We use this as the estimated *nonuniform* buffer capacity for the prefabricated structured ASIC characterized by the corresponding ranges in R_p and R_k, and denote this as nonuniform (NU) distribution. Based on this, we can further calculate the average number of buffers per tile as the level of the estimated *uniform* buffer capacity, and denote it as uniform (UNI) buffer distribution. We also experiment on a distribution that the ratio between logic cells and buffers is 2:1 everywhere like [9], and denote this as a uniform 2:1 ($U21$) distribution. In our experimental setup, there are 32 buffers in each tile for the $U21$ distribution (since there are 64 VCCs each tile).

To verify the choices that have been made, we apply a buffer insertion algorithm from [8] to actually insert buffers into the above placed and routed circuits, under the NU, UNI and $U21$ buffer capacity models. This will produce the *actual* number of buffers used in each tile. Comparing this actual buffer number distribution with that from the estimation models, we list the experimental results in Table 1. The first four columns list the circuit names, the values of Rent's exponent p and coefficient k, and the tile array size. The next four columns list the average number of buffers per tile for the estimated buffer capacity (EBC), and the actual buffer usages from buffer insertion under the three different buffer distribution models. The value of EBC has been rounded to the nearest integer, and it is exactly the uniform buffer capacity used in the uniform (UNI) distribution model. The uniform buffer capacity for the $U21$ model is 32 for all structured ASICs, and is not explicitly listed. As we can see, the average number of buffers inserted in the cases of NU and UNI models are close to those from our statistical estimation; in fact, the actual number of buffers required is always a little smaller than the estimated value due to the fact that our buffer estimation method determines the maximum number of buffers for a set of circuits falling in a range of Rent's exponent and coefficient, and therefore, this estimation can be larger than its actual usage for a specific circuit. On the other hand, this pessimism also increase the robustness of the estimation, so that the estimated buffer capacity will satisfy the buffering requirement of circuits even in the presence of fluctuations in the buffer usages of practical circuits. For the buffer usage under $U21$ model, the average number of buffers used is much less than the capacity, 32, and this suggests an inefficient use of buffer resources.

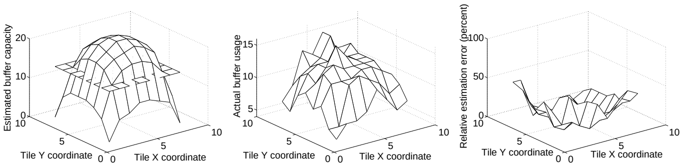
The columns labeled "# buffer overflow per tile" report the average

Circuit	p	k	Tile array size	Average # buffers per tile				# buffer overflow per tile			Average buffer usage rate			Critical path delay (ns)		
				EBC	NU	UNI	$U21$	NU	UNI	$U21$	NU	UNI	$U21$	NU	UNI	$U21$
alu4	0.628	4.38	5 × 5	11	9.48	9.52	9.24	0	0.2	0	85%	86%	29%	2.02	1.91	2.00
apex2	0.640	4.28	5 × 5	13	9.60	9.44	9.20	0	0	0	74%	73%	29%	1.80	1.90	1.83
apex4	0.657	4.23	4 × 4	10	8.06	8.19	7.75	0	0.13	0	85%	86%	24%	2.04	1.95	2.05
clma	0.578	4.37	12 × 12	14	10.62	11.15	10.54	0	0.6	0	76%	79%	33%	3.35	3.33	3.30
des	0.389	4.34	8 × 8	4	3.02	3.33	2.90	0	0.72	0	79%	88%	9%	1.54	1.61	1.51
diffeq	0.460	4.07	5 × 5	4	3.64	3.60	3.48	0.08	0.32	0	88%	87%	11%	2.12	2.43	2.11
elliptic	0.641	3.87	8 × 8	10	8.19	8.53	8.30	0	0.44	0	81%	85%	26%	3.55	3.95	3.62
ex1010	0.573	4.49	8 × 8	11	7.81	8.06	7.58	0.02	0.08	0	69%	71%	24%	2.31	2.50	2.29
ex5p	0.675	4.39	4 × 4	8	6.25	6.81	6.69	0	0.13	0	83%	90%	21%	2.02	1.88	1.84
frisc	0.695	4.39	7 × 7	16	11.92	13.71	12.22	0.02	0.73	0	76%	87%	38%	4.19	4.59	4.27
misex3	0.628	4.38	5 × 5	7	5.40	4.92	5.28	0	0	0	78%	71%	17%	1.45	1.68	1.47
pdc	0.674	3.93	8 × 8	14	11.38	11.28	11.26	0	0.09	0	83%	82%	35%	2.46	2.55	2.48
s298	0.528	4.28	6 × 6	8	5.50	5.58	5.50	0	0	0	69%	70%	17%	4.15	4.43	4.16
s38417	0.437	4.15	10 × 10	7	5.81	5.54	5.26	0.01	0.27	0	82%	83%	16%	3.03	3.71	3.06
s38584.1	0.413	4.18	10 × 10	7	4.06	4.62	3.99	0.01	0.05	0	62%	69%	13%	2.70	2.99	2.58
seq	0.616	3.98	5 × 5	9	8.36	8.08	8.20	0	0.32	0	90%	87%	26%	1.87	1.97	1.76
spla	0.676	3.99	8 × 8	12	7.69	7.83	7.81	0	0.03	0	64%	62%	24%	2.03	2.30	2.05
tseng	0.496	3.94	4 × 4	3	2.44	2.19	2.31	0	0	0	81%	73%	7%	2.08	2.08	2.09

Table 1: Comparison of the buffer usage and timing performance results from buffer insertion under three buffer distribution models: nonuniform (NU) distribution, uniform (UNI) distribution and uniform 2:1 ($U21$) distribution. EBC is the estimated buffer capacity from our estimation algorithm.

buffer usage overflow per tile for each of the three buffer distribution models. $U21$ model, due to its extreme pessimism, results in no overflow at all, but at the price of large waste of resources. For the NU model, it is observed that most of the circuits are free from buffer overflow, and the occurrence of instances that do have overflows is very low, less than 0.08 per tile. The UNI buffer distribution model results in more overflows, because it is derived from the UNI model, but the uniformity of the distribution incurs overflow, and it can be considered as a trade-off for the regularity in buffer distribution. However, it is observed these overflows are of low values, and even the worst case has less than 0.73 overflow per tile. These results show that our buffer estimation method can produce an adequate solution, so that the solution can successfully satisfy the buffer insertion requirements of practical circuits. Moreover, even at the trade-off of regularity, our uniform distribution estimation still shows good estimation of buffer levels.

The next three columns list the average buffer usage rate of all circuits under different buffer distribution models. It shows that for most of the circuits, the average buffer usage rate is between 70%-90% for both NU and UNI models, which means that the pessimism of our estimation algorithm is low, and that it actually produces reliable and economical *a priori* buffer distribution solutions. However, due to the extreme high buffer capacity, the $U21$ buffer distribution shows a very poor usage rate, and thus this solution is not economical. The last three columns of Table 1 show the critical path delays for benchmark circuits under three buffer distribution models. For the overflowed buffers, we remove them from buffer insertion solution, and then calculate the critical path delay. We can find there is not much difference in the timing performance of the three distribution models. Although there are some buffer overflow for the UNI model, the rip-up of those buffers does not affect the timing performance much due to: (a) the number of overflowed buffers is small, (b) they may not lie on the critical path. These facts legitimize the use of the *uniform* buffer capacity model based on our estimation in structured ASICs; we can thus acquire an adequate and economic buffer solution with great regularity to improve the manufacturability and reduce cost, while not affecting the timing performance significantly.



(a) (b) (c)

Figure 5: Accuracy of the statistical buffer distribution estimation. (a) Estimated buffer capacity distributions for the nonuniform and uniform distributions. (b) Actual buffer usage distribution under the uniform buffer capacity. (c) Relative error of the buffer capacity estimation compared with actual buffer usage under the uniform buffer capacity.

Figure 5 further shows the two dimensional buffer distribution for a specific representative circuit, *pdc*. The three graphs show, respectively, the estimated buffer capacity distributions for nonuniform and uniform models, the actual buffer usage distribution for uniform model and the relative errors. We can see from Figures 5(a) that the distribution curve for the nonuniform distribution is of a "bell curve" form, but with a flat region in the center and a sharp dropoff near the boundary. Thus it does not deviate much from an average uniform distribution as shown in the figure. This property makes it reasonable to use a uniform buffer distribution based on the average of the nonuniform distribution, but still get good buffer usage and small buffer overflow. Figure 5(b) shows that the distribution of the actual buffer usage under the uniform buffer distribution model. For this and all other benchmarks, the general trend is that the usage of buffers fits the uniform buffer capacity well in most part of circuits, but less buffers are used at the periphery. This is due to the fact there is generally less interconnect wires at periphery. In practice, we may preallocate some buffer areas on periphery to be decoupling capacitors to save some resources. The relative error curve in Figure 5(c) shows that the estimated buffer capacity is generally a little higher than the actual buffer number, because our estimation is aimed at the maximum buffer capacity for a range of circuits, and naturally builds in some pessimism. For the most part, this error is less than 20%, which shows that our *a priori* buffer distribution estimation provides an economic solution.

In this paper, we have presented a practical distributed length-based buffer insertion model for structured ASIC design. Based on this model, we have proposed an early statistical buffer distribution estimation. Experimental results show it can accurately and economically plan buffer resources on structured ASIC chip.

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