# Deep Trench Capacitor based Step-up and Step-down DC/DC Converters in 32nm SOI with Opportunistic Current Borrowing and Fast DVFS Capabilities

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*Abstract*-**A switched capacitor step-down converter fabricated in 32nm CMOS achieves a 5X improvement in response time for fast dynamic voltage and frequency scaling (DVFS). We also present a step-up converter based on a bi-directional voltage doubler, which is capable of reducing supply noise up to 45% by opportunistically borrowing current from adjacent idle power domains. Using ultra-high density deep trench capacitors, we are able to achieve an output power density of 2.78W/mm$^2$ at a peak efficiency of 85% from the step-down converter and 0.9W/mm$^2$ at a peak efficiency of 82% from the voltage doubler.**

## I. INTRODUCTION

DVFS has become a popular approach to improve the performance of microprocessors, especially for multi-core multi-power domain processors, while keeping an acceptable power consumption budget. However, long voltage switching time and large supply noise are major performance limiting factors of per-core or per-cluster DVFS. In this paper, we propose a circuit technique based on switched capacitor DC/DC step-down converter to improve DVFS response time significantly. We also propose to use switched capacitor DC/DC step-up converter for supply noise reduction in a multi-power domain scenario by implementing a bi-directional opportunistic current borrowing scheme. Deep trench capacitors, which can be associated with "More-than-Moore" paradigm of ITRS roadmap, are used in our proposed DC/DC converters as flying capacitors. Originally meant for high density embedded memory applications, deep trench capacitors are slowly finding their ways into real systems, e.g. they are being used in DC/DC converters [1], PLL loop filters [2], decoupling circuitry [3] etc. Because of their inherent 3-D nature, large capacitance can be realized using a significantly smaller silicon footprint as compared to a metal-oxide-semiconductor (MOS)/ metal-insulator-metal (MIM) capacitors. They are more than 100X denser than MOS capacitors, and hence can show significant improvement in power density when used in DC/DC converters [1].

## II. DEEP TRENCH CAPACITORS AS FLYING CAPACITORS

Fig. 1 shows a cross-sectional view of a deep trench capacitor along with a 4x4 deep-trench array layout with trenches and contacts highlighted. Sidewalls of silicon (Si) trenches are arsenic (As) implanted to form the bottom plate of the capacitor, on top of which high-k dielectric materials are deposited. Finally, the trenches are refilled with As-doped polysilicon, which form the top electrode of the capacitor [4].

Large capacitor density of a deep trench capacitor comes with its large inherent series resistance, which is quite big in comparison to the equivalent series resistance (ESR) of MOS/MIM capacitors. Ref. [4] presents a distributed RC model in order to characterize trench capacitors.
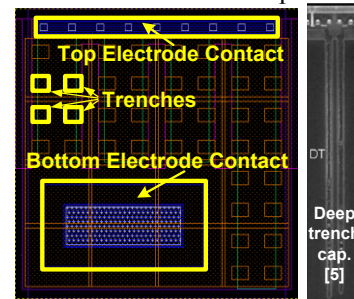


Fig. 1: Layout and cross-sectional view of a deep trench capacitor.

Trench fill resistance and plate resistance of the outer electrode are the sources of parasitic resistance of deep trench capacitors. To a first order approximation, a deep trench capacitor can be modeled as an ideal capacitance in series with an ESR, whose frequency responses are shown in Fig. 2(a). Because of the distributed nature of deep trench capacitors, ESR and $C_{ideal}$ are found to decrease at ultra high frequency, although they are practically frequency independent within our operating frequency range. However, because of the presence of large ESR, a deep-trench capacitor exhibits slower transients than an equivalent MOS capacitor, which is detrimental to high speed DVFS. Also, the presence of high
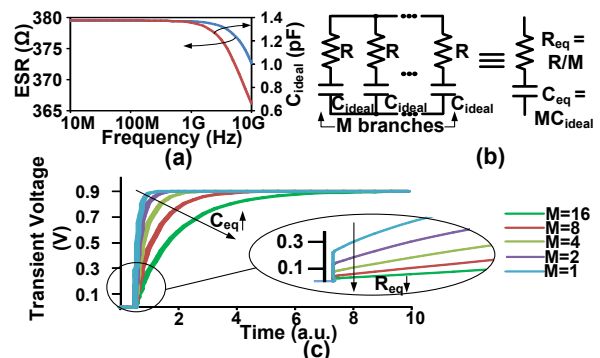


Fig. 2: (a) Frequency response of a deep trench capacitor (6x6 array). (b) ESR reduction with multiplicity. (c) Transient response of a deep trench capacitor as a function of capacitor multiplicity.

ESR affects the efficiency of deep trench capacitor based DC/DC converters adversely. However, in order to supply even a light load (~10μW), necessary flying capacitors can be

realized by connecting multiple deep trench arrays in parallel, which in turn lowers the effective series resistance of the structure by a factor of multiplicity of the arrays as shown in Fig. 2 (b). Fig. 2 (c) shows transient response of a deep trench capacitor as a function of the multiplicity (M) of the capacitor. Although our design is virtually insensitive to the high ESR associated with a deep trench capacitor array, designers should carefully consider the impact of high series resistance on circuit performance before using deep trench capacitors.

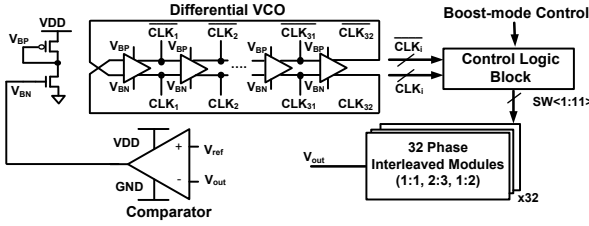### III. FAST DVFS SCHEME USING BOOST MODE



Fig. 3: Block diagram of step-down converter in a feedback control loop.

Block diagram of proposed step-down converter has been shown in Fig. 3. 32 converter modules operate in a time-interleaved manner in order to ensure smaller output ripple. The voltage request sent by the microprocessor ($V_{ref}$) is compared with the output voltage of the converter ($V_{out}$). Output of the comparator provides proper bias to a voltage-controlled oscillator (VCO) to generate multi-phase complementary clock signals which drive the step-down converter. The number of stages of the VCO is selected as large as possible to achieve better multi-phase interleaving for the step-down converter block. On the other hand, it should also satisfy the requirement of the maximum operating frequency, which is determined by the trade-off between power density and efficiency. The power consumption of the VCO needs to be minimized to optimize the overall efficiency of the proposed converter. Proposed reconfigurable step-down converter using deep trench capacitor is capable of generating $V_{out}$ with conversion ratios 1:1, 2:3 and 1:2. The usefulness to generate three voltage ratios from a single converter is that, it can cover a greater range of output voltage without sacrificing efficiency significantly. Schematic of a step-down converter module along with its switch configurations to generate above-mentioned output ratios are shown in Fig. 4.



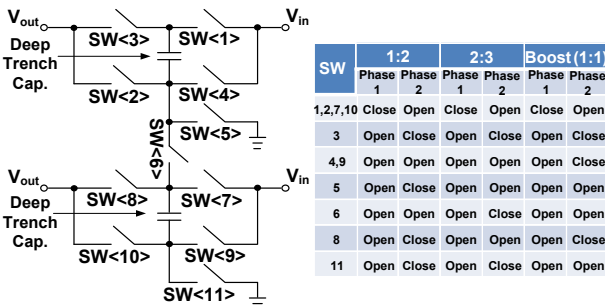| SW | 1:2 | | 2:3 | | Boost (1:1) | |
|---|---|---|---|---|---|---|
| | Phase 1 | Phase 2 | Phase 1 | Phase 2 | Phase 1 | Phase 2 |
| 1,2,7,10 | Close | Open | Close | Open | Close | Open |
| 3 | Open | Close | Open | Close | Open | Close |
| 4,9 | Open | Open | Open | Open | Open | Close |
| 5 | Open | Close | Open | Open | Open | Open |
| 6 | Open | Open | Open | Close | Open | Open |
| 8 | Open | Close | Open | Open | Open | Close |
| 11 | Open | Close | Open | Close | Open | Open |

Fig. 4: Basic step-down converter module showing switch configurations for different conversion ratios.

Our fast DVFS scheme using step-down converter has been explained in the flowchart shown in Fig. 5. Sluggish response

due to voltage level rise during DVFS can be attributed to the charging time of the large output load, which can be greatly reduced by pumping more charge during voltage rise transient. With each request to raise the output voltage level, control logic of the step-down converter configures itself to 1:1 ratio. Since the amount of charge delivered per unit time using 1:1 configuration is maximum compared to the charge delivered using other smaller ratios, time required to charge output load reduces. However, once the converter reaches desired voltage level, switches are reconfigured according to the closest higher output configuration in order to ensure high efficiency.
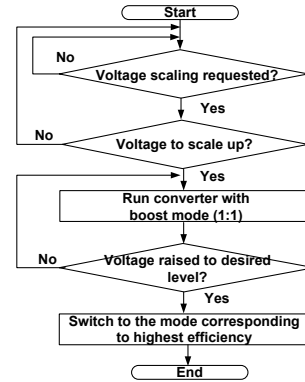


Fig. 5: Proposed fast DVFS control scheme with boost mode operation.

### IV. SUPPLY NOISE REDUCTION BY OPPORTUNISTIC CURRENT BORROWING

Proposed supply noise reduction technique works on the basis of borrowing current from adjacent idle/lightly loaded cores and dumping it to an active core. Although borrowed current will lead to an extra IR drop on adjacent cores, performance degradation in those cores will be negligible since those cores are running under light-load condition. One thing to note here is that the supply voltage of the adjacent idle cores can be lower than that of the active core due to the nature of DVFS. Therefore, the voltage levels of the idle cores must be boosted before they can provide current to the active core. Based on this observation, we propose to use a step-up converter, which uses deep trench capacitors as flying capacitors, to achieve this goal. Fig. 6 (a) shows the step-up converter consisting of voltage doubling units, a differential VCO for generating multiphase clock and a comparator connected in a feedback loop. Modified Favrat cells (Fig. 6 (b)) are used for bi-directional voltage doubling [6].
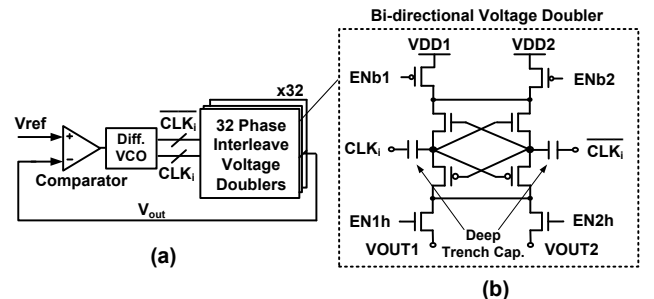


Fig. 6: (a) Step-up converter block diagram with feedback and (b) Modified Favrat cell for bi-directional voltage doubling.
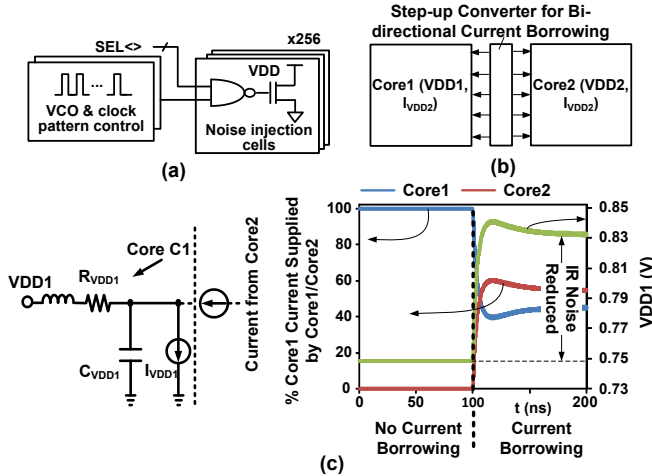
Fig. 7: (a) On-chip supply noise generation circuits for test purposes. (b) Per-core DVFS architecture with proposed opportunistic current borrowing step-up converter. (c) Equivalent circuit and simulation waveforms explaining proposed current borrowing scheme.

As shown in Fig. 7 (a), core replica circuits consist of a number of noise injection blocks whose turn-on times can be precisely controlled. These noise injection blocks are clocked by an on-chip VCO, and they are able to generate noise of different patterns and amplitudes. Two different power domains (VDD1, $I_{VDD1}$ and VDD2, $I_{VDD2}$) (Fig. 7 (b)) interact with each other with the help of the voltage doubler placed between them. By controlling switches (EN1h, EN2h, ENb1, ENb2) of the bi-directional voltage doubler unit cell shown in Fig. 6 (b), it can work in three different modes: (1) VDD1 provides current to boost VDD2; (2) VDD2 provides current to boost VDD1; (3) and a disabled mode. This flexibility in supplying current through multiple power domains provides an additional control knob which helps improve the overall power efficiency of the processor. Equivalent circuit and simulation waveforms showing IR noise reduction of core1 by borrowing current from core2 have been presented in Fig. 7(c).

## V. DEEP TRENCH CAPACITOR BASED CONVERTER MEASUREMENTS

Open-loop efficiency vs. $V_{out}$ and open-loop efficiency vs. power density plots of step-down and step-up converters are shown in Fig. 8(a) and Fig. 8(b), respectively. Efficiency plots for the step-down and the step-up converters are obtained at optimum frequencies of 110MHz and 24MHz, respectively. Efficiency vs. $V_{out}$ plots for various input voltage levels ($V_{in}$) of the step-up converter show largest efficiency with smallest $V_{in}$ for $V_{out}$ in the range between 0.7V and 1.0V. This implies that for a nominal supply voltage of 0.9V of the active core, the smaller the supply voltage of the idle core is, the better the efficiency of the current borrowing scheme will be. With an input voltage of 0.9V, the step-up converter is able to deliver a power density of 0.9W/mm$^2$ at a peak efficiency of 82% while maintaining efficiency over 70% throughout the voltage range from 1.25V to 1.73V. Step-down converter, on the other hand, uses an input voltage of 1.5V, and is capable of delivering 2.78W/mm$^2$ at a peak efficiency of 85% when it is configured

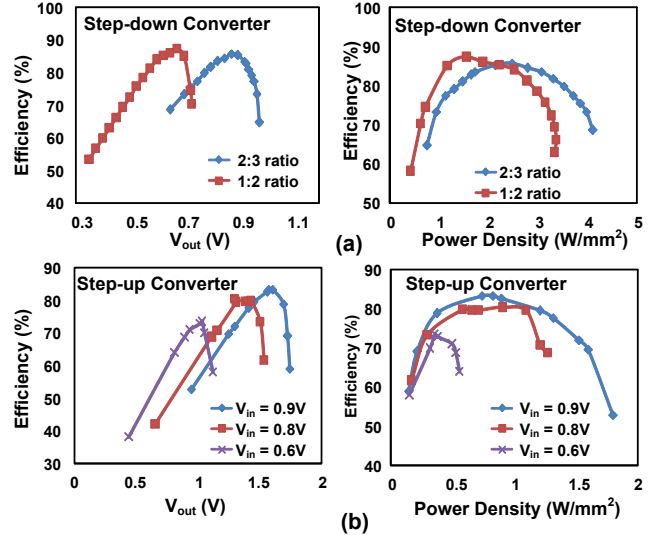as 2:3. It has efficiency over 70% in the voltage range from 0.5V to 0.98V.



Fig. 8: Open-loop efficiency vs. $V_{out}$ and open-loop efficiency vs. power density for (a) step-down converter at 110MHz and (b) step-up converter at 24MHz.

Closed-loop efficiency vs. $V_{out}$ plots of the step-up and step-down converters assuming ring oscillator loads are shown in Fig. 9. Closed-loop efficiency numbers take the loss in the feedback control loop into account, and hence are smaller compared to their open-loop counterpart.
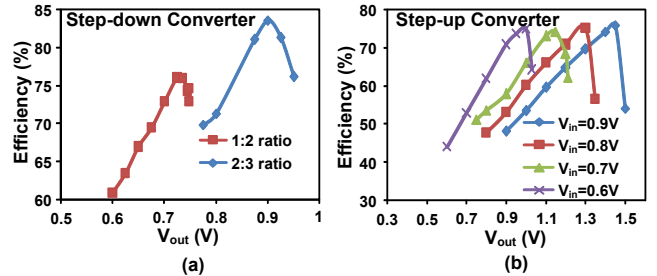


Fig. 9: Closed-loop efficiency vs. $V_{out}$ of (a) step-down and (b) step-up converter.

In order to evaluate proposed current borrowing scheme for IR noise reduction, we have plotted percentage improvement in noise as a function of supply voltage levels of idle core for various VCO frequencies of the step-up converter (Fig. 10 (a)), and as a function of power budget for various supply voltage levels of the idle core (Fig. 10 (b)). Larger VCO frequency leads to faster charge transfer to the active core, whereas limited power budget poses a current limit on the idle
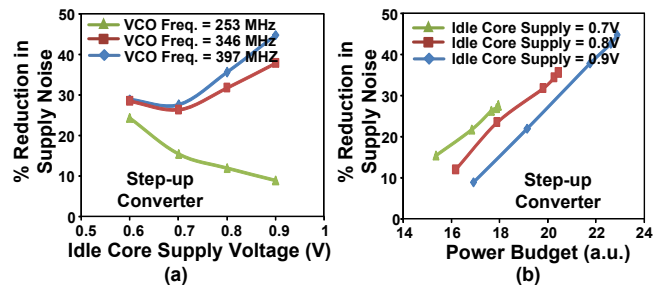


Fig. 10: (a) Percentage reduction in supply noise vs. idle core supply voltage and (b) Percentage reduction in supply noise vs. power budget.

core, thereby limiting percentage noise improvement.

Measurement results for fast DVFS scheme have been shown by the voltage transients for constant initial and different final voltage levels (top left of Fig. 11), constant final and different initial voltage levels (bottom left of Fig. 11). Ratio of switching time with no-boost scheme and with boost scheme has been plotted as a function of varying final voltage (top right of Fig. 11) and varying initial voltage (bottom right of Fig. 11). We get 5X improvement in switching time for the case when $V_{out}$ rises from 0.5V to 0.9V.
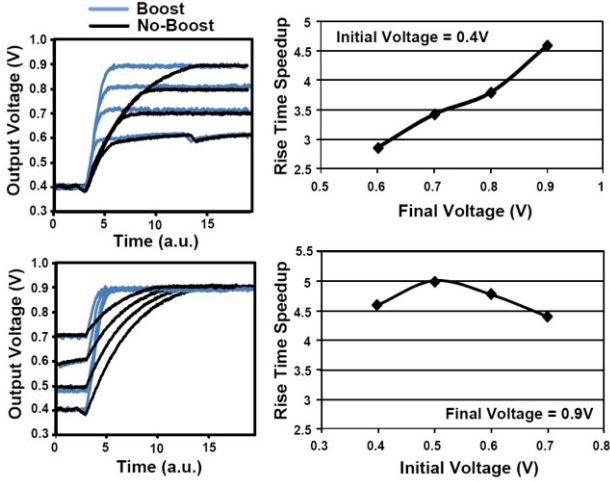


Fig. 11: Measured waveforms showing rise transients of step-down converter with and without boost mode (left). Rise time speedup as functions of final $V_{out}$ and initial $V_{out}$ (right).

Test chip microphotographs highlighting major blocks of the step-up and step-down converters are shown in Fig. 12 alongside the unit cell layouts.
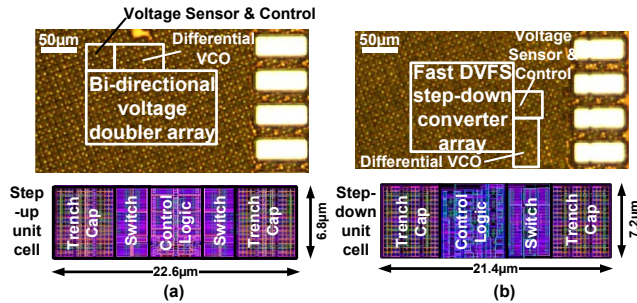


Fig. 12: Test chip microphotographs of (a) step-up and (b) step-down converters in 32nm SOI with unit converter cell layout.

A summary of our step-up and step-down converters and their performance in comparison to the current state-of-the art switched capacitor converters are tabulated in Table I.

## VI. CONCLUSION

We have presented switched capacitor based step-down and step-up converters using deep trench capacitors as flying capacitors. Simulation results have verified that with larger multiplicity of deep trench capacitors, effective ESR reduces by the same factor, and its effect on switching transient of the converter becomes negligible. We have designed the step-down converter for high speed DVFS by operating the

converter with highest possible ratio (1:1 in our case) during rise transient of output voltage. On the other hand, step-up converter has been implemented for IR noise reduction of a core by borrowing current opportunistically from adjacent low activity cores. Measured data from a 32-nm test chip have shown a power density of $0.9W/mm^2$ at a peak efficiency of 82% from the proposed step-up converter, and a power density of $2.78W/mm^2$ at a peak efficiency of 85% from the proposed step-down converter. We have measured 45% reduction in IR noise using opportunistic current borrowing scheme, which can further be improved with larger VCO frequencies, although the power budget will act as a bottleneck at higher frequencies. From the test chip, a 5X improvement in rise transient has also been measured when $V_{out}$ of the step-down converter is made to change from 0.5V to 0.9V.

TABLE I
COMPARISON WITH RECENT SWITCHED CAPACITOR CONVERTER DESIGNS

| | Tech. Node | Flying Cap. | Operating Modes | Feedback Control Loop | Max. Eff. | Power Density at Max. Eff. | Additio-nal Circuit Feature |
|---|---|---|---|---|---|---|---|
| [1] | 45nm SOI | Deep Trench Cap. | 2:1 Step-up & 1:2 Step-down | No | 90% | 2.3W/mm² | None |
| [7] | 32nm SOI | MOS Cap. | 2:3, 1:2, 1:3 Step-down | No | 81% | 0.55W/mm² | None |
| [8] | 32nm Bulk | Metal Finger Cap. | 2:1 Step-up | No | 60% | 1.12W/mm² | None |
| This work | 32nm SOI | Deep Trench Cap. | 2:1 Step-up & 1:2, 2:3, 1:1 Step-down | Yes | 85% | 2.78W/mm² for 2:3 ratio | Fast DVFS, IR noise reduction |

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