Analyzing the Electromigration Effects on Different Metal Layers and Different Wire Lengths

Gracieli Posser*, Vivek Mishra†, Ricardo Reis*, Sachin S. Sapatnekar†

*Universidade Federal do Rio Grande do Sul (UFRGS)
Instituto de Informática - PPGC/PGMicro
Av. Bento Gonçalves 9500 Porto Alegre, RS - Brazil
Email: {gposser,reis}@inf.ufrgs.br

†Department of Electrical and Computer Engineering
University of Minnesota
Minneapolis, MN 55455
Email: {vivek,sachin}@umn.edu

***Abstract*—Electromigration (EM) is a significant problem in integrated circuits and can seriously damage interconnect wires and vias, reducing the circuit's lifetime. In this paper we are testing the EM effects on 6 different metal layers for different wire lengths. The layouts are constructed considering the 45nm technology and scaled to 22nm technology. We are testing the EM effects considering three different wire lengths, 100μm, 200μm and 300μm in 22nm technology. The delay is also analyzed and it increases when the wire length increases and decreases for a higher metal layer.**

I. Introduction

Electromigration (EM) is a critical reliability concern, [1] causing shorts and voids in metal interconnects, leading to failures of the interconnects and decreasing the time to failure (TTF) of the circuits. EM affects global and local interconnects and is becoming a progressively increasing concern as feature sizes shrink and designs grow more complex [2].

EM is initiated by the flow of current through metal wires: the drift of metal atoms along with the flow of electrons causes a depletion of the upstream metal and a deposition of metal downstream along the current flow direction. The upstream thinning increases the wire resistance and could ultimately result in open-circuit failures, as the first example in Figure 1 presents. While the downstream deposition may cause short-circuit failure to the nearby metal, as the second example in Figure 1. Consequently, the EM effects slow down the circuit through time, and in the worst case can lead to the eventual loss of one or more connections and an intermittent failure of the entire circuit [3].

The focus of this work is on the analysis of the EM effects on different metal layers and different wire lengths for signal wires connecting standard-cells. Our specific contributions are as follows:

- To show how the EM affects different metal layers and different wire lengths.
- To analyze the delay behavior for the different metal layers and wire lengths.

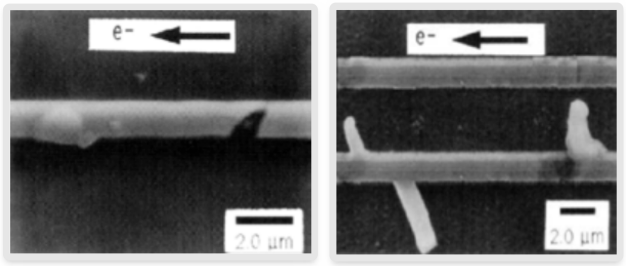

Figure 1. Void (open circuit) and hillock (short circuit) [4].

- To present how the average current I_{avg} reduces through the wire.

The rest of this paper is organized as follows. Section II presents a brief description about the AC electromigration presents in signal wires. Section III describes the model used in this work to calculate the EM lifetime where the Joule heating is incorporated. The experimental analysis flow is discussed in Section IV and the experimental results are presented in Section V. Finally, the conclusions and future works are shown in Section VI.

II. AC Electromigration

Traditionally, EM has been a significant concern in power delivery networks, referred to as DC electromigration. The reason for this is that the current flow is generally unidirectional and the EM causes a unidirectional migration of the metal atoms.

Of late, it has become increasingly important to consider the effects of electromigration in signal wires, where the direction of current flow is bidirectional. For this reason, this is often referred to as *AC electromigration*. The AC electromigration has become a serious concern and its limits become tighter with the technology scaling due to the increasing of the on-current of drivers with smaller channel lengths, the decreasing of the interconnect widths and a faster switching of the transistors increasing the operation frequency [5]. Thus,

this work touch upon the EM effects on signal interconnects considering different metal layers and different wire lengths.

A. Average current calculation

Currents in signal interconnects must necessarily flow in both directions (as they charge and discharge the output load). Therefore, the motion of atoms in one direction under one direction of current flow is negated by the "sweep-back" effect that moves atoms in the opposite direction when the current flow is reversed. However, even in cases where the current in both directions is identical, it is observed that EM effects are manifested. This is because a reverse-direction current only allows partial recovery of the EM degradation due to forward-direction current, and this effect is often referred to as recovery. This effect is captured by an effective average current, I_{avg} [6], [7], as:

$$I_{avg} = I^{+}_{avg} - \mathcal{R} \cdot I^{-}_{avg}, \tag{1}$$

where I^{+}_{avg} is the foward-direction current (larger of the currents), I^{-}_{avg} is the average reverse-direction current (smaller current), and $\mathcal{R}$ represents the *recovery factor* that captures the sweep-back effect due to reverse current. In this work, we use a recovery factor $\mathcal{R}$ of 0.7 [6]. When the current is unidirectional the value of I_{avg} is simply the time average of the current.

III. EM MODELING

The EM lifetime estimation is computed using the well-known Black's equation [8], given by:

$$TTF = A\, J^{-n} \exp\left(\frac{Q}{k_B T_m}\right) \tag{2}$$

where TTF is the time-to-failure, A is an empirical constant that depends on the material properties of the interconnect, J is the current density, the exponent n is typically between 1 and 2, Q is the activation energy, k_B is Boltzmann's constant and T_m is the metal temperature. In this work, the value of $A = 1.47 \times 10^7$As/m^2 in SI units, which corresponds to an allowable current density of 10^{10} A/m^2 over a lifetime of 10 years at 378K, with an activation energy, $Q = 0.85$eV [9].

The current density is given by $J = I_{avg}/(T_w \cdot W)$, where T_w is the wire thickness, W is the wire width, and I_{avg} is the average current. The I_{avg}, in this work, is calculated by Eq. 1 as we are considering signal interconnections and the current is bidirectional.

A. Joule Heating

The flow of current in an interconnect results in the dissipation of power within the resistance of the wire. This leads to an increase in temperature within the wire, a phenomenon known as Joule heating or self-heating. The TTF for EM depends on the metal temperature, T_m, in Eq. (2), and it is clearly seen from the equation that a temperature rise hastens the time to failure of the wire. Therefore, our approach incorporates Joule heating effects for modeling EM. The value of T_m used in Eq. (2) is given by:

$$T_m = T_{ref} + \Delta T_{Joule} \tag{3}$$

where T_{ref} is the reference chip temperature specified for EM (378K in this work), and ΔT_{Joule} is the temperature rise due to Joule heating.

In this work, we use the thermal model from [10] to compute Joule heating. Under steady-state thermal conditions, the temperature rise in the wire can be calculated as:

$$\Delta T_{Joule} = I^2_{rms} R R_\theta \tag{4}$$

where I_{rms} is the root mean square (RMS) current in the wire, R is the wire resistance, and $R_\theta = t_{ins}/\left(K_{ins} L W_{eff}\right)$ is the thermal impedance of the wire to the substrate, where t_{ins} is the dielectric thickness, K_{ins} is the thermal conductivity normal to the plane of the dielectric, L is the wire length, and $W_{eff} = W + 0.88 t_{ins}$, for a wire width W.

We obtain I_{rms} by SPICE characterization. R is obtained by parasitic extraction using a commercial tool, t_{ins} changes for different metal layers, as Table I shows, and $K_{ins} = 0.07$W/m.K [10].

IV. EXPERIMENTAL SETUP

The objective of this work is to present the EM effects in different metal layers considering different wire lengths. For this, the layout presented in Figure 2 is the test case used to run the experiments. The layout is composed by two INV_X16 from the 45nm NANGATE Open cell library [11] connected by a net (wire). In the tests, we are changing the metal layer and the wire length of this net. The width of this net is the minimum value given by the technology, as Table I presents. For each metal layer and different wire length, a different layout is constructed and the parasitics are extracted using a commercial tool. The parasitic extractor divides the wire into a number of wire segments. Thus, a separate TTF is calculated for each wire segment and the worst TTF is considered. The worst TTF is the TTF of the closest segment of the first INV_X16 , this is because the parasitics of each segment reduce the current through the next segment.

Table I presents the wire width (W), the wire thickness (T_w) and the dielectric thickness t_{ins} considered in our tests based on the values from 45nm technology [12] and the scaled values to 22nm technology.

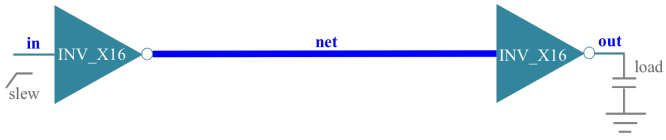

Figure 2. Layout used to analyze the characteristics for different metal layers with different wire lengths.

Table I. WIRE WIDTH (W), WIRE THICKNESS (T_w) AND THE DIELECTRIC THICKNESS t_{ins} BASED ON THE VALUES FROM 45NM TECHNOLOGY [12] AND THE VALUES SCALED TO 22NM TECHNOLOGY.

Metal layers	45nm technology			22nm technology		
	W (nm)	T_w (nm)	t_{ins} (nm)	W (nm)	T_w (nm)	t_{ins} (nm)
M1	70	130	120	34	64	59
M2	70	140	120	34	68	59
M3	70	140	120	34	68	59
M4	140	280	290	68	137	142
M5	140	280	290	68	137	142
M6	140	280	290	68	137	142

The tests are executed considering the layout shown in Figure 2. The structure of this layout is kept; just the wire

Table II. INPUT SLEW, OUTPUT LOAD, TTF AND THE TTF REDUCTION WHEN THE WIRE (NET) LENGTH OF THE LAYOUT PRESENTED IN FIGURE 2 IS CHANGED FROM $100\mu m$ TO $200\mu m$ AND FROM $200\mu m$ TO $300\mu m$.

Metal	Input slew (ps)			Output load (fF)			TTF (years)			TTF reduction (%)	
layers	$100\mu m$	$200\mu m$	$300\mu m$	$100\mu m$	$200\mu m$	$300\mu m$	$100\mu m$	$200\mu m$	$300\mu m$	$\frac{200\mu m}{100\mu m}$	$\frac{300\mu m}{200\mu m}$
M1	1.2	1.2	1.2	0.60	0.60	0.60	8.59	5.71	5.49	**33.53**	**3.85**
M2	1.2	1.2	1.2	0.60	0.60	1.20	11.06	6.94	5.50	**37.25**	**20.75**
M3	1.2	1.2	1.2	0.60	0.60	0.60	13.10	8.54	6.85	**34.81**	**19.79**
M4	1.2	1.2	1.2	2.00	0.60	0.60	52.52	33.00	23.89	**37.17**	**27.61**
M5	1.2	1.2	1.2	2.00	0.60	0.60	58.90	38.88	28.75	**33.99**	**26.05**
M6	1.2	1.2	1.2	2.00	0.60	7.50	63.00	42.82	31.99	**32.03**	**25.29**

length and the metal layer of the net are changed. The layouts are scaled from the 45nm Nangate cell library down to 22nm technology. In 45nm, the wire lengths used in the layout are 200μm, 400μm and 600μm. Scaling to 22nm technology, these wire lengths will be about 100μm, 200μm and 300μm. SPICE simulation is used to characterize the layout for I_{avg} and I_{rms} values considering 2GHz as a reference frequency and a temperature of 378K. The simulations are of the scaled 22nm library based on the 22nm SPICE ASU PTM model for High Performance applications (PTM HP), and the supply voltage (VDD) used is 0.88V.

The layout is characterized for 7 different values each for the input slew and output load, generating a 7×7 look-up table with the RMS and average current values. The input slew values are applied to the in signal that is the input of the first inverter in the Figure 1. The output load is the capacitance connected to the out signal, i.e., to the output of the second INV_X16. In this way, the output load of the first INV_X16 is a combination of the net capacitance plus the capacitance of the second INV_X16 plus the output load connected to the second INV_X16. The maximum input slew and output load values are determined based on SPICE simulation. They are limited by the largest values that enable the out signal to reach the VDD value and to get an output transition time smaller than the maximum input slew, defined as $198.5ps$. The other constraints are the minimum input slew, defined as $1.2ps$ and the minimum output load, equal to $0.6fF$, which is an approximation of the input capacitance of the inverter with size 1 scaled from the 45nm technology to the 22nm technology. The TTF values are calculated considering just the current through the wire, the TTF of the vias is not calculated.

V. EXPERIMENTAL RESULTS

The results presented in this section are considering the layout shown in Figure 2. Table II presents the worst TTF for a combination of allowable input slew and output load and the conditions where it occurs, i.e., the input slew and the output load of the worst TTF. Moreover, the TTF reduction is also shown for the conditions when the wire length that connects the two INV_X16 in the Figure 2 is increased from 100μm to 200μm and from 200μm to 300μm in 22nm technology. The input slew for the worst TTF was the same for all test cases, and this is the minimum input slew we are using. This is expected because as faster is the input transition, larger is the provided current reducing the TTF. The output load presented in the table is that connected to the second INV_X16 in Figure 2 and its value for the worst TTF is always larger than the constraint $0.6fF$.

About the EM effects, Table II shows that as lower is the metal layer, lower is the lifetime of the wire. Considering that traditional IC implementation flows have an intended TTF of at least 10 years [5] [2], there are some TTF values in the table smaller than 10 years. And we are considering the test cases with a TTF smaller than 10 years as critical. The wires in metal 1 are all critical, where the criticality is increased as the wire length increases. The wires in metal 2 and metal 3 have a critical TTF for a wire length of 200μm and 300μm, for a wire length of 100μm the TTF is larger than 10 years. For the metal layers 4, 5 and 6 the TTF is not critical for the wire lengths we are considering in this work, where the smallest TTF for these metal layers is 23.89 years for a wire length of 300μm. The TTF reduction when the wire length is increased from 100μm to 200μm is about 35% and from 200μm to 300μm the TTF is reduced from 3.85% to 27.61%.

Our tests show that the TTF is smaller for lower metal layers, even when the metal layers have the same wire width, wire length and wire thickness. One reason for this is the parasitic capacitance on the wire. Looking the parasitic extraction file, as possible to see that the parasitic capacitances are larger as lower is the metal layer.

Figure 3 shows the delay (ps) by metal layers considering the three different wire lengths 100μm, 200μm and 300μm of the test cases presented in Table II. The figure shows that the delay increases as the wire length increases. Furthermore, as higher is the metal layer, smaller is the delay.

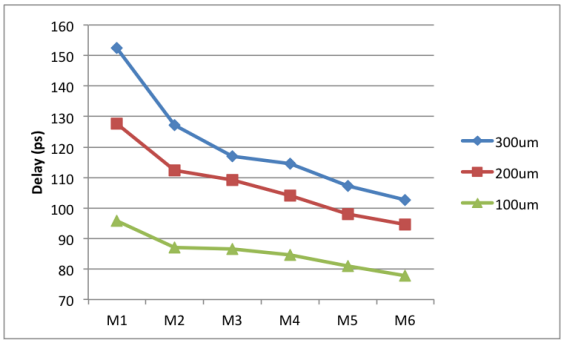

Figure 3. Delay (ps) by metal layers considering the three different wire lengths in 22nm 100μm, 200μm and 300μm.

Table III presents the maximum input slew and the maximum output transition time (tt) from 5% to 95% (95%-5%) of the output signal in ps for the different metal layers and wire lengths tested in this work. The maximum input slew we are considering, $198.5ps$, is about 40% of the clock period ($500ps$). All the maximum output transition time values shown in Table III are smaller than the maximum input slew. Thus, the second inverter is able to load other cells and wires since

Table IV. THE EFFECTIVE AVERAGE CURRENT (I_{avg}) IN μA AT THE POINT WHERE THE NET STARTS (INITIAL) AND AT THE POINT WHERE THE NET ENDS (END) FOR THE DIFFERENT WIRE LENGTHS AND THE I_{avg} REDUCTION (RED.) IN $\times$ AND THE I_{avg} REDUCTION AT THE BEGIN AND END POINTS WHEN THE WIRE LENGTH IS INCREASED.

Metal layers	100μm			200μm			300μm			Initial comparison (%)			End comparison (%)		
	Initial	End	Red. ($\times$)	Initial	End	Red. ($\times$)	Initial	End	Red. ($\times$)	$\frac{200\mu m}{100\mu m}$	$\frac{300\mu m}{200\mu m}$	$\frac{300\mu m}{100\mu m}$	$\frac{200\mu m}{100\mu m}$	$\frac{300\mu m}{200\mu m}$	$\frac{300\mu m}{100\mu m}$
M1	15.5	6.87	**2.26**	21.9	6.27	**3.49**	25.3	5.48	**4.62**	41.3	15.5	63.2	8.7	12.6	20.2
M2	14.4	6.97	**2.07**	21.0	6.71	**2.22**	25.6	6.11	**4.19**	45.8	21.9	77.8	3.7	8.9	12.3
M3	13.1	6.94	**1.89**	18.7	6.73	**2.78**	22.6	6.20	**3.65**	42.8	20.9	72.5	3.0	7.9	10.7
M4	14.5	7.03	**2.06**	21.1	6.85	**3.08**	27.4	6.63	**4.13**	45.5	29.9	89.0	2.6	3.2	5.7
M5	13.2	7.04	**1.88**	18.7	6.88	**2.72**	24.0	6.71	**3.58**	41.7	28.3	81.8	2.3	2.5	4.7
M6	12.5	7.06	**1.77**	17.4	6.89	**2.53**	22.3	6.69	**3.33**	39.2	28.2	78.4	2.4	2.9	5.2

Table III. MAX INPUT SLEW AND MAX OUTPUT TRANSITION TIME (TT) FOR THE DIFFERENT METAL LAYERS AND WIRE LENGTHS USED IN THIS WORK.

Metal layers	100μm		200μm		300μm	
	input slew (ps)	output tt (ps)	input slew (ps)	output tt (ps)	input slew (ps)	output tt (ps)
M1	198.5	142.4	198.5	155.1	17.2	197.2
M2	198.5	144.0	198.5	155.6	130.0	174.0
M3	198.5	142.6	198.5	156.6	180.0	161.8
M4	198.5	142.4	198.5	162.5	198.5	171.0
M5	198.5	137.9	198.5	160.5	198.5	172.1
M6	198.5	130.6	198.5	160.3	198.5	170.0

the output signal can reach the VDD value and the output transition time is respected. For metals 1 and 2 and 3 and wire length of 300μm, the input slew has to be smaller than the maximum value because using larger input slew than the values presented in the table the output transition time constraint is not respect.

Table IV presents the effective average current I_{avg} in μm, calculated by equation 1, for the tests presented in Table II, i.e., for that input slew and output load. Table presents the I_{avg} value at the point where the net starts (initial), that is the point connected to the via that is connected to the output of the first INV_X16. And the average current at the point where the net ends (end), that is the point connected to the via that is connected to the input of the second INV_X16 in the Figure 2. The average current reduces significantly along the wire. For a wire with 100μm, the current reduces from 1.77 to 2.26$\times$ until reaching the via connected to the second inverter. The metal 1 has the largest current reduction. For a wire length of 200μm, the current is reduced from 2.22 to 3.49$\times$ along the wire. For a wire with 300μm, the current reduces from 3.33 to 4.62$\times$ through the wire.Table IV also shows that increasing the wire length, the I_{avg} current at the *initial* point reduces from 63.2 to 89% when the wire length is increased from 100μm to 300μm. At the end *point* of the wire, the I_{avg} current reduces from 4.7 to 20.2% increasing the wire length from 100μm to 300μm.

VI. CONCLUSION AND FUTURE WORK

This work has shown an analysis of the EM effects on different metal layers for different wire lengths. We can conclude that as lower is the metal layer, lower is the lifetime of the wire. Then, larger metal layers have smaller EM effects and consequently a higher lifetime of the wires. We are considering critical the nets with a TTF smaller than 10 years. The signal nets in metal 1 in out test cases for wire lengths of 100μm, 200μm and 300μm are critical and the lifetime is reduced as the wire length increases. The wires in metal 2 and metal 3 have a critical TTF for a wire length of 200μm and 300μm. For the metal layers 4, 5 and 6 the TTF is not critical for the wire lengths we are considering in this work.

The delay in our test cases increases when the wire length increases and decreases for a higher metal layer, i.e., as lower is the metal layer higher is the delay.

As a future work, we intend to evaluate the EM effects on the vias, comparing the effects for the different metal layer vias and considering the vias connected to different wire lengths.

REFERENCES

[1] K.-C. Wu, M.-C. Lee, D. Marculescu, and S.-C. Chang, "Mitigating lifetime underestimation: A system-level approach considering temperature variations and correlations between failure mechanisms," in *DATE, 2012*, March 2012, pp. 1269–1274.

[2] J. Lienig, "Electromigration and its impact on physical design in future technologies," in *Proceedings of the ACM International Symposium on Physical Design*, 2013, pp. 33–40.

[3] J. Xie, V. Narayanan, and Y. Xie, "Mitigating electromigration of power supply networks using bidirectional current stress," in *Proceedings of the Great Lakes Symposium on VLSI*, 2012, pp. 299–302.

[4] B. Geden, "Understand and avoid electromigration (em) & ir-drop in custom ip blocks," Nov 2011. [Online]. Available: http://www.synopsys.com/Tools/Verification/CapsuleModule/CustomSim-RA-wp.pdf

[5] A. Kahng, S. Nath, and T. Rosing, "On potential design impacts of electromigration awareness," in *Design Automation Conference (ASP-DAC), 2013 18th Asia and South Pacific*, Jan 2013, pp. 527–532.

[6] K.-D. Lee, "Electromigration recovery and short lead effect under bipolar- and unipolar-pulse current," in *Proceedings of the IEEE International Reliability Physics Symposium*, 2012, pp. 6.B.3.1–6.B.3.4.

[7] P. Jain and A. Jain, "Accurate current estimation for interconnect reliability analysis," *IEEE Transactions on VLSI Systems*, vol. 20, no. 9, pp. 1634–1644, 2012.

[8] J. R. Black, "Electromigration – a brief survey and some recent results," *IEEE Transactions on Electron Devices*, vol. ED-16, pp. 338–347, 1969.

[9] C.-K. Hu *et al.*, "Impact of Cu microstructure on electromigration reliability," in *International Interconnect Technology Conference, IEEE*, 2007, pp. 93–95.

[10] K. Banerjee and A. Mehrotra, "Global (interconnect) warming," *IEEE Circuits & Devices Magazine*, vol. 17, no. 5, pp. 16–32, Sept. 2001.

[11] "Nangate 45nm open cell library," http://www.nangate.com.

[12] FreePDK45, "Freepdk45 process design kit," 2011, http://www.eda.ncsu.edu/wiki/ FreePDK45:Contents.