# Physical Design Automation Challenges for 3D ICs

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***Abstract*— Recent advances in process technology have brought forth several options that have brought three-dimensional (3D) circuits within the realm of the possible and probable. This new design paradigm will require a major change in design methodologies, and an optimal 3D design will look very different from an optimal 2D design. Since the move from conventional 2D to 3D is inherently a topological change, it stands to reason that a number of 3D-specific problems lie in the domain of physical design. This paper addresses challenges related to physical design for 3D integrated circuits.**

## I. Introduction

With interconnect delays becoming the dominant factor in determining circuit performance, it has become important to use all possible means to negate their effects. Thanks to recent progress in fabrication technology, it has become possible to build circuits "upwards" in the third dimension to reduce the problem of congestion.

The need to densely pack circuits, and locate critical blocks as close as possible to each other, has led to the advent of three-dimensional (3D) technologies [1], with multiple tiers of devices stacked atop each other. The increased packing density improves the computation per unit volume, and results in diminished on-chip interconnect problems due to reduced parasitics. This curtailment in the parasitics is achieved by reductions in the average interconnect lengths (in comparison with 2D implementations, for the same circuit size), as well as by denser integration, which results in the replacement of chip-to-chip interconnections by intra-chip connections. Consequently, 3D integration can be an enabler for enhancements in system performance, power, reliability, and portability. Recent advances in industrial [2], government [3] and academic [4] research laboratories have demonstrated 3D designs with inter-tier separations of the order of a few microns.

Fundamentally, the problem of 3D design is related to topological arrangements of blocks, and therefore, physical design plays a natural role in determining the success of 3D design strategies. Physical design in the 3D realm requires a fresh approach, as new cost functions become important, and new design structures must be devised, and ordinary extensions of 2D approaches are unequal to the task of solving these problems.

## II. 3D-specific Physical Design

Physical design for 3D circuits includes problems related to floorplanning, placement and routing. An additional concern in chip-level 3D integration is related to the fact that a large number of active devices are packed into a much smaller area, so that the power density is much higher than in a corresponding 2D circuit. As a result, high levels of temperature build-up are possible unless thermal issues are given primacy among the set of design objectives.

During *placement*, cells are arranged in rows within the layout to achieve a reasonable temperature distribution, while also capturing traditional placement requirements. The challenges here lie in ensuring that all of the competing constraints are simultaneously satisfied, while also ensuring that the algorithms within the CAD tool are scalable and can handle large problem instances. A 3D placement technique, based on a force-directed paradigm, with embedded finite element-based thermal analysis, is presented in [5].

Although placement may try its utmost to equalize the distribution of temperature, it is either fundamentally unable to create an even thermal profile, or the tradeoffs with other optimization criteria, such as wirelength, may be unacceptably large. Even the best placement may not be able to meet a specific temperature criterion, simply because there is no escape path for the heat generated.

This issue is addressed by judiciously positioning *thermal vias* within the layout, which achieves improved heat removal. These vias correspond to inter-tier metal connections that have no electrical function, but instead, constitute a passive cooling technology that draws heat from the problem areas to the heat sink. Methods for optimal thermal via positioning have been presented in [6] as a post-placement optimization. However, the issue of thermal via placement is one that can be addressed at all levels of design, ranging from design planning right up to optimization.

A placed circuit must undergo a *routing* step to obtain a complete layout. During routing, several objectives and constraints must be taken into consideration, including avoiding blockages due to areas occupied by thermal vias, incorporating the effect of temperature on the delays of the routed wires, and of course, traditional objectives such as wire length, timing, congestion and routing completion. An algorithm for temperature-driven 3D routing, with integrated thermal via insertion, is presented in [7].

## III. Challenges

Current research has made a promising start to addressing the challenges of physical design for 3D ICs, but many issues remain to be resolved. Besides enhancing the efficiency of floorplanning, placement and routing methods, reliable power delivery in 3D designs is a significant bottleneck. In addition, as 3D technologies become more sophisticated, adding more layers, heterogeneous layers, or building systems with integrated analog/RF/digital components, physical design issues related to design complexity and noise mitigation will have to be addressed, while working under the constraints imposed by the underlying technology.

## References

[1] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A novel chip design for improving deep submicron interconnect performance and systems-on-chip integration," *Proceedings of the IEEE*, vol. 89, pp. 602–633, May 2001.

[2] K. W. Guarini *et al.*, "Electrical integrity of state-of-the-art 0.13$\mu$m SOI CMOS devices and circuits transferred for three-dimensional (3D) integrated circuit (IC) fabrication," in *Technical Digest of the IEEE International Electron Devices Meeting*, pp. 943–945, 2002.

[3] J. Burns, L. McIlrath, J. Hopwood, C. Keast, D. P. Vu, K.Warner, and P. Wyatt, "An SOI-based three dimensional integrated circuit technology," in *IEEE International SOI Conference*, pp. 20–21, Oct. 2000.

[4] R. Reif, A. Fan, K. N. Chen, and S. Das, "Fabrication technologies for three-dimensional integrated circuits," in *Proceedings of the International Symposium on Quality Electronic Design (ISQED)*, 2002.

[5] B. Goplen and S. S. Sapatnekar, "Efficient thermal placement of standard cells in 3D ICs using a force directed approach," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 86–89, 2003.

[6] B. Goplen and S. S. Sapatnekar, "Thermal via placement in 3D ICs," in *Proceedings of the ACM International Symposium on Physical Design*, 2005.

[7] T. Zhang and S. S. Sapatnekar, "Temperature-aware routing in 3D ICs," in *Proceedings of the Asia-South Pacific Design Automation Conference*, pp. 309–314, 2006.