Circuit Delay Variability Due to Wire Resistance Evolution Under AC Electromigration

Vivek Mishra and Sachin S. Sapatnekar
Department of Electrical and Computer Engineering
University of Minnesota
Minneapolis, MN, 55455, USA

***Abstract*—Electromigration (EM) in signal interconnects can induce voids, and the evolution of these voids may cause the wire resistance to increase with time. Previous approaches use the mean time to failure metric based either on a fixed resistance increase or open circuit failure criterion. This work shows that even noncatastrophic EM on critical paths may cause performance degradation, resulting in incorrect circuit operation. HSPICE-based Monte Carlo simulations on a set of on-chip structures are performed to quantify the impact of EM on circuit performance degradation.**

***Keywords*: AC EM analysis, delay, clock skew, technology scaling.**

I. Introduction

Electromigration (EM) is a significant problem in interconnects in nanometer-scale technologies. Due to the scaling of wire dimensions, current densities in successive technologies have increased [1] to the point that EM-induced void nucleation and growth may occur during product lifetimes, leading to significant performance shifts. In this work, we analyze such shifts caused by bidirectional (AC) EM in copper dual damascene (Cu DD) wires. We perform analyses on typical circuit topologies in on-chip signal and clock networks and link the physics of AC EM in Cu DD wires to circuit-level outcomes, i.e., circuit performance metrics that are meaningful to a designer, such as delay and clock skew.

Prior works on circuit-level EM primarily use Black's equation [2] and consider EM as a catastrophic failure. These are often based on a mean time to failure (MTTF) criterion that assumes that a wire will fail due to EM when its resistance increase crosses a threshold limit. Typically, this limit is the same for all wires. However, the change in circuit performance characteristics in a wire depends on its context. For some wires, it is possible that the circuit performance can degrade beyond the target specification before this limit, and others may function correctly even beyond the limit. For example, wires on timing-critical paths can only tolerate very small changes in delay, while wires on noncritical paths can tolerate larger resistance changes. A related idea has recently been explored in DC-EM-related works [3], [4] that directly study the impact of EM wire degradation on circuit performance parameter such as voltage (IR) drop. However, a circuit-performance-based AC EM analysis has not been proposed so far, and this is one contribution of our work.

We propose a paradigm for AC EM analysis aimed at capturing the effect of EM on circuit performance parameters such as delay and clock skew. We move beyond simple MTTF metrics and incorporate the circuit impact of wire resistance changes arising from EM void nucleation and growth [5], which is observed to be probabilistic [6], [7].

We employ a probabilistic wire resistance evolution model for AC EM. Under probabilistic resistance evolution, voids nucleate and grow, causing parametric changes in wire resistance over time, resulting in a probabilistic impact on circuit performance that causes a spread in the lifetimes of manufactured parts.

Besides quantifying the impact of EM probabilistic behavior, we incorporate the peculiarities in AC EM arising as a result of the flow of bidirectional currents. Unlike DC EM, where the electron wind force responsible for EM occurs only in one direction, the electron wind is bidirectional in AC EM, and causes incomplete recovery as metal migration occurs in both directions. Our analysis considers AC recovery [8] due to bidirectional current flow using a recovery factor.

We address recent experimental results on bidirectional currents, which show that void can be nucleated at both ends of a wire carrying an AC signal [9], [10]. We also include the effect of temperature rise due to local wire Joule heating, using the model from [11]. In addition, our analysis considers EM flux divergence [12], which models the impact of current flowing in neighboring wires on the EM atomic flux. Thus, we link the important facets of the mechanism of AC EM in Cu DD wires to circuit-level performance metrics.

We link our AC wire resistance evolution model and HSPICE-based circuit simulation to analyze parametric variations in circuit delay and clock skew arising as a result of probabilistic resistance increase due to void nucleation and growth. We consider typical on-chip circuit structures at multiple technology nodes and observe that AC EM causes not only catastrophic functional failures, but also parametric delay variations over the chip lifetime, an effect that becomes more acute in scaled technologies.

The paper is organized as follows: Section II describes an EM model that incorporates probabilistic resistance evolution, the peculiarities of AC EM, and the impact of bidirectional currents in neighboring wires. Section III describes our Monte Carlo simulation framework and Section IV presents our simulations that report the impact of EM on the performance of standard circuit structures in advanced technology nodes.

II. Modeling EM

As an EM-induced void evolves in a Cu DD wire, its resistance shows a temporal change. This is because the absence of Cu metal in a void spanning through the cross section of the wire forces more current to flow through the resistive Ta barrier layer and causes an increase in the effective wire resistance, which is proportional to the size of the void [13].

This resistance increase due to EM-induced voids will first change the circuit performance parameters such as the delay and eventually cause functional failure, when the circuit performance degrades beyond a threshold margin.

We model the EM-induced void physics based on [5], which assumes that the void evolution occurs in two steps: void nucleation, where the void begins to form, and void growth, where the nucleated void, increases in size as more metal atoms migrate in the direction of electron flow. A key factor influencing void evolution is the effective activation energy [14], E_a for EM void nucleation and growth: this is experimentally shown to be normally distributed between metal lines [7], [14]–[16]. Thus, resistance change under probabilistic void evolution must be modeled probabilistically.

A. Probabilistic DC EM resistance evolution

We build our AC EM framework based on the probabilistic resistance evolution model for DC EM [3]. Our starting point is the model for effective diffusivities for void nucleation and growth, D_{eff}, which show the Arrhenius relationship:

$$D_{eff} = D_0 \exp\left(\frac{E_a}{k_B\left(T_{ref} + \Delta T_J\right)}\right) \quad (1)$$

$$\Delta T_J = I_{rms}^2 R R_\theta \quad (2)$$

where D_0 is a constant, k_B is Boltzmann's constant, T_{ref} is the reference temperature, and ΔT_J is the local temperature rise due to Joule heating, which is modeled based on its RMS current, I_{rms}, resistance, R, and thermal impedance, R_θ [11]. Since E_a is normally distributed, D_{eff} is a lognormal.

For a given circuit operation time, t_o. The DC EM resistance model in [3] observes that:

- The time taken for the void to form, defined as the nucleation time, is inversely proportional to D_{eff} for the nucleation phase, and is hence a lognormal.
- After nucleation, the void grows and its length depends on the corresponding D_{eff}, t_o and the nucleation time.
- The void length is given by the difference of two lognormal functions, which can be approximated by another lognormal using standard techniques [17].
- The resistance increase due to EM-induced voids, being a linear function of void length [13], is also lognormal.

Thus, resistance increase due to an EM-induced void in a wire with DC current is lognormally distributed. This resistance change, ΔR, corresponding to an EM void in a wire is given by:

$$\Pr(\Delta R) = \Pr(\Delta R \mid \text{nuc}) \cdot \Pr(\text{nuc}) \quad (3)$$

where $\Pr(\text{nuc})$ is the probability of a nucleation event at a potential void site in a wire, and $\Pr(\Delta R \mid \text{nuc})$ is linearly related to the void length. Thus, the wire resistance increase is lognormally distributed with the statistics dependent on both process parameters that determine E_a and circuit parameters that determine the current through the wire.

B. AC EM peculiarities: Recovery and multiple void sites

For signal wires, the passage of AC current in opposite directions in a wire results in partial EM degradation and recovery. This is because the forward current flow in one direction changes the structural properties (grain boundary locations) of the wire [18], and the reverse current heals some of this restructuring. A recovery factor r models this [8], [19] and determines an "effective current density" for the signal wire, which corresponds to the equivalent DC current density for bidirectional signals. The expressions for DC EM are then used for AC EM modeling, with the effective current density replacing the DC current density.

However, it is important to emphasize that AC and DC EM are manifested in different ways. In DC EM, the current direction is unchanged, the cathode and anode locations stay the same, and void formation is seen near one end, the cathode. In contrast, for AC EM, the cathode and anode are exchanged whenever the current direction reverses. This can lead to void possibilities at either endpoint of the Cu DD wire.

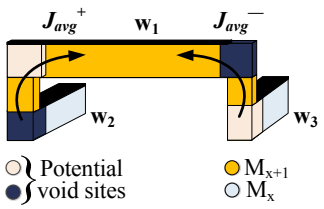


Figure 1: Potential void locations for AC EM. The arrows for J_{avg}^+ and J_{avg}^- denote the direction of electron flow.

Starting from Section II-A, we incorporate the possibilities of voids at either ends in our framework by calculating average current densities in the forward and reverse cycle separately.

Consider a Cu DD wire carrying a bidirectional current (Fig. 1). The arrows are in the directions of electron average current; conventional currents flow in opposite directions. In the forward cycle, due to the current density J_{avg}^+, electrons flow from left to right in wire $\mathbf{w_1}$ in metal layer M_{x+1}, leading to potential void sites at the left end of $\mathbf{w_1}$ and below the via in wire $\mathbf{w_3}$ on layer M_x. For $\mathbf{w_1}$, the effective current density at the left end of the wire, J_{EM^L} is given by:

$$J_{EM^L} = J_{avg}^+ - r \cdot J_{avg}^- \quad (4)$$

where r is the recovery factor [8]. In the reverse cycle, the current density J_{avg}^- may cause voids at the right end of $\mathbf{w_1}$ and under the via in $\mathbf{w_2}$. the effective current density at the right end of the wire, J_{EM^R}, is given by:

$$J_{EM^R} = J_{avg}^- - r \cdot J_{avg}^+ \quad (5)$$

Therefore, to extend the DC resistance evolution model to AC EM, we derive a model for AC-EM-based on current density calculations using Eq. (4) and Eq.(5). However, special attention should be made while calculating the probability distribution function (PDF) of resistance change to incorporate multiple void sites. For each potential void site, the PDF of the resistance change using Eq. (3) should be evaluated.

C. AC EM flux divergence

The effective current for AC EM in a wire is not necessarily given by J_{EM^L} and J_{EM^R} (Eq. (4) and Eq. (5)) for all wires. In circuits, when multiple segments are connected by a via, the void evolution at the vias depends on the direction and magnitude of current flow in neighboring wires [12]. For such vias in Cu DD interconnect stacks, the flux divergence comes into play because the Ta barrier layer at the via acts as a

barrier to the migration of metal atoms. Therefore, if a current flows through a via, any metal flux that approaches the via cannot go through the via, but instead, proceeds in the direction associated with flux divergence. In such cases, the effective current is calculated by accounting for the flux divergence.

The work in [12] incorporates the DC EM atomic flow in the wire as well as the divergence flow from neighboring wires. For AC EM, the flux divergence calculations are more involved as they must keep track of bidirectional currents and the recovery factor. We show here that the way to incorporate divergence into AC EM leads to relatively simple equations, although these have not been derived in the published literature.

We consider a generic multi-layer interconnect scenario shown in Fig. 2 in which the nets have multiple fanouts and are routed over adjacent multiple metal layers connected by vias 1 through 5. The current density in each direction through each wire is shown by the arrows, which point in the direction of electron flow. These current flows are in the directions of electron avg current; conventional currents flow in opposite directions. For each edge e_i in the figure, $J_{avg}^{blue}(e_i)$ is the average current density flowing from left to right in a horizontal wire, and bottom to top in a vertical wire; average currents in the opposite direction are denoted by $J_{avg}^{green}(e_i)$).

We consider one edge e_1 and compute its effective current density, incorporating flux divergence. Using the notation in the figure, for a candidate void location at the left end of edge e_1, at node 1, the effective flux (including divergence) away from the node is $J_{avg}^{blue}(e_1) + J_{avg}^{blue}(e_3)$. The effective sweep-back flux due to current in the opposite direction is $J_{avg}^{green}(e_1) + J_{avg}^{green}(e_3)$. Similarly, at the right end of edge e_1, at node 5, the effective flux away from the node is $J_{avg}^{green}(e_1)$ and $J_{avg}^{blue}(e_3)$, while the effective sweep-back flux is $J_{avg}^{blue}(e_1) + J_{avg}^{green}(e_3)$. Thus, the net effective flux, accounting for divergence as well as recovery, for voids at left and right end points of e_1, is given by:

$$
\begin{aligned}
J_{flux^L}(e_1) &= \{J_{avg}^{blue}(e_1) + J_{avg}^{blue}(e_3)\} - r \cdot \{J_{avg}^{green}(e_1) + J_{avg}^{green}(e_3)\} \\
&= \{J_{avg}^{blue}(e_1) - r \cdot J_{avg}^{green}(e_1)\} + \{J_{avg}^{blue}(e_3)\} - r \cdot J_{avg}^{green}(e_3)\} \\
&= J_{\mathrm{EM^L}}(e_1) + J_{\mathrm{EM^L}}(e_3) \\
J_{flux^R}(e_1) &= \{J_{avg}^{green}(e_1) + J_{avg}^{blue}(e_3)\} - r \cdot \{J_{avg}^{blue}(e_1) + J_{avg}^{green}(e_3)\} \\
&= \{J_{avg}^{green}(e_1) - r \cdot J_{avg}^{blue}(e_1)\} + \{J_{avg}^{blue}(e_3) - r \cdot J_{avg}^{green}(e_3)\} \\
&= J_{\mathrm{EM^R}}(e_1) + J_{\mathrm{EM^L}}(e_3)
\end{aligned}
$$

For edge (e_1), the effective current density expressions for a void at the left endpoint ($J_{flux^L}(e_1)$) and the right endpoint ($J_{flux^R}(e_1)$), mirror Eq. (4) and Eq. (5), but $J_{\mathrm{EM^L}}(e_3)$ is added to *both* terms here to allow for current divergence: this is a new result. The effective current densities for e_2, e_3 and e_4 can be calculated in a similar way.

We quantify the impact of current divergence by applying our simulation framework, which is described in Section III, to a 16nm multi-layer circuit shown in Fig. 3(a), observing the delay from X_1 to load 4. We perform two sets of circuit simulations. For the first set, we use the current density without incorporating flux divergence and for the second set, we use the current density incorporating the flux divergence. Fig. 3(b), shows the worst-case percentage delay shift for various circuit operation times, comparing it against a conventional approach

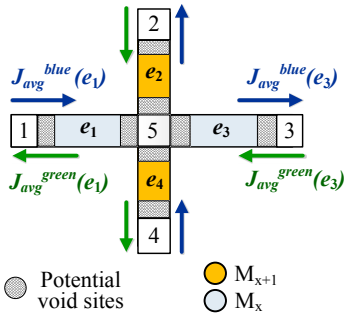
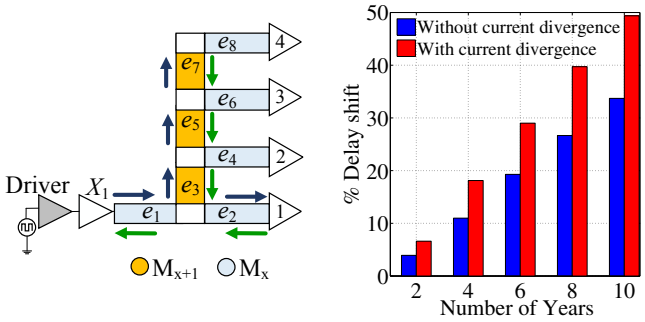


Figure 2: Current divergence calculation example.

that is ignorant of current divergence. The error from such an approach can be significant, e.g., at ten years, it is 16% of the nominal delay value. Thus, neglecting flux divergence underestimates the delay degradation because it does not account for flux blockages at boundary points.



(a) F04 test case (b) Delay comparison

Figure 3: Current divergence effect for a multi-layer F04 case.

III. Monte Carlo simulation framework

To observe the effect of EM on signal wires, we perform probabilistic EM analysis on a set of typical on-chip signal interconnects where the performance parameter of interest is the delay of a signal net or the skew of a clock network. Since our focus is on accuracy, we use HSPICE based simulations at various values of circuit operation time.

Our circuit simulations follow a Monte Carlo (MC) approach. We model the wire as a distributed RC line, with potential void locations near the vias that could cause resistance change. As described previously in Section II-A and Section II-B, we model the resistance change at the end-point segments near vias as a lognormal random variable.

For all the test cases, the first step is to perform a single HSPICE circuit simulation to extract the effective average current density (previously discussed in Section II-C) to be used for void resistance calculations and RMS current density to calculate temperature change due to Joule heating using Eq. (1) and Eq. (2). This nominal case represents the circuit state at time zero, with no EM damage. The EM average and RMS current density values are passed on to the probabilistic AC EM model, described in Section II, which predicts the resistance change distribution for each wire. Using a set of 5000 samples from the probability distribution of each wire's resistance change, we perform circuit simulation, and extract the statistics of EM-induced timing shifts over all samples.

Our simulations are performed at temperature $T = 105°$C and use a recovery factor $r = 0.7$ [8]. Other process parameters for the EM model are [6], [20]: $\sigma_c = 41$MPa, $Z^{\star}_{eff} = 1$, and $D_{eff} = 1.3 \times 10^{-9}$m^2/s, $E_a = 0.80 \pm 0.06eV$. The metal layer technology parameters are derived from 45nm FreePDK [21] and Joule heating parameters are taken from [11].

Our analysis spans multiple technology nodes starting from the 45nm technology node and projected up to the 7nm technology node. For circuit construction of the base case node: 45nm, the standard cells are taken from the NANGATE open standard cell library [22] based on the 45nm FreePDK [21]. For other technology nodes, the physical layout parameters of the standard cells are obtained by shrinking the transistor and wire features within the cell by the appropriate scaling factor [23], [24], S, which is taken to be $\frac{1}{0.7}$ for successive technologies. We assume that the same process technology is used for interconnects at all nodes and we use the Predictive Technology Model (PTM) [25]–[27] to incorporate process changes for devices (e.g., the use of FinFETs). For circuit performance analysis, we perform HSPICE circuit simulation using these PTM SPICE models. Our MC simulation framework is summarized in Algorithm 1.

Algorithm 1 HSPICE Monte Carlo simulation.

```
Run HSPICE to obtain J_fluxL, J_fluxR and J_rms for each wire.
for each wire do
    Use the resistance evolution model to obtain
    lognormal PDFs of wire resistance
end for
for each Monte Carlo iteration do
    for each wire do
        Sample the wire resistance values
    end for
    Build a circuit sample for the netlist using the
    above set of wire resistances
    Perform HSPICE simulation for this netlist
    Tabulate the value of the performance
    parameter (delay/skew) for the sample
end for
Report statistics (mean, standard deviation, etc.)
```

IV. Results

We use our MC simulation method described in Section III, to observe the EM degradation in the circuit performance at various values of circuit operation time for advanced technology nodes. We discuss the impact of EM on two circuits: a buffered wire and an H-tree (Fig. 4 and Fig. 8).

A. MC simulation: Buffered wire

A buffered wire topology is commonly observed in buses, clock networks and in general logic for carrying signals across blocks. We construct this circuit by stitching together multiple instances of 32× size inverter cell, INV_X32, using Cu DD wires routed in one metal layer, as shown in Fig. 4. The total wire length L is 2000μm for the base case of a 45nm technology. The cell and the wire dimensions are chosen to construct a balanced design of an RC-loaded wire, such that neither the cell delay nor the net delay solely dominates the total delay of the buffered wire. We assume a worst-case switching scenario corresponding to an always-switching buffered wire in a clock-network. For signals that are not always active, the circuit switching will be a fraction of the clock frequency. This implies that both the average and RMS effective current densities will be smaller than the always-switching case, resulting in slower resistance evolution. For advanced nodes, the standard cell and the wire geometry are scaled by a scaling factor, S, as described in Section III. The total wire length of a buffered wire also scales between successive technology nodes, as shown in Fig. 4, since the circuitry shrinks. The number of repeaters remains roughly constant over all technology nodes.

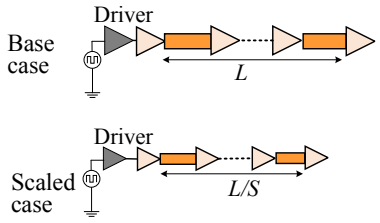


Figure 4: Schematic of the buffered wire for the base case 45nm technology node and the successive 32nm technology node.

We apply the framework described in Section III to perform MC simulation on the buffered wire. We observe the EM-induced delay degradation from the input pin of the first repeater to the input pin of the last repeater. Since our EM analysis is probabilistic, the delay degradation due to EM is also observed to be probabilistic. Given two identical parts with identical process variations, facing identical stimuli and environments in the field, it is impossible to predict which part will age faster in the field. Thus, margins for EM-related delay shifts must correspond to worst-case aging: in this paper, we take this to be the 99.97 percentile point.

We compare this worst-case EM-induced delay degradation against the delay degradation caused by other circuit aging mechanisms: Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI). The BTI and HCI mechanisms result in an increase in the standard cell delay while EM results in an increase in the wire delay. For calculating the delay degradation due to BTI and HCI in the INV_X32 repeater cells we use an aging model based on [28] and [29], respectively.

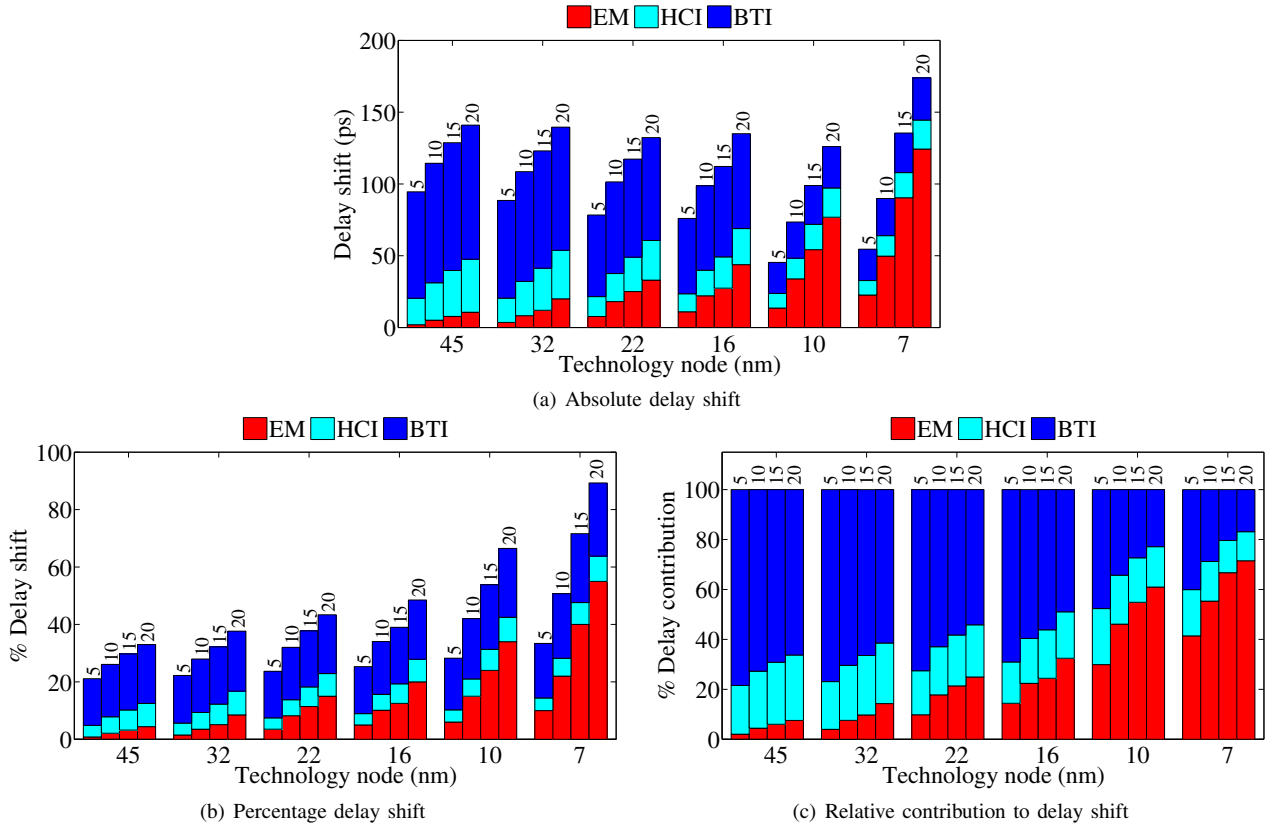
Fig. 5(a) shows the absolute delay shift caused by the various aging mechanisms for the buffered wire. The plots indicate the magnitude of the delay shift values at various values of circuit operation time, $t_o = 5$, 10, 15, and 20 years, for advanced technology nodes ranging from 45nm to 7nm. The percentage delay shift relative to the nominal delay value at the beginning of circuit operation is shown in Fig. 5(b) and the relative contribution of each aging mechanism, normalized by the total delay shift, is shown in Fig. 5(c).

Fig. 5(a) indicates that for a given technology node, the contribution due to each aging mechanism increases with circuit operation time because of the increased impact with time on both transistor and wire degradation. We observe that, for a fixed circuit operation time, as technology advances, the absolute BTI- and HCI-induced delay shift monotonically decreases while the absolute EM-induced delay shift monotonically increases. Notice that although the absolute BTI- and HCI-induced delay shift decreases with technology, but the percentage degradation, as shown in Fig. 5(b), is roughly constant. This is consistent with technology scaling trends for ring oscillators frequency degradation in [30]–[32].

Fig. 5(c) indicates that BTI is the dominant mechanism during early circuit operation. For large values of circuit operation time, the delay contribution due to EM increases sharply, especially for more deeply scaled technologies. The amplified EM contribution is due to the increase in the wire current density as wire geometries shrink, thereby increasing the EM driving force and accelerating resistance change due to void formation and subsequent growth for advanced technology nodes and large circuit operation time. For the data point corresponding to the 7nm technology at 10 years, in Fig. 5(c), our simulations show that EM can contribute as much as 55% of the total delay shift due to all the mechanisms. Such large degradation can cause serious problems for high stress, always-on parts, e.g., in server (computing) applications.

There are two key issues that must be kept in mind while interpreting this data. First, as stated in Section III, our analysis assumes that the same process is used for Cu DD interconnects at all technology nodes, and only geometrical scaling is applied for interconnects between technology nodes. However, the interconnect process may transform as technology advances. On the one hand, process improvements such as use of doping with alloyed seed layers in the Cu DD process, or replacing the SiN capping layer by CoWP are projected to alleviate the large impact of EM to some extent for deeply scaled technologies [1], on the other hand, advanced process scaling issues may negate these improvements, for instance, as Cu wire dimension shrinks, the Cu microstructure becomes more polygranular and the wire resistivity increases due to the combined effect of shrinking in dimensions and changes in Cu microstructure [33], [34]. This increased resistivity contributes to increased EM effects as wire delays will be increasingly interconnect-dominated in future technologies and shifts in wire resistance translate to more significant shifts in the overall delay. Second, the analysis assumes that the signal wires switch on every clock transition. This assumption may be true for some global wires but is less likely to be valid for more local wires. For wires that switch less frequently, the average and RMS currents are lower, implying that the delay shift will be lower. Correspondingly, HCI effects are reduced due to lower switching, but the BTI contribution remains unchanged. Therefore, for wires that switch less frequently, the relative contribution of BTI towards delay shift will be larger and that of HCI and EM will be reduced.

Next, we observe the variation in the delay degradation focusing solely on the EM-induced delay shift, for advanced technology nodes from 45nm to 7nm, at various values of circuit operation time. Fig. 6(a), (b), (c), and (d) show the percentage delay shift for the buffered wire at various values of circuit operation time, $t_o = 5$, 10, 15, and 20 years. Each bar in these figures shows the mean delay shift as a percentage of nominal delay, along with the 0.03 and 99.97 %ile points. For both the mean as well as the spread of the delay shift, in all cases, we observe that the rate of EM degradation with respect to time increases as technology scales from 45nm to 7nm node. For a fixed circuit operation time, the increase in the delay shift with technology is primarily attributed to the increase in the

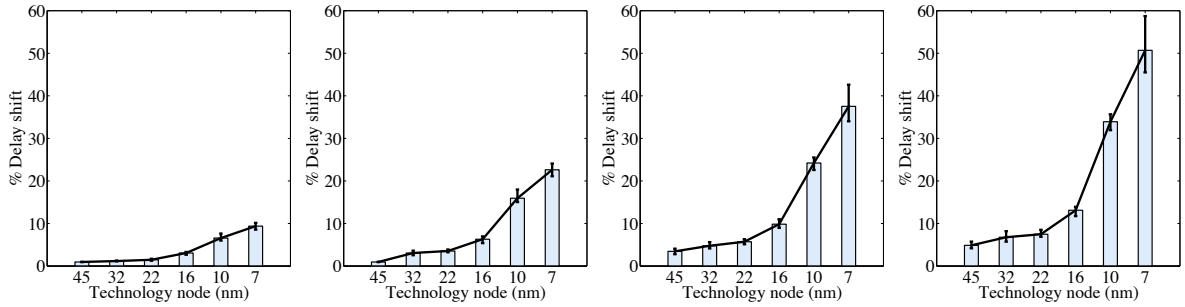


(a) Absolute delay shift

(b) Percentage delay shift

(c) Relative contribution to delay shift

Figure 5: Buffered wire: (a) Absolute delay shift due to various aging mechanisms for advanced technology nodes at various values of circuit operation time. (b) Percentage delay shift, relative to the nominal value. (c) Relative delay contribution normalized by the total delay shift.



(a) $t_o = 5$ years (b) $t_o = 10$ years (c) $t_o = 15$ years (d) $t_o = 20$ years

Figure 6: Buffered wire: EM-induced delay shift variation for advanced technology nodes at various values of circuit operation time, t_o.

current density in the wires, exacerbating EM damage. For a fixed technology node, the delay shift is magnified for a higher circuit operation time, since the EM voids grow to larger sizes as circuit operation time increases and more voids keep being formed. In particular, for the 10-year plot in Fig. 6(b), which corresponds to the lifetime of server computing applications, we observe that the worst-case percentage shift value increases from 1% to 22% from the 45nm to the 7nm nodes.

B. MC simulation: H-tree clock backbone

Next, we consider the impact of EM on a clock distribution network, focusing on a single-level H-tree clock backbone. Such top-level clock networks are particularly susceptible to EM since they almost always switch and are seldom gated. We study the EM-induced skew, i.e., the maximum difference in clock latencies between any two end points of the tree as result of EM. Ideally, its value should be low, since a larger skew translates into the need for a larger timing margin.

We observe the effect of EM on skew for the H-tree structure shown in Fig. 8. We build the H-tree for the base case of the 45nm technology node using the Cadence Virtuoso layout editor. The H-tree dimensions, shown in Fig. 8, are similar to a global clock-tree for a typical mobile processor core. The chip size is 1600μm$\times 1000\mu$m and the metal layers used are metal 6 and metal 7. The H-tree is driven by a buffer cell BUF_X32 and the intermediate wires are buffered using multiple buffer cells. The endpoints are connected to multiple sized fanout-4 (F04) loads constructed using inverter cells, INV_X32 and INV_X16. For the 45nm node, the H-tree is simulated with a clock frequency of 1.6GHz.

The circuit netlist, extracted from the H-tree layout, is scaled for advanced technology nodes from the 45nm technology node to the 7nm technology node using the methodology discussed in Section III. The H-tree wire lengths are kept constant, since the chip area is constant even as

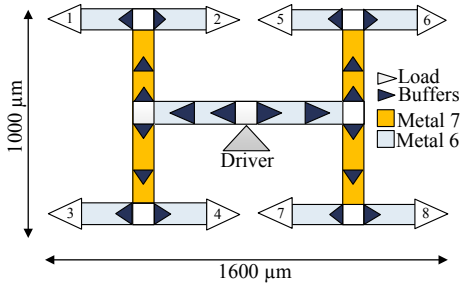


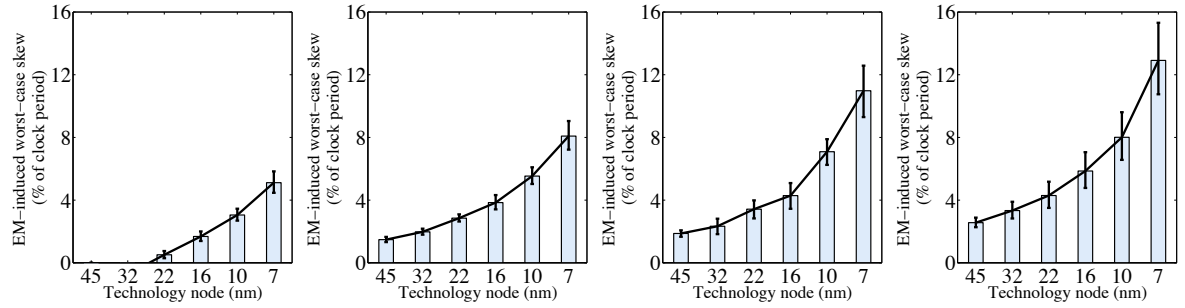
Figure 8: An H-tree clock backbone layout.

technology shrinks. For scaled technologies, additional buffers are inserted in between metal wires to counterbalance the increase in the wire delay with shrinking dimensions and ensure correct functioning of the circuit.

For the 45nm H-tree structure, the nominal skew for the test-case with no EM degradation is observed to be 10ps, i.e., 1.6% of the clock period. This nominal value of skew is entirely due to design and does not include process, temperature and voltage (PVT) variations, which can contribute as much as 10% as seen from previously implemented designs [35, Chapter 43].

We use the framework described in Section III to calculate the EM-induced resistance change for all wires and corresponding skew degradation. The H-tree structure is composed of multi-layer interconnects connected by vias. For such interconnects, the current density for EM is calculated taking into account the flux divergence, using the methodology described in Section II-C.

For each MC iteration, we tabulate the EM-induced worst-skew, defined as the maximum value of skew between any two endpoints due to EM. We perform simulations for advanced technology nodes at various values of circuit



(a) $t_o = 5$ years (b) $t_o = 10$ years (c) $t_o = 15$ years (d) $t_o = 20$ years

Figure 7: H-tree: The impact of EM on the worst-case skew for advanced technology nodes at various values of circuit operation time, t_o.

operation time, $t_o = 5$, 10, 15, and 20 years. Fig. 7(a), (b), (c), and (d) show the EM-induced worst-case skew as a fraction of clock period for advanced technology nodes at various circuit operation time values. For each of the plots, the bars show the mean value for worst-case skew as a percentage of the clock period along with the 0.03 and 99.97 %ile points.

For each technology node, the worst-case skew deteriorates with increased operation time, since more voids nucleate and voids that are already formed grow to larger sizes. For the 45nm node, the EM-induced worst-case skew after 10 years is 9ps, which is 1.4% of the clock period. However, this changes at 7nm, where the skew is no longer negligible. After 10 years, the worst-case skew increases to 8.2% of the clock period, which is about 6× of the 45nm value, and comparable to the magnitude of skew due to PVT variation mentioned previously.

V. Conclusion

Unlike prior work on signal wires that treats EM as catastrophic failure, this work analyzes and quantifies the performance degradation on circuits as a result of EM. Using a set of on-chip structures, we have demonstrated that EM-induced delay shift is circuit dependent. Our projections to future technologies show significant EM degradation comparable to major transistor aging mechanisms.

References

[1] "International Technology Roadmap for Semiconductors," online chapter available at http://www.itrs.net/Links/2013ITRS/2013Chapters/2013Interconnect.pdf

[2] J. R. Black, "Electromigration failure modes in aluminum metallization for semiconductor devices," *Proceedings of the IEEE*, vol. 57, no. 9, pp. 1587–1594, 1969.

[3] V. Mishra and S. S. Sapatnekar, "The impact of electromigration in copper interconnects on power grid integrity," in *Proceedings of the ACM/IEEE Design Automation Conference*, 2012, pp. 88:1–88:6.

[4] X. Huang, T. Yu, V. Sukharev, and S. X.-D. Tan, "Physics-based electromigration assessment for power grid networks," in *Proceedings of the ACM/IEEE Design Automation Conference*, 2014, pp. 80:1–80:6.

[5] M. A. Korhonen, P. Borgesen, K. N. Tu, and C. Y. Li, "Stress evolution due to electromigration in confined metal lines," *Journal of Applied Physics*, vol. 73, no. 8, pp. 3790–3799, 1993.

[6] S. P. Hau-Riege, "Probabilistic immortality of Cu damascene interconnects," *Journal of Applied Physics*, vol. 91, no. 4, pp. 2014–2022, 2002.

[7] R. L. de Orio, H. Ceric, and S. Selberherr, "A compact model for early electromigration failures of copper dual-damascene interconnects," *Microelectronics Reliability*, vol. 51, no. 9–11, pp. 1573–1577, 2011.

[8] K. D. Lee, "Electromigration recovery and short lead effect under bipolar- and unipolar-pulse current," in *Proceedings of the IEEE International Reliability Physics Symposium*, 2012, pp. 6B.3.1–6B.3.4.

[9] M. K. Lim *et al.*, "Effects of pulsed current on electromigration lifetime," in *Proceedings of the International Symposium on the Physical and Failure Analysis of Integrated Circuits*, 2008, pp. 1–6.

[10] L. Doyen, L. Arnaud, X. Federspiel, P. Waltz, and Y. Wouters, "Use of bidirectional current stress for in depth analysis of electromigration mechanism," in *Proceedings of the IEEE International Reliability Physics Symposium*, April 2008, pp. 681–682.

[11] K. Banerjee and A. Mehrotra, "Global (interconnect) warming," *IEEE Circuits and Devices Magazine*, vol. 17, no. 5, pp. 16–32, 2001.

[12] Y. J. Park, P. Jain, and S. Krishnan, "New electromigration validation: Via node vector method," in *Proceedings of the IEEE International Reliability Physics Symposium*, 2010, pp. 698–704.

[13] M. Hauschildt *et al.*, "Statistical analysis of electromigration lifetimes and void evolution," *Journal of Applied Physics*, vol. 101, no. 4, pp. 682–687, 2007.

[14] J. R. Lloyd and J. Kitchin, "The electromigration failure distribution: The fineline case," *Journal of Applied Physics*, vol. 69, no. 4, pp. 2117–2127, 1991.

[15] Z.-S. Choi, R. Mönig, and C. V. Thompson, "Dependence of the electromigration flux on the crystallographic orientations of different grains in polycrystalline copper interconnects," *Applied Physics Letters*, vol. 90, no. 24, p. 24193, 2007.

[16] V. M. Dwyer, "Modeling the electromigration failure time distribution in short copper interconnects," *Journal of Applied Physics*, vol. 104, no. 5, pp. 053 708–1–053 708–6, 2008.

[17] A. A. Abu-Dayya and N. C. Beaulieu, "Comparison of methods of computing correlated lognormal sum distributions and outages for digital wireless applications," in *Proceedings of the IEEE Vehicular Technology Conference*, 1994, pp. 175–179.

[18] J. Tao, N. Cheung, and C. Hu, "An electromigration failure model for interconnects under pulsed and bidirectional current stressing," *IEEE Transactions on Electron Devices*, vol. 41, no. 4, pp. 539–545, 1994.

[19] W. R. Hunter, "Self-consistent solutions for allowed interconnect current density – Part II: Application to design guidelines," *IEEE Transactions on Electron Devices*, vol. 44, no. 2, pp. 310–316, 1997.

[20] S. Alam, C. L. Gan, F. L. Wei, C. V. Thompson, and D. Troxel, "Circuit-level reliability requirements for Cu metallization," *IEEE Transactions on Devices and Materials Reliability*, vol. 5, no. 3, pp. 522–531, 2005.

[21] J. E. Stine *et al.*, "FreePDK: An open-source variation-aware design kit," in *IEEE International Conference on Microelectronic Systems Education*, 2007, pp. 173–174.

[22] "Nangate open cell library," available at http://www.nangate.com

[23] M. T. Bohr and Y. A. El-Mansy, "Technology for advanced high-performance microprocessors," *IEEE Transactions on Electron Devices*, vol. 45, no. 3, pp. 620–625, 1998.

[24] H. Iwai, "Roadmap for 22nm and beyond (Invited Paper)," *Microelectronic Engineering*, vol. 86, no. 7–9, pp. 1520–1528, 2009.

[25] "Predictive Technology Model," available at http://www.ptm.asu.edu

[26] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45nm design exploration," in *Proceedings of the IEEE International Symposium on Quality Electronic Design*, March 2006, pp. 6–590.

[27] S. Sinha, G. Yeric, V. Chandra, B. Cline, and Y. Cao, "Exploring sub-20nm FinFET design with predictive technology models," in *Proceedings of the ACM/IEEE Design Automation Conference*, 2012, pp. 283–288.

[28] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "Adaptive techniques for overcoming performance degradation due to aging in digital circuits," in *Proceedings of the Asia-South Pacific Design Automation Conference*, 2009, pp. 284–289.

[29] T. Nigam, "Impact of transistor level degradation on product reliability," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, 2009, pp. 431–438.

[30] V. Huard, F. Cacho, and X. Federspiel, "Technology scaling and reliability challenges in the multicore era," in *Proceedings of the IEEE International Reliability Physics Symposium*, April 2013, pp. 3A.5.1–3A.5.7.

[31] S. Mahapatra *et al.*, "Universality of NBTI - From devices to circuits and products," in *Proceedings of the IEEE International Reliability Physics Symposium*, June 2014, pp. 3B.1.1–3B.1.8.

[32] A. Rahman *et al.*, "Reliability studies of a 22nm SoC platform technology featuring 3-D tri-gate, optimized for ultra low power, high performance and high density application," in *Proceedings of the IEEE International Reliability Physics Symposium*, April 2013, pp. PI.2.1–PI.2.6.

[33] B. Li, C. Christiansen, D. Badami, and C.-C. Yang, "Electromigration challenges for advanced on-chip Cu interconnects," *Microelectronics Reliability*, vol. 54, no. 4, pp. 712–724, 2014.

[34] C. Pan and A. Naeemi, "A proposal for a novel hybrid interconnect technology for the end of roadmap," *IEEE Electron Device Letters*, vol. 35, no. 2, pp. 250–252, 2014.

[35] C. J. Alpert, D. P. Mehta, and S. S. Sapatnekar, *Handbook of algorithms for physical design automation*. CRC Press, 2008.