Leakage Modeling for Devices with Steep Sub-threshold Slope Considering Random Threshold Variations

Ayan Paul, Chaitanya Kshirsagar, Sachin S. Sapatnekar, Steven Koester and Chris H. Kim
Electrical and Computer Engineering
University of Minnesota,
Minneapolis, MN 55455, USA
Contact E-mail: paul0661@umn.edu

***Abstract*- In this paper we propose a generic approach to statistically model leakage variation of devices with steep sub-threshold slope caused by random threshold variations. Monte Carlo simulation results based on our model show less than 11% error in 6σ leakage current estimation compared to 65% error using conventional square root method. A design example based on SRAM bitline leakage issue is also presented to show the correctness of our model in a realistic circuit scenario. This general-purpose modeling technique could be a useful tool in estimating leakage in a variety emerging device technology.**

Keywords- sub-threshold slope; leakage current; Monte Carlo simulation; statistical analysis; SRAM

I. INTRODUCTION

For the last several decades, the semiconductor industry has relied upon semiconductor device scaling as the basis for advancements in integrated circuit technology. However, future scaling of complementary metal oxide semiconductor (CMOS) technology is uncertain due to limits on the power density that can be dissipated in conventional systems. The most effective way to reduce power consumption in logic circuits is to reduce the supply voltage (V_{dd}) since both static and dynamic power consumption depend strongly on V_{dd}. However, the ability to scale V_{dd} in metal oxide semiconductor field effect transistor (MOSFET) is limited by the fact that the sub-threshold slope (SS) must be greater than $2.3k_BT/q$ (60 mV/decade) at room temperature, where k_B is Boltzmann constant, T is the temperature in absolute scale, and q is electronic charge. This requirement, which arises from the thermionic nature of the sub-threshold conduction mechanism in MOSFETs, leads to a fundamental power/performance trade-off. As V_{dd} is reduced, the leakage power must be allowed to increase in order to maintain constant performance, or the speed must be sacrificed in order to control the leakage power. A detailed analysis of these trade-offs has been performed in [1], and it has been shown that practical supply voltage scaling is limited to ~0.5 V for conventional CMOS circuits.

The above power/performance trade-off could be overcome if SS values significantly lower than 60mV/decade could be achieved. A steeper SS would allow the threshold voltage (V_T) to be reduced while meeting the same off current. If, at the same time, the on current could be maintained, then the supply voltage could be reduced without sacrificing performance. Many device types have been proposed that could produce steep SS values, including homojunction and heterojunction based tunneling field effect transistors (TFETs) [2,3,4,5], nanoelectromechanical devices [6], ferroelectric-gate FETs [7], and impact ionization MOSFETs [8]. Several recent papers have reported experimental observation of SS values in TFET as low as 40 mV/decade at room temperature [9-10]. Although from leakage standpoint steep SS is favorable, smaller SS, on the other hand, makes a device more susceptible to statistical variations. TFET, NEMS device, ferroelectric-gate FET show a wider leakage distribution than MOSFET because of the relatively steeper SS of these devices compared to a MOSFET.

In the next section, we discuss V_T induced leakage and ON current variation of TFET, which can be extended to any generic steep sub-threshold device. In section III, we discuss why conventional square-root approach for leakage modeling is not very useful for devices with steep SS. This motivates us to look for a better modeling technique for steep SS devices. In section IV, we propose width dependent statistical leakage modeling technique based on Wilkinson's approach [11], which technique can be used to model leakage of steep SS devices. Section V presents experimental results to verify goodness of the model compared to the square-root approach in modeling the leakage distribution. Finally, in section VI, we provide a leakage sensitive design example to show the usefulness of our model, which is followed by the conclusion in section VII.

II. V_T INDUCED LEAKAGE AND ON CURRENT DISTRIBUTION AS A FUNCTION OF SUB-THRESHOLD SLOPE

In this section, we first show the effect of V_T variation on leakage as well as ON current as a function of SS for TFET devices. An n-channel TFET (n-TFET) differs from an

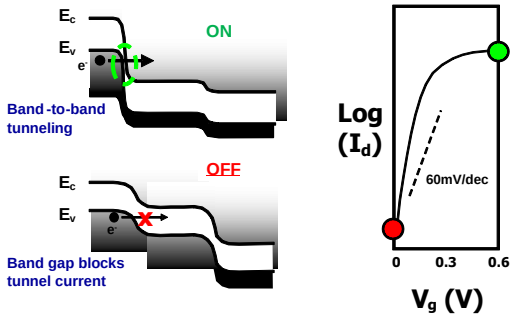


Fig. 1. (a) Band-diagram of TFET in ON and OFF state. (b) I_d-V_g characteristic of a TFET [12].

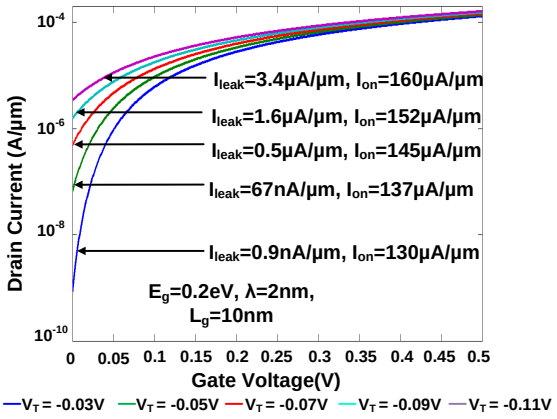
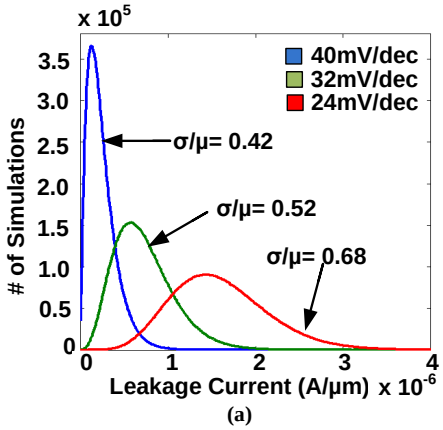


Fig. 2. I_d-V_g characteristics of the modeled TFET for different V_T values.

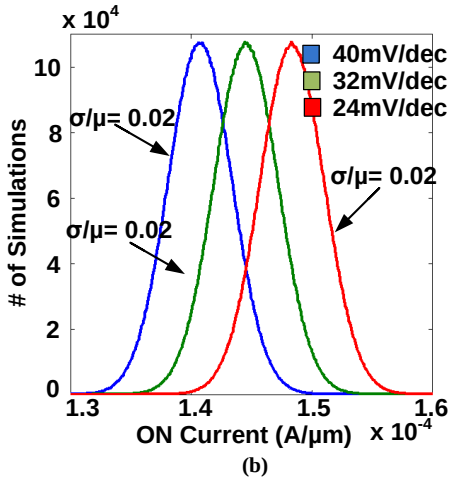
n-MOSFET in that the TFET utilizes a p-i-n source-channel-drain configuration. The operational principle is shown in Fig. 1(a). In the on-state, a positive voltage on the gate lowers the conduction band edge in the channel, allowing current to flow via band-to-band tunneling between the source and the channel. In the off-state, the current flow is blocked due to increase in the channel conduction band edge energy. This turn-off mechanism inherently allows SS to be less than 60 mV/decade (Fig. 1(b)), because the Fermi-Dirac distribution function in the source is filtered by the band gap [13]. Although drain current (I_d)-gate voltage (V_g) relation of a TFET has been studied and modeled in [14] and [15], no closed form analytical I_d-V_g relation has been reported so far. However, an empirical relation based on the measured data describes I_d versus V_g for on and off region of the characteristic by the same equation given by:

$$I_d = W \cdot A \cdot E_s \cdot e^{-B/E_s} \qquad (1)$$

where A and B are material dependent parameters, W is the width of the device, and E_s is defined as $(V_g\text{-}V_T)/\lambda$ [10]. λ is the effective tunneling distance of the device and V_T is the value of the gate voltage required to make the potential difference between the source and the channel zero. One important thing to note here is that SS of a TFET is a function of V_g unlike a MOSFET. Fig. 2 plots typical I_d-V_g characteristics of a TFET with A = 0.00084 S-nm, band gap (E_g) = 0.2 eV, λ = 2 nm and for a range of V_T values varying from -0.03V to -0.11V.



(a)



(b)

Fig. 3. (a) Leakage current and (b) ON current distributions of TFET as a function of SS.

We have performed Monte-Carlo analysis of leakage and ON current for TFETs with SS (at V_g= 0V) of 24mV/decade, 32mV/decade, and 40mV/decade. We have assumed V_T to follow normal distribution with $\sigma_{V_T}/\mu_{V_T} = 0.1$, where σ_{V_T} and μ_{V_T} are the standard deviation and mean of V_T distribution, respectively. Leakage distributions and ON current distributions are shown in Fig. 3 (a) and (b), respectively. As seen from the Fig. 3 (a), the ratio of standard deviation and mean (σ/μ) of leakage currents change by more than 60% as SS of the device changes from 24mV/decade to 40mV/decade. However, Fig. 3 (b) shows that σ/μ values of ON currents remain essentially constant over the same range of variation of SS. This observation leads us to the conclusion that in TFETs, leakage current is a very strong function of the SS, although ON current remains practically unaffected by SS. This conclusion, which will hold true in case of a generic device with steep sub-threshold region and CMOS-like ON behavior, has motivated us to study and model leakage variation of generic steep SS devices.

III. SQUARE-ROOT METHOD FOR V_T INDUCED LEAKAGE DISTRIBUTION MODELING AND ITS SHORTCOMINGS

Here we assume CMOS like ON and OFF behavior of a generic steep SS device with an underlying assumption that SS can go below 60mv/decade. Although device specific leakage modeling techniques might be necessary in order to obtain more accurate results, this generic approach can model leakage distribution of any devices with CMOS-like OFF behavior very accurately. Even though the device under consideration does not show exponential I_d-V_g relation in the sub-threshold regime similar to case of a TFET described in the previous section, we believe, to a first order approximation, the slope of $\log(I_d)$ vs. V_g curve can be assumed to be constant over a small range of variation of V_T, and our modeling approach should still be applicable. Let us

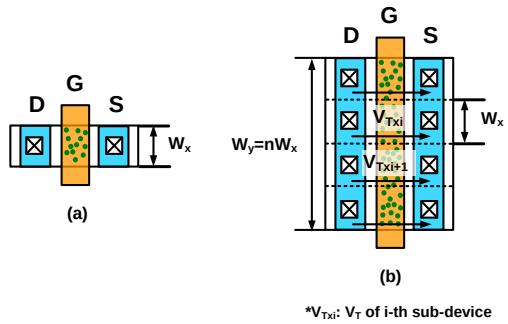


Fig. 4. (a) Reference device, and (b) Device to be modeled for leakage [16].

assume that for small V_T variation, I_d-V_g relation in the sub-threshold region can be written as $I_d = W \cdot K_1 \cdot e^{K_2 \cdot (V_g - V_T)}$, where K_1 and K_2 are curve-fitting parameters and W is the width of the device under consideration.

We can estimate the leakage distribution of a device having an arbitrary width from the known leakage distribution of a reference device using conventional square-root approach. Leakage current of a reference device of width W_x can be given by $W_X \cdot K_1 \cdot e^{-K_2 \cdot V_{TX}}$. We assume threshold voltage (V_{TX}) of the reference device to follow a normal distribution with mean $\mu_{V_{TX}}$ and standard deviation $\sigma_{V_{TX}}$. An arbitrary device of width W_y, which is n-times wider than the reference device and has the same SS, can be thought to be made up of n slices of the reference devices connected in parallel, as shown in Fig. 4. If we ignore the fringing effects at the device boundaries, the actual leakage distribution of this arbitrarily wide device can be given by $I_{leak} = \sum_{i=1}^{n} W_X \cdot K_1 \cdot e^{-K_2 \cdot V_{TX}}$, where we assume that mean and standard deviation of V_T for each of these slices are same as the mean and the standard deviation of V_T of the reference device, respectively. We refer this actual scenario as the golden scenario. Now our goal is to find out the mean and standard deviation of threshold voltage (V_{Ty}) of the device of width W_y as a function of the mean and standard deviation of V_{TX} so that the model matches the actual golden case leakage distribution closely.

According to the conventional square root leakage estimation approach, a steep SS device with the same SS as the reference device and width W_y will have $\mu_{V_{Ty}} = \mu_{V_{TX}}$ and $\sigma_{V_{Ty}} = \sigma_{V_{TX}} / \sqrt{\frac{W_y \cdot L_y}{W_X \cdot L_X}}$, where L_y and L_x are the lengths of the devices of width W_y and W_X, respectively.

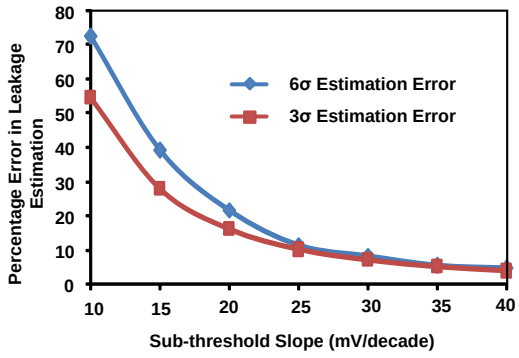


Fig. 5. Percentage leakage estimation error using square-root method vs. sub-threshold slope.

In Fig. 5, we have presented the result of the Monte Carlo simulations performed in order to compare the golden approach with the conventional square root method. From the figure, it is evident that the steeper the SS is, the larger the 6σ and 3σ leakage estimation errors of the square-root method are. This led us to the conclusion that a modeling technique better than the square-root method is necessary in order to model leakage distribution of devices with steep SS. In the following section we have presented a method based on Wilkinson's approach of moment matching for more accurate leakage estimation of steep SS devices.

IV. MODELING OF STATISTICAL LEAKAGE DISTRIBUTION OF STEEP SUB-THRESHOLD SLOPE DEVICES

Conventional square-root method does not take into account the shift in mean value of V_T with the increase in device width. Note that the mean value of V_T for the device under estimation is reduced because the overall leakage is dominated by that of a sub-device with a low V_T.

We propose to use Wilkinson's approach in estimating steep SS device's leakage current [11]. This approach has been previously used for statistical leakage estimation of MOSFETs and FinFETs and can be successfully applied in case of any devices with CMOS like OFF behavior, too [16-17]. In this approach, the sum of log-normal distributions of a number of random variables can be expressed as a single log-normal distribution, where the random variable follows Gaussian distribution of calculable mean and standard deviation [11]. Wilkinson's approach is explained briefly in the next paragraph.

Let us assume (m_{X_i}, σ_{X_i}) and (m_y, σ_y) are the mean and standard deviation of the original Gaussian random variables X_i and the new Gaussian variable y of the lognormal functions, respectively. We define $S = \sum_{i=1}^{n} \frac{1}{n} e^{X_i}$, and denote r_{ij} as the correlation coefficient between the random variables. By equating the first two moments of the original lognormal equation and the new lognormal equation, we get:

$$u_1 = E(S) = \sum_{i=1}^{n} \frac{1}{n} e^{m_{X_i} + \frac{\sigma_{X_i}^2}{2}} = e^{m_y + \frac{\sigma_y^2}{2}}$$

$$u_2 = E(S^2) = \frac{1}{n^2} \left(\sum_{i=1}^{n} e^{2m_{X_i} + 2\sigma_{X_i}^2} + 2 \sum_{i=1}^{n-1} \sum_{j=i+1}^{n} e^{m_{X_i} + m_{X_j}} e^{\frac{\sigma_{X_i}^2 + \sigma_{X_j}^2 + 2r_{ij}\sigma_{X_i}\sigma_{X_j}}{2}} \right)$$

$$= e^{2m_y + 2\sigma_y^2}$$

Solving for m_y and σ_y and assuming r_{ij} is same between any pair of random variables and denoting it by r, we get

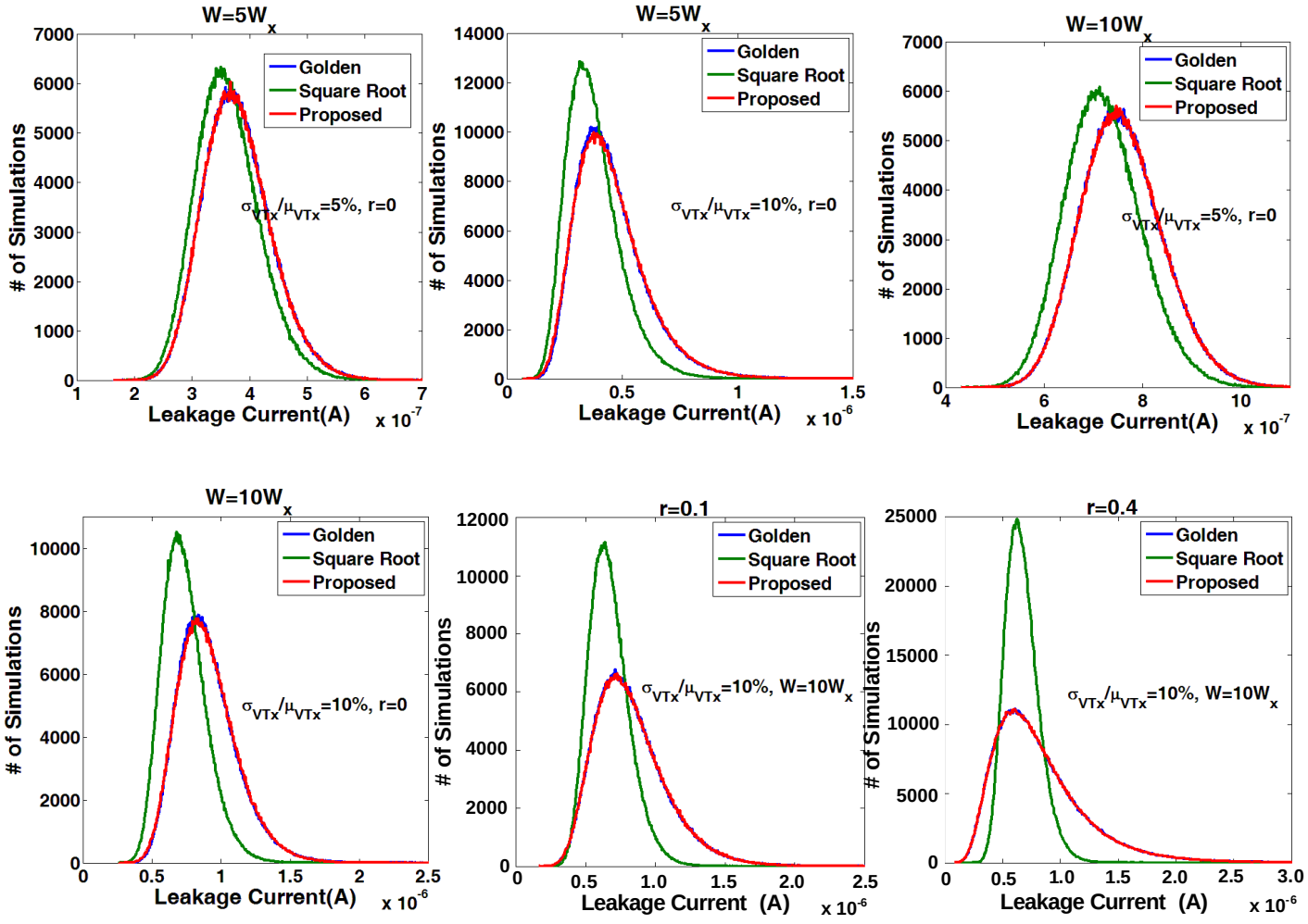


Fig. 6. Monte Carlo simulation results for leakage estimation results for golden, square root, and proposed methods for various device width, V_T distribution and correlation co-efficient.

$$m_y = m_X + \frac{1}{2}\Delta$$
$$\sigma_y^2 = \sigma_X^2 - \Delta$$

where $\Delta = \sigma_X^2 - \ln(\frac{e^{\sigma_X^2}+(n-1)\cdot e^{r\cdot\sigma_X^2}}{n})$.

From this expression for m_y and σ_y, we can write the mean and standard deviation of V_{Ty} from the previous section as:

$$\mu_{V_{Ty}} = \mu_{V_{TX}} - \frac{1}{2}\Delta/K_2$$
$$\sigma_{V_{Ty}}^2 = \sigma_{V_{TX}}^2 - \Delta/K_2^2 \quad (\Delta \geq 0) \qquad (2)$$

where $\Delta = K_2^2\sigma_{V_{TX}}^2 - \ln\left(\frac{e^{K_2^2\sigma_{V_{TX}}^2}+(n-1)\cdot e^{r\cdot K_2^2\sigma_{V_{TX}}^2}}{n}\right) \geq 0$.

Thus this model gives us width dependent mean and sigma value of V_T in terms of the mean and sigma of V_T of the reference device. $\mu_{V_{Ty}}$ and $\sigma_{V_{Ty}}$ found in this way are used for statistical leakage estimation in the sections to follow.

V. SIMULATION RESULTS COMPARING GOLDEN, SQUARE-ROOT AND PROPOSED METHOD

In this section we present the result of the Monte Carlo simulations performed in order to compare the proposed method with the conventional square root method. We assumed that the mean and standard deviation of V_T of the reference device were given, and wider device was made up of a number of reference devices. We then found out the mean and standard deviation of V_T of the wider device from (2) using our proposed model, and the conventional square root model. Using those mean and standard deviations we then performed Monte Carlo analysis for square root method and our proposed method. We found out golden leakage distribution, which depicts the actual leakage distribution of the wider device, by performing Monte Carlo simulation using actual mean and standard deviation values.

In Fig. 6, we have plotted the Monte Carlo leakage distribution for different $\sigma_{V_{TX}}/\mu_{V_{TX}}$ ratios, different widths and different correlation coefficients. In each of these plots, leakage distribution for golden, square root and proposed scheme were overlaid for comparison purpose. In all the cases, our proposed scheme showed a much closer match

with the golden results while the conventional square root method was found to exhibit large discrepancies. As one can expect, we found larger leakage estimation errors with larger $\sigma_{V_{TX}}/\mu_{V_{TX}}$ ratio. If device slices are spatially correlated, error in leakage estimation using square root method becomes worst, as this model does not take correlation into account. However, our proposed scheme continues to estimate leakage distribution accurately. Table 1 compares leakage estimation errors under various scenarios.

Table 1. Comparison of square-root and proposed leakage estimation techniques.

$W=5W_X$, $\sigma_{V_{Tx}}/\mu_{V_{Tx}}=5\%$, r=0		
	Square Root	**Proposed**
3σ error in leakage	5.36%	0.09%
6σ error in leakage	6.50%	1.66%
$W=5W_X$, $\sigma_{V_{Tx}}/\mu_{V_{Tx}}=10\%$, r=0		
	Square Root	**Proposed**
3σ error in leakage	22.21%	0.99%
6σ error in leakage	31.52%	10.91%
$W=10W_X$, $\sigma_{V_{Tx}}/\mu_{V_{Tx}}=5\%$, r=0		
	Square Root	**Proposed**
3σ error in leakage	5.68%	0.09%
6σ error in leakage	6.84%	0.72%
$W=10W_X$, $\sigma_{V_{Tx}}/\mu_{V_{Tx}}=10\%$, r=0		
	Square Root	**Proposed**
3σ error in leakage	23.58%	1.11%
6σ error in leakage	30.47%	5.98%
$W=10W_X$, $\sigma_{V_{Tx}}/\mu_{V_{Tx}}=10\%$, r=0.1		
	Square Root	**Proposed**
3σ error in leakage	33.61%	0.49%
6σ error in leakage	42.58%	2.37%
$W=10W_X$, $\sigma_{V_{Tx}}/\mu_{V_{Tx}}=10\%$, r=0.4		
	Square Root	**Proposed**
3σ error in leakage	50.58%	0.59%
6σ error in leakage	64.60%	0.30%

VI. CIRCUIT EXAMPLE: SRAM BITLINE DELAY

To check the validity of our model in real circuit scenario, we used a leakage sensitive circuit like SRAM, where large leakage through the access devices of the unaccessed cells of the SRAM array may result in read failure of the SRAM. Worst case scenario happens when the cell which is being accessed contains a '1', and all other cells store '0', as shown in Fig 7(a). In this situation, $\overline{BL}$ starts discharging through the read current of the cell being accessed. However, BL also starts to get discharged by the leakage current of all the unaccessed devices. This increases the time to develop sufficient voltage difference between BL and $\overline{BL}$, thereby causing an increase in the sensing delay. The problem gets

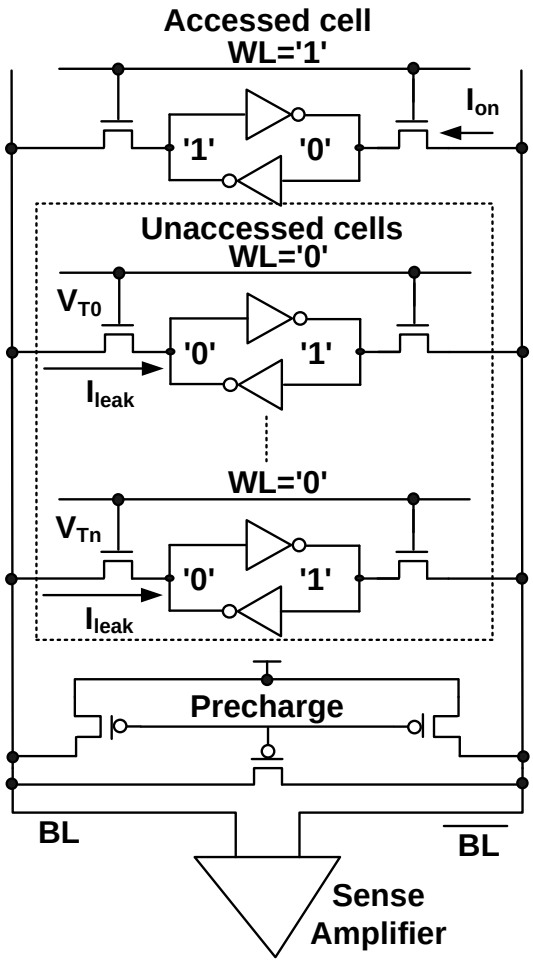


Fig. 7. (a) Schematic showing bitline leakage issue during SRAM read (b) Waveforms showing increase in the bitline delay due to leakage current in unaccessed cells.

even worse with increased number of cells per bitline. In Fig. 7(b) BL and $\overline{\text{BL}}$ waveforms are shown during the read access. Bitline sensing delay is seen to increase from 36ps to 44ps in presence of leakage.

We can successfully use our proposed leakage variation model to estimate SRAM bitline delay. We lumped all the unaccessed cells of the bitline into a single cell whose width is equal to the width of a single device multiplied by the number of the unaccessed cells in the bitline. We then performed Monte Carlo simulation for golden, square root and proposed schemes assuming 64, 128 and 256 devices in the bitline assuming $\sigma_{V_T}/\mu_{V_T}$for a single device to be 15%. The results are shown in Fig. 8 with the percentage estimation errors on top of the bars for the square root method and proposed method. As we can see, estimation error in 3σ bitline delay increases with more number of devices attached to the bitline. However, proposed method maintains a high accuracy with less than even 0.5% error in all the cases.

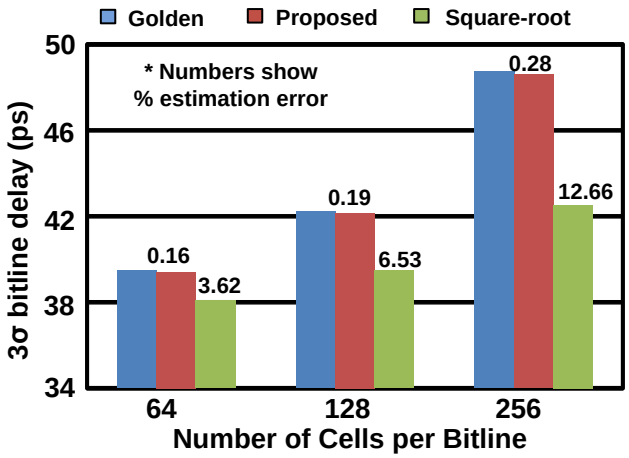


Fig. 8. Comparison between golden, square root and proposed method for 3σ bitline delay due to SRAM bitline leakage.

VII. CONCLUSION

Steep SS devices are being deemed as one of the promising successors of MOSFETs in the domain of low power applications. However, steepness of the SS makes these devices vulnerable to leakage variation due to random V_T shift. Conventional square root method is unable to model this leakage variation accurately. In this paper, we have presented a method based on Wilkinson's approach in order to estimate leakage variation in steep SS devices with extremely high accuracy. To show the correctness of our proposed scheme, we performed various Monte Carlo simulations, which showed that using our model worst-case error in estimating 6σ leakage current is less than 11%, whereas it goes up to 65% in case square root model is used instead. We also presented a circuit example based on SRAM read delay issue due to the bitline leakage. In the worst case, square root method underestimates the 3σ bitline delay by about 13%. However, worst-case 3σ bitline delay using our model is as low as less than 0.5%.

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