An Aging Model for Current DACs, and its Application to Analyzing Lifetime Degradation in a Wireline Equalizer

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Abstract

Temporal degradation of transistors due to aging causes mismatch in the current mirror, a matching-critical building block of current digital to analog converters (IDACs). This mismatch induces non-linearity in IDAC behavior and can cause nonmonotonicity in the worst case. This paper performs an application-driven analysis of IDAC aging within a feed-forward equalizer (FFE) context. The work first models the effect of aging-induced mismatch over IDAC performance metrics and analyzes the performance shifts of IDACs over different topologies and input distributions. Next, the work illustrates how IDAC aging affects FFE behavior and presents novel schemes for FFE calibration to counter the impact of IDAC aging effectively.

Keywords: Aging, mismatch, current mirror, IDAC, equalizer.

1. Introduction

Compatibility to digital technology, high operating speeds, and low area footprint have made the current-mode digital-to-analog converter (IDAC) a popular choice of DAC implementation in state-of-the-art mixed-signal SoCs. An IDAC is the preferable option of converter for high-speed link (HSL) components operating at multi-GHz frequency, such as feed-forward equalizers [1], decision feedback equalizers [2], and linear equalizers [3], due to its fast response time. HSLs are often subject to high data rates as well as high levels of activity. As a result, especially in deeply-scaled technologies, IDACs in the HSL are subject to aging-induced performance degradation that can cause nonlinearity and nonmonotonicity, at the worst case.

Temporal performance shifts of IDACs can vary based on the architectural decisions, such as implementation topologies and bit position of segmentation, and distribution of inputs that depends on IDAC applications. Hence, understanding the significance of IDAC design choices and input distribution is essential to counteract aging-induced performance degradation efficiently. With this objective, the work performs an application-driven detailed modeling study of IDAC aging. We show how aging induces mismatch over time in matched transistors and the induced mismatch affects IDAC behavior over time. We study the impact of aging within the context of a feed-forward equalizer (FFE) used in an HSL. In contrast, prior studies on IDAC aging [4, 5] have examined aging in standalone current-steering DACs. We also present novel methods to optimize FFE performance after aging. Unlike the contemporary IDAC calibration schemes presented in prior works [6, 7, 8, 9, 10], our proposed techniques consider aging-induced performance shifts of IDACs and are application specific, i.e., they utilize the operating principles of FFE to counter IDAC aging. Our study incorporates the calibration methods used in analog systems to recover from performance drifts. A preliminary version of this work appeared in [11]. This work enhances the work in [11] through the following additions:

- The models for estimating performance drifts of IDACs are generalized for any digital encoding scheme (unary, binary-weighted, and segmented); the models in [11] were limited to binary-weighted IDACs only.
- Aging-induced nonlinearities in a current-switching DAC significantly vary with input code distribution (Section 7). This paper explores input distributions of three different categories: unvarying, binomial, and uniform. In comparison, [11] only explored unvarying inputs.
- This paper illustrates how the position of segmentation can affect the performance of a segmented IDAC configured with a current-switching architecture. This part is entirely new to this manuscript, since segmented IDACs were not previously considered.
- A complete study is presented of the effects of IDAC aging on its application in an FFE, illustrating how aging can affect the adaptive equalization scheme. A new technique is proposed to counteract the impact of aging in this scheme. In comparison, [11] explored the lone pulse equalization scheme only.

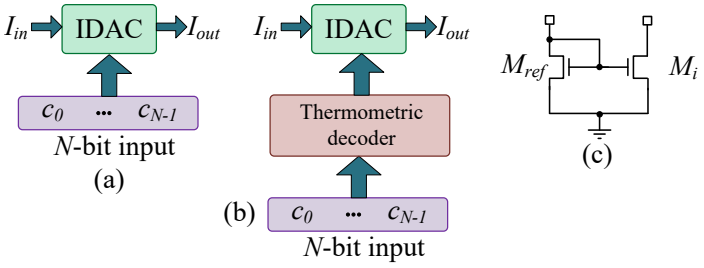

Fig. 1. (a) Binary-weighted IDAC and (b) unary IDAC configurations. (c) Structure of a current mirror (CM) used within these IDACs.

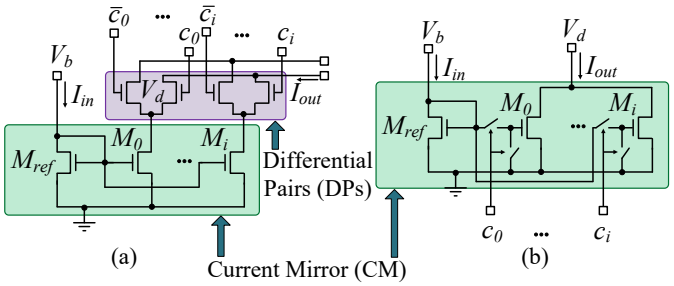

Fig. 2. IDAC schematic: (a) current-steering, (b) current-switching topology.

- Finally, this paper includes qualitative remarks throughout the result section of this paper that can help circuit designers to improve IDAC's robustness to aging.

The paper is organized as follows: Sec. 2 discusses the IDAC operating principle with an analytical approach; Sec. 3 presents analytical models to estimate performance shifts of IDAC due to aging; Sec. 4 provides a brief description of FFE, a requisite for subsequent sections; Sec. 5 explains different coefficient selection schemes of FFE and how aging affects these schemes; Sec. 6 presents novel approaches to counter IDAC aging in an FFE; Sec. 7 includes the results of our analyses to illustrate the impact of aging in IDAC and FFE, as well as to demonstrate how our proposed schemes effectively counter IDAC aging in an FFE; and Sec. 8 concludes the paper.

2. Analysis of IDACs

2.1. IDACs: Operating Principles

Given an integer value, c, as input, a current digital-to-analog converter (IDAC) scales an analog input current, I_{in}, to generate an analog output current, I_{out}, using a digital representation of the input. Based on the digital encoding scheme used for c, IDAC architectures are categorized into three classes: *binary-weighted*, *unary*, and *segmented IDACs*. These three classes differ in how they convert an input current, I_{in}, to the output current I_{out}.

A *binary-weighted* IDAC (Fig. 1(a)) uses an N-bit binary encoding of c, i.e., $0 \leq c < 2^N$, to generate

$$I_{out} = \left(\sum_{i=0}^{N-1} c_{b,i} \cdot \mathcal{R}_i \right) I_{in} \tag{1}$$

Here, $c_{b,i}$ is the i^{th} bit in the binary representation of c. An appropriately sized current mirror (CM) (Fig. 1(c)) translates the input current I_{in} through schematic transistor M_{ref} to the current $(\mathcal{R}_i I_{in})$ through schematic transistor M_i, where $\mathcal{R}_i$ is the transfer ratio for M_i. For binary-coded input, M_i is sized at $2^i\times$ relative to M_{ref}. In the FinFET technology used in our analyses, each sized schematic transistor is implemented using multiple discrete FinFETs, e.g., a $4\times$ transistor is implemented as four FinFETs.[1]

[1] M_{ref} could be implemented using f FinFETs; if so, the other transistor sizes and indices could be scaled up by f. For ease of exposition, we assume a unit-sized M_{ref}.

A *unary* IDAC (Fig. 1(b)) uses a thermometric decoder to convert an N-bit binary representation of c is to a $(2^N - 1)$-bit thermometer code, generating the output current as follow:

$$I_{out} = \left(\sum_{i=0}^{2^N-2} c_{t,i} \cdot \mathcal{R}_i \right) I_{in} \tag{2}$$

where $c_{t,i}$ is the i^{th} bit in the thermometer-coded representation of c. In contrast to binary-weighted IDAC, the transfer ratio $\mathcal{R}_i$ for transistor M_i is independent of the position, i, in a unary IDAC architecture, and is implemented with equal sizing of M_i, irrespective of i.

A *segmented* IDAC partitions the binary representation of input c into two segments: the P least significant bits (LSBs) use a binary-weighted IDAC, and the $(N-P)$ most significant bits (MSBs) use a unary IDAC structure. Binary-weighted IDAC requires fewer resources compared to unary IDAC. On the other hand, unary IDAC is inherently monotonic [12]. A segmented IDAC balances the trade-offs of binary-weighted and unary IDAC architectures. The output current of the segmented IDAC can be written as:

$$I_{out} = (\underbrace{\sum_{i=0}^{P-1} c_{b,i} \cdot \mathcal{R}_{b,i}}_{\text{Binary-weighted IDAC}} + \underbrace{\sum_{i=0}^{2^{(N-P)}-2} c_{t,i} \cdot \mathcal{R}_{t,i}}_{\text{Unary IDAC}}) I_{in} \tag{3}$$

Here, the transfer ratio $\mathcal{R}_{b,i}$ is the same as in the binary-weighted scheme (i.e., the size of transistor M_i is $2^i\times$ that of M_{ref}), and $\mathcal{R}_{t,i}$ is as in the thermometer scheme (i.e., all transistors M_i are identically sized to $2^P\times$ the size of M_{ref}); $c_{b,i}$ and $c_{t,i}$ are bit by positions in the the binary-coded and thermometer-coded segments of c that can be mapped to decimal values, c_b and c_t, respectively, such that:

$$c_b = \sum_{i=0}^{P-1} c_{b,i} \cdot 2^i; \; c_t = \sum_{i=0}^{2^{(N-P)}-2} c_{t,i} \cdot 2^P \tag{4}$$

Here, $\mathcal{R}_{t,i}$ is identical for all transistors in unary IDAC and sized $2^P\times$ relative to M_{ref}.

In other words, the segmented IDAC is a generalization of the other two schemes: it reduces to a binary-weighted IDAC when $P = N$, and to a unary IDAC when $P = 0$.

Based on the implementation technique, IDAC architectures can be realized with two different topologies [13]: *current-steering*, and *current-switching* (Fig. 2). Both topologies use a current-mirror (CM) to convert an analog input current, I_{in}, to a scaled analog output current, I_{out}, by binary-coded or thermometer-coded digital input. The current-steering DAC also includes a set of differential pairs (DPs), which function in "digital mode" with input values at logic 1 or logic 0. For the DP, aging only affects the settling time of the output, and its impact can be minimized with wider transistors. On the other hand, as we will show, IDAC performance is very susceptible to CM aging.

Notation: We summarize our notation below:

- c_i: The i^{th} bit in the digital input code of c. In specific scenarios, if we have a binary-weighted or thermometric representation, we may more specifically refer to c_i as
  - $c_{b,i}$, which represents the i^{th} bit in the binary-weighted digital input code of c_b, $0 \le i < N$.
  - $c_{t,i}$, which is the i^{th} bit in the thermometer code of c_t, $0 \le i < 2^N - 1$.
- M_i: the i^{th} transistor in the schematic.
- $M_{i,j}$: the j^{th} FinFET in M_i. The range of j, for M_i in: ∘ binary-weighted IDAC is $0 \le j < 2^i$.
  ∘ unary IDAC is $0 \le j < 2^P$ where $P \ge 0$.
- $\mathcal{R}_{i,j}$: FinFET transfer ratio, $(I_{M_{i,j}}/I_{M_{ref}})$ from the reference transistor current to the current in FinFET $M_{i,j}$.
- $\mathcal{R}_i$: transfer ratio of bit i, the ratio $(I_{M_i}/I_{M_{ref}})$ from the current in M_{ref} to that in schematic transistor M_i.
- $\Delta[M_{ref}, M_{i,j}] = \Delta V_{th,M_{ref}} - \Delta V_{th,M_{i,j}}$: threshold voltage mismatch between FinFETs $M_{i,j}$ and M_{ref}.

Based on this notation, the current through M_i is:

$$I_{M_i} = c_i \cdot \mathcal{R}_i \cdot I_{in} = \sum_j (c_i \cdot \mathcal{R}_{i,j})\, I_{in} \tag{5}$$

We use $V_{GS,M_{i,j}}$ and $V_{DS,M_{i,j}}$ to denote the gate-to-source and drain-to-source voltages, respectively, of $M_{i,j}$. In both IDAC topologies, M_{ref} is a diode-connected transistor that converts an input current, I_{in}, to a voltage, V_b. Hence,

$$V_{GS,M_{ref}} = V_{DS,M_{ref}} = V_b \tag{6}$$

In the current-steering topology, the gate node of each FinFET in M_i is always connected to V_b. In the current-switching topology, the gate of M_i is connected to V_b if $c_i = 1$ (i.e., $V_{GS,M_i} = V_b$), or to ground if $c_i = 0$ (i.e., $V_{GS,M_i} = 0$).

In the ideal circuit, all FinFETs have identical threshold voltage, $V_{th,\mu}$. Process variations are minimized using larger transistor sizes and using layout techniques such as common-centroid. If $V_{GS,M_{i,j}} = V_b$, then for all FinFETs $M_{i,j}$ of M_i,

$$V_{DS,M_{i,j}} = V_d \approx V_b - V_{th,\mu} \tag{7}$$

These transistors are placed in saturation to maximize output current, and V_d is chosen to maximize output swing.

The transfer ratio, $\mathcal{R}_{i,j} = I_{M_{i,j}}/I_{M_{ref}}$ for FinFET $M_{i,j}$ can be represented using the alpha-power law [14] as:

$$\mathcal{R}_{i,j} = \left[\frac{V_{GS,M_{i,j}} - V_{th,M_{i,j}}}{V_{GS,M_{ref}} - V_{th,M_{ref}}}\right]^{\alpha} \left[\frac{1 + \lambda V_{DS,M_{i,j}}}{1 + \lambda V_{DS,M_{ref}}}\right] \tag{8}$$

2.2. Performance for the Ideal Case

In this subsection, we present the expressions of various performance parameters that are used to analyze the impact of aging of an IDAC. Generalized expressions are presented for N-bit segmented IDAC consisting of a P-bit binary-weighted IDAC and an $(N - P)$-bit unary IDAC that can easily be mapped for N-bit binary-weighted IDAC and N-bit unary IDAC by setting $P = N$ and $P = 0$, respectively.

Ideally, $V_{GS} = V_b$ and $V_{th} = V_{th,\mu}$, the nominal value, for all transistors. The circuit performance parameters are:

FinFET transfer ratio: For each FinFET $M_{i,j}$,

$$\mathcal{R}_{i,j} = \left[\frac{V_b - V_{th,\mu}}{V_b - V_{th,\mu}}\right]^{\alpha} \left[\frac{1 + \lambda V_d}{1 + \lambda V_b}\right] = \frac{1 + \lambda V_d}{1 + \lambda V_b} \triangleq r \tag{9}$$

Transfer ratio of the i^{th} transistor: For the binary-weighted IDAC segment, the transfer ratio for bit position i can be modeled as:

$$\mathcal{R}_{b,i} = \sum_{j=0}^{2^i - 1} \mathcal{R}_{i,j} = 2^i \cdot r \tag{10}$$

For the unary IDAC segment, the transfer ratio of a transistor is independent of bit position i, and dependent on the minimum bit position in the array segment of the binary-coded input bits, P, it is handling:

$$\mathcal{R}_{t,i} = \sum_{j=0}^{2^P - 1} \mathcal{R}_{i,j} = 2^P \cdot r \text{ where } P \ge 0 \tag{11}$$

If l represents the bit position in combined representation of an input that uses a P-bit binary code and an $(N - P)$-bit thermometer code, the transfer ratio of the segmented

IDAC can be represented as:

$$\mathcal{R}_l = \begin{cases} \mathcal{R}_{b,l}, 0 \le l < P \\ \mathcal{R}_{t,l}, l \ge P \end{cases} \tag{12}$$

Finding I_{out}: For the segmented IDAC, we can calculate I_{out} combining Eqs. (3), (4), (10), and (11) as follows:

$$\begin{aligned} I_{out} &= \left(\sum_{i=0}^{P-1} c_{b,i} \cdot \mathcal{R}_{b,i} + \sum_{i=0}^{2^{(N-P)}-2} c_{t,i} \cdot \mathcal{R}_{t,i} \right) I_{in} \\ &= \left[\sum_{i=0}^{P-1} c_{b,i} \cdot 2^i + \sum_{i=0}^{2^{(N-P)}-2} c_{t,i} \cdot 2^P \right] \cdot r \cdot I_{in} \\ &= (c_b + c_t) \cdot r \cdot I_{in} = c \cdot r \cdot I_{in} \end{aligned} \tag{13}$$

Gain: For an IDAC, gain is the ratio of full-scale current, I_{FS}, of the IDAC that corresponds to the maximum range of its input, c^{max}. Gain of the segmented IDAC can be measured using (13) as follows:

$$G = \frac{I_{FS}}{c^{max}} = \frac{c^{max} \cdot r \cdot I_{in}}{c^{max}} = r \cdot I_{in} \tag{14}$$

Differential nonlinearity (DNL): To compute DNL for an input c, we determine the step size in the output current in moving from input word $c-1$ to c, and compare it with the ideal gain for a single step (Eq. (14)):

$$\text{DNL}_c = (I_c - I_{c-1}) - r \cdot I_{in} \tag{15}$$

For the segmented IDAC, the step size in the ideal case can be calculated using Eq. (13) as follows:

$$I_c - I_{c-1} = c \cdot r \cdot I_{in} - (c-1) \cdot r \cdot I_{in} = r \cdot I_{in} \tag{16}$$

Integral nonlinearity (INL): The INL of an input c is the difference between actual output and ideal output for the input c, and can be represented as:

$$\text{INL}_c = I_c - c \cdot r \cdot I_{in} \tag{17}$$

For the ideal case, from Eq. (13), $\text{INL}_c = 0$ for all c.

3. Aging Effects in IDACs

3.1. Aging Model

We consider the impact of aging on FinFET-based IDAC circuits with n-type FinFETs. We focus on hot carrier degradation (HCD) induced aging that causes a positive threshold voltage shift, ΔV_{th}, in n-type FinFETs prompting V_{th} to increase over time, t. We ignore smaller PBTI shifts as its impact can be considered negligible compared to HCD [15]. We extend the model in [16] to incorporate dependency of the threshold voltage shift to channel length using data from [17].

The impact of aging at time t is modeled as:

$$\Delta V_{th} = V_{th} \left(1 - e^{[-(\beta \cdot t/\tau_L)^n]} \right) \tag{18}$$

$$\begin{aligned} \text{where } \tau &= \frac{A}{e^{[\Gamma_{A2}(V_{DS})]}} e^{[\Gamma_{A1}(V_{DS} - \gamma V_{GS})]} \\ \tau_L &= \tau e^{[s(L-L_0)]} \\ n &= n_0 e^{[-(\beta \cdot t/\tau_n)^\kappa]} \\ A &= A_1 e^{[-E_a/(kT)]} \\ \beta &= \beta_1 \cdot \beta_2 \end{aligned}$$

Here, k is Boltzmann's constant; L is the gate length; β_1 is the activity factor of the FinFET in IDAC; β_2 is the activity factor of the IDAC; the temperature $T = T_0 + T_{SH}$ where T_0 is the base temperature and T_{SH} is the local temperature rise due to device self-heating. We incorporate self-heating using the equations in [16]. Other model parameters are: $\Gamma_{A1} = 3.85\text{V}^{-1}$, $\Gamma_{A2} = 9.40\text{V}^{-1}$, $\gamma = 5.2$, $s = 0.045\text{s/nm}$, $L_0 = 14\text{nm}$, $n_0 = 0.8$, $\tau_n = 10^5\text{s}$, $\kappa = 0.036$, $A_1 = 6 \times 10^{13}\text{s}$, $E_a = -0.58\text{eV}^{-1}$.

3.2. Performance Shifts due to Aging

A transistor only ages at the active state when it carries current. During normal operation, the M_{ref} transistor is always active. In the current-steering DAC, FinFETs $M_{i,j}$ in the CM are also always active, but in the current-switching DAC, $M_{i,j}$ may be active or inactive, depending on c_i. Even if $M_{i,j}$ is active, from Eq. (7), $V_{DS,M_{i,j}} < V_{DS,M_{ref}}$.

Moreover, in a diode-connected configuration, at a constant current I_{in}, V_{th} degradation in M_{ref} implies that $V_{GS,M_{ref}}$ increases over time to maintain the I_{in}. This causes $V_{DS,M_{ref}} = V_{GS,M_{ref}}$ to rise [18], further worsening the gap between M_{ref} and $M_{i,j}$. Therefore, M_{ref} typically undergoes more HCD aging than FinFETs $M_{i,j}$. The imbalance in aging rates leads to *mismatch* between transistors, quantified as:

$$\Delta[M_{ref}, M_{i,j}] = \Delta V_{th,M_{ref}} - \Delta V_{th,M_{i,j}} \tag{19}$$

The aging equation (18) models this mismatch, based on factors such as time, activity factor, and applied voltage.

We present expressions that quantify the impact of aging-induced shifts on IDAC performance parameters. The expressions are derived for N-bit segmented IDAC consisting a P-bit binary-weighted IDAC and a $(N-P)$-bit unary IDAC. The expressions can easily be mapped for N-bit binary-weighted IDAC and N-bit unary IDAC by setting $P = N$ and $P = 0$, respectively. Proofs for these expressions are provided in Appendix A.

FinFET transfer ratio: The shift in the transfer ratio of an individual FinFET $M_{i,j}$ is as follows:

$$\Delta \mathcal{R}'_{i,j} = \frac{\alpha \cdot r}{(V_b - V_{th,\mu})} \cdot \Delta[M_{ref}, M_{i,j}] \tag{20}$$

$$= \alpha K_1 r \cdot \Delta[M_{ref}, M_{i,j}] \tag{21}$$

Here, $K_1 = 1/(V_b - V_{th,\mu})$.

Transfer ratio: For a P-bit binary-weighted IDAC, the transfer ratio shift of the i^{th} transistor is given by:

$$\Delta\mathcal{R}'_{b,i} = \alpha K_1 r \sum_{j=0}^{2^i-1} \Delta[M_{ref}, M_{i,j}], 0 \leq i < P \tag{22}$$

For $(N-P)$-bit unary IDAC, the transfer ratio shifts by:

$$\Delta\mathcal{R}'_{t,i} = \alpha K_1 r \sum_{j=0}^{2^P-1} \Delta[M_{ref}, M_{i,j}], 0 \leq i < 2^{(N-P)} - 1 \tag{23}$$

If l represents the bit position in a combined representation of a P-bit binary-coded and an $(N-P)$-bit thermometer-coded input, the shift in the transfer ratio of the segmented IDAC can be represented as follows:

$$\Delta\mathcal{R}'_l = \begin{cases} \alpha K_1 r \sum_{j=0}^{2^l-1} \Delta[M_{ref}, M_{l,j}], 0 \leq l < P \\ \alpha K_1 r \sum_{j=0}^{2^P-1} \Delta[M_{ref}, M_{l,j}], l \geq P \end{cases} \tag{24}$$

I_{out}: The output current perturbation due to aging is given by:

$$\Delta I_{out} = I_{in} \left[\sum_{i=0}^{P-1} c_{b,i} \Delta\mathcal{R}'_{b,i} + \sum_{i=0}^{2^{(N-P)}-2} c_{t,i} \Delta\mathcal{R}'_{t,i} \right] \tag{25}$$

Gain: The shift in the gain due to aging is:

$$\Delta G = \frac{I_{in}}{2^N - 1} \left[\sum_{i=0}^{P-1} \Delta\mathcal{R}'_{b,i} + \sum_{i=0}^{2^{(N-P)}-2} \Delta\mathcal{R}'_{t,i} \right] \tag{26}$$

DNL: Without any calibration, the differential nonlinearity after aging is:

$$\text{DNL}_c = I_{in} \left[\sum_{i=0}^{N-1} \left[c_{b,i} - (c-1)_{b,i}\right] \Delta\mathcal{R}'_{b,i} + \sum_{i=0}^{2^{(N-P)}-2} \left[c_{t,i} - (c-1)_{t,i}\right] \Delta\mathcal{R}'_{t,i} \right] \tag{27}$$

INL: Without any calibration, the integral nonlinearity introduced by aging is:

$$\text{INL}_c = I_{in} \left[\sum_{i=0}^{N-1} c_{b,i} \Delta\mathcal{R}'_{b,i} + \sum_{i=0}^{2^{(N-P)}-2} c_{t,i} \Delta\mathcal{R}'_{t,i} \right] \tag{28}$$

Note that all terms depend on the mismatch, $\Delta[M_{ref}, M_{i,j}]$. A slower aging rate of both M_{ref} and $M_{i,j}$ will result in a smaller $\Delta[M_{ref}, M_{i,j}]$. Since gate length, L, affects both devices simultaneously, larger gate-length causes smaller ΔV_{th} (Eq. (18)) and smaller $\Delta[M_{ref}, M_{i,j}]$ as a consequence. Hence, a proper selection of L in the design phase can be used to quantify aging and contain $\Delta[M_{ref}, M_{i,j}]$ in the acceptable range.

In modern systems, the aging-induced gain error, ΔG, can be calibrated to zero by tuning I_{in}. Regulating $\Delta G = 0$ will also set DNL and INL to zero in a segmented IDAC with the current-steering configuration (Appendix B). However, I_{in} tuning only scales the nonlinearities in a segmented IDAC with the current-switching configuration, and the extent of nonlinearities varies based on the input distribution, and position of segmentation, P. We illustrate these facts in Section 7.

3.3. Susceptibility to aging-induced nonmonotonicity

Nonmonotonicity is an undesirable property in an IDAC, and it can cause system-level failures when the IDAC is used in a larger system. An IDAC is nonmonotonic if its output displays a negative step size as the input moves from $c-1$ to c, i.e., if $\text{DNL}_c < -1\times$LSB.

The value of DNL_c only depends on the bitwise difference between the digital representation of successive input codes, $c-1$ and c. At $t = 0$, the contribution of aging to DNL_c is zero for all c for an ideal IDAC (Eq. 15). As the transistors age with time, the contribution of aging to DNL_c shifts from zero. In thermometer encoding, successive codes only flip one bit from zero to one, irrespective of N. Hence, the step size of an aged unary IDAC for any c is positive. In unary IDAC with the current-steering topology, $\text{DNL}_c \geq 0\times$LSB as all transistors age at the same rate. In unary IDAC with the current-switching topology, $\text{DNL}_c > -1\times$LSB as only one device will switch with successive inputs. Consequently, a unary IDAC is robust to nonmonotonicity. On the other hand, successive codes can flip a bit both ways, from zero to one or from one to zero, in a binary-weighted IDAC. Moreover, the number of bits that can flip in a binary encoding of successive inputs increases with N. Hence, unlike a unary IDAC, DNL_c can be $< -1\times$LSB in an aged binary-weighted IDAC with the current-switching topology, and the range of aging-induced $|\text{DNL}_c|$ increases with N.

The robustness of a unary IDAC to nonmonotonicity comes at the cost of additional resources, such as the overhead of a thermometric decoder (Fig. 1), whose area and power overhead increase at the exponential rate of 2^N with the number of binary bits, N. A segmented IDAC balances the advantages and disadvantages of binary-weighted and unary IDAC architectures by lowering the overhead and countering process variations. This architecture ensures monotonicity at $t = 0$ by partitioning the design at a bit position P that defines the LSB handled by the unary IDAC segment. However, unlike a unary IDAC, a segmented IDAC with the current-switching configuration is susceptible to aging-induced nonmonotonicity due to the partially binary-weighted IDAC substructure within the architecture.

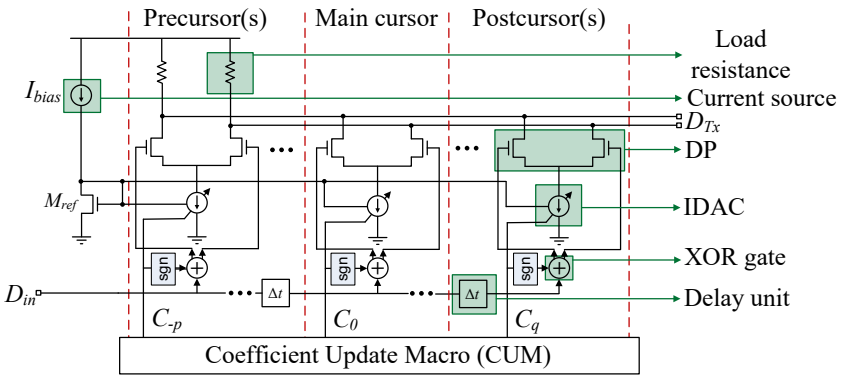

Fig. 3. Schematic of a feed-forward equalizer (FFE) architecture.

4. FFE Circuit Structure

The feed-forward equalizer (FFE) is a multi-tap multi-level transmit equalizer that reduces inter-symbol interference (ISI) when data is transmitted through a wired channel. The transmitted data bounces between two voltage levels, V_{Tx}^{max}, and V_{Tx}^{min}. The channel is band-limited and attenuates the high-frequency contents of the Tx pulse causing energy of a pulse to be dispersed over adjacent pulse positions. This energy dispersion introduces precursor ISI and postcursor ISI to the future and past pulses, respectively. An FFE counters ISI by shaping the outgoing pulse, transmitting a weighted sum of past, present, and future pulse(s). The weights are regulated by coefficients that can be adjusted adaptively (e.g., during each power-up). An automatic level control algorithm is used on the Tx side to maintain a fixed peak-to-peak output, V_{Tx}^{max} to V_{Tx}^{min}, as coefficients change. The core of the FFE (Fig. 3) consists of:

Taps For each of the past, present, and future pulses that are summed to generate the equalized pulse, the FFE has a tap and a coefficient, c^j, associated with it where j indicates the position of the pulse. For an FFE that considers p precursor(s), the main cursor, and q postcursor(s), the coefficients can be represented as a vector:

$$\mathbf{C} = \left[c^{-p}, \cdots, c^0, \cdots, c^q\right] \text{ where } \sum_{j=-p}^{q} |c^j| = C^{tot} \tag{29}$$

Here, C^{tot} is the maximum allowable value of any tap-coefficients. The latter condition is set to limit the maximum swing of the equalized pulse.

Delay Units (DUs) The input bit stream propagates through a set of DUs, Δt, to ensure that the precursor(s), main cursor, and postcursor(s) are fed to the FFE at the right time. An FFE with $(p+q+1)$ taps includes $(p+q)$ DUs.

Differential Pairs (DPs) A set of DPs are used for each precursor, main cursor, and postcursor, to propagate each input bit to the channel using two complementary signals.

IDACs The IDACs convert each tap coefficient to an appropriately weighted multiple of a reference bias current, I_{bias}. The weights determine the relative importance of the main cursor, precursor(s), and postcursor(s).

Resistive load (R_{load}) The load terminates the transmission line at the transmitter side and corresponds to the characteristic impedance of the channel. The differential voltage drop across the resistive loads is the transmitted signal, D_{Tx}.

XOR gates Depending on the sign of the coefficient, detected using the sgn(.) function, an XOR gate sends data to DP for the pre/main/postcursors in either true or complemented form.

The DP is driven by two complementary digital inputs. It is relatively insensitive to aging, and only requires transistors to remain in the linear region even after aging. It is easy to ensure this. On the other hand, the IDACs, which translate the coefficient weights into precise analog currents, are very analog in nature, and undergo significant aging effects.

The current-steering DAC is aging-resilient, as illustrated in Section 7, but, it can consume extra voltage headroom to accommodate DPs. This limits the output voltage swing [19], making it more susceptible to noise and perturbation. Hence, a current switching DAC and circuits with similar topology, e.g., current-mode logic drivers, are prevalent in HSLs. We will consider an FFE with a current-switching DAC, quantifying the impact of aging on FFE performance in Section 5, and presenting mitigation schemes for recalibration in Section 6.

5. FFE Performance Analysis

5.1. Operation under Nominal Conditions

In the FFE, the vector of tap coefficients, $\mathbf{C}$, regulates the weights of the main pulse and its adjacent pulses to generate the equalized pulse. For this purpose, absolute values of these tap coefficients are used in an encoded format as inputs to IDACs to generate a set of weighted currents. These are represented by the weight vector:

$$\mathbf{W} = [I_{-p}, \cdots, I_0, \cdots, I_q] = I_{bias} \cdot r \cdot \left[c^{-p}, \cdots, c^0, \cdots, c^q\right]$$

Since in the ideal case, for tap τ, $I_\tau = c^\tau \cdot r \cdot I_{bias}$ (Eq. (13)),

$$c^{-p} : \cdots : c^0 : \cdots : c^q = I_{-p} : \cdots : I_0 : \cdots : I_q \tag{30}$$

$$I_{tot} = \sum_{j=-p}^{q} |I_j| = C^{tot} \cdot r \cdot I_{bias} \tag{31}$$

Fig. 4(a) shows an unequalized pulse and its equalized output with a 3-tap equalizer (one precursor, one main cursor, and one postcursor) at the transmitter end. Fig. 4(b) shows the pulse responses of the unequalized and equalized pulse of Fig. 4(a) at the receiver end: a narrower spread of the pulse response mitigates ISI.

Coefficient selection: Figure 5(a) shows a simplified block diagram illustrating the tap coefficient assignment process of FFE that includes a separate channel to communicate data back to the transmitter from the receiver [20]. To set the tap coefficients, a pulse or sequence of pulses is generated from the transmitter and propagated through the channel. A sample and hold (S/H) circuit samples response of the pulse or sequence of pulses, attenuated by the channel, at the receiver. Based on the sampled data, a coefficient generator (CG) module at the receiver calculates the optimal tap coefficients required to minimize read failures at the receiver. These coefficients are sent to the transmitter with an up-channel protocol [21]. At the transmitter, a coefficient update macro (CUM) module receives, stores, and inputs these tap coefficients to the FFE.

The tap coefficients are determined by the CG module using either of the following approaches [22, 23, 24]:

Lone-pulse equalization: In this process, the transmitter generates a pulse, at the operating frequency with the maximum allowable amplitude, V_{Tx}^{max}, on system power-up:

$$V_{Tx}(t) = V_{Tx}^{max} \cdot [u(t) - u(t-T)] \tag{32}$$

Here, $u(t)$ is the unit step function and T is the pulse width.

The signal propagates through the channel, whose impulse response is $h(t)$, and creates a response at the receiver:

$$V_{Rx}(t) = (V_{Tx}^{max} \cdot [u(t) - u(t-T)]) * h(t) \tag{33}$$

where $*$ represents the convolution operator. The receiver samples the channel-modulated signal, V_{Rx}. Under a fixed equalization scheme with a given number of p past pulses (precursors) and q future pulses (postcursors) to be used, along with the current pulse (main cursor), for equalization, the receiver establishes the vector of tap coefficients, $\mathbf{C}$, from V_{Rx} using an equalization algorithm, such as, zero forcing solution (ZFS) or minimum mean square error (MMSE) [23].

Adaptive equalization: In this approach, the tap coefficients are initialized to a convenient set of values, e.g., tap coefficients of the main cursor and other cursor(s) are set to the maximum and minimum, respectively [25]. Next, a known data sequence is propagated through the channel from the transmitter. Using the response of the known sequence sampled at the receiver, coefficient c^j, for each tap j is adjusted using an error function, f_e, and an input function, f_i, as follows:

$$c^j(t+1) = c^j(t) + \mu f_e(\hat{V}_{Rx}(t) - V_{Rx}(t)) \cdot f_i(V_{Tx}(t - j\Delta t))$$

Here, V_{Tx} is the pulse amplitude of the training sequence at the transmitter; V_{Rx} and $\hat{V}_{Rx}$ are the actual and expected pulse amplitude at the receiver, respectively; μ is the scaling factor for tap adjustment; and Δt is propagation delay of a DU. For implementation simplicity, the sign-sign least mean square (LMS) algorithm is widely used in the adaptive equalization process: sgn(.) is used for f_e and f_i.

Unlike the lone-pulse equalization process, adaptive equalization can continue at runtime through, replacing the training sequence with the decision of the receiver on V_{Rx} [24].

5.2. Impact of Aging on the FFE

The tap coefficients of an FFE are determined to cancel ISI from the data to be transmitted considering channel characteristics, environmental conditions, and data rates. In ideal scenario, tap coefficients, $\mathbf{C}$, and the weighted current generated from a set of IDACs using the tap coefficients, $\mathbf{W}$, maintain Eq. (30) which is important for effective ISI cancellation. In practical scenario, a smaller difference between the ratio among coefficients and the weighted current will cause better ISI cancellation. This balance between the coefficients and weighted currents can only be maintained if all transistors, $M_{i,j}$, in the current mirror (CM) of all IDACs of the FFE age at the same rate causing identical transfer ratio, $R'_{i,j}$, over time (Eq. (46)). This is unlikely to happen in an FFE with current-switching DACs, since:

(i) in a multi-tap FFE, each c^j in $\mathbf{C}$ can be significantly different from each other as these can vary in a wide range: c^j is only limited by Eq. (29) and the range of input of the IDAC it is associated with. For example, the tap coefficient of the main cursor is usually kept larger than the sum of rest of the tap coefficients and assigned a value above the center of its range, since it incorporates the weight of the current pulse.

(ii) each bit of the encoded representation of c^j acts as a input to a transistor or group of transistors that controls activity factor of the transistor(s). Unless c^j is assigned to zero or the maximum value of its range, the activity factor of transistors in an IDAC may not be same.

As a consequence, the transfer ratio of each branch of an IDAC may depart from ideal behavior under aging, shifting the weight vector $\mathbf{W}$ of the FFE, generated from the vector of tap coefficient, $\mathbf{C}$, to:

$$\mathbf{W}'(t) = \left[I'_{-p}(t), \cdots, I'_0(t), \cdots, I'_q(t)\right] \tag{34}$$

As the IDAC transistors age over time, the ratio of the coefficients keeps deviating from Eq. (30), since the output currents of each IDAC in an FFE changes (Eq. (25)) at a different rate. Hence,

$$c_{-p} : \cdots : c_q \neq I'_{-p}(t) : \cdots : I'_q(t); \sum_{j=-p}^{q} |I'_j(t)| \neq I_{tot} \tag{35}$$

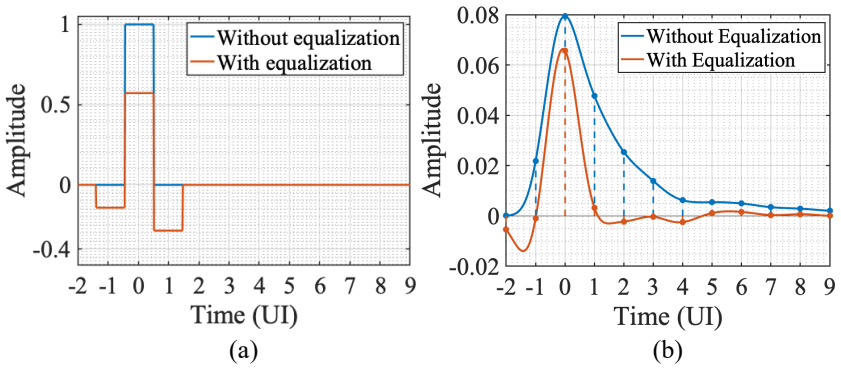

Fig. 4. An unequalized pulse with its precursor and postcursor, and its equalized output. The signal is sampled at integer multiples of the unit interval (UI), and the equalized signal provides low ISI at $t \leq -1$ and $t \geq 1$ [11].

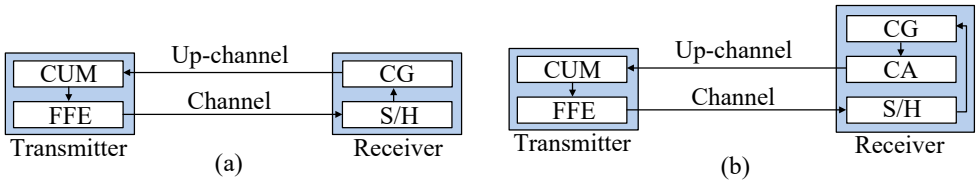

Fig. 5. (a) Conventional communication between Tx and Rx for the FFE. (b) Aging mitigation scheme with CA unit on the Rx side [11].

As a result, for a vector of tap coefficients, $\mathbf{C}$, effective equalization will continuously deviate from expected equalization. We consider the two types of equalization, described earlier in this section, to determine $\mathbf{C}$:

- For *lone-pulse equalization*, the tap coefficients will not change over time if channel characteristics, environment conditions, and data rates remain unchanged. As a consequence, the performance of FFE degrades over time causing vertical and horizontal width of the eye diagram at the receiver to shrink, as illustrated in Sec. 7, increasing bit-error rate (BER) at the receiver.
- For *adaptive equalization*, the tap coefficients will be adjusted automatically at runtime to adapt to the change in effective equalization. However, as we show in Sec. 7, Eq. (35) can introduce nonmonotonicity in IDAC at the worst case, where an increase in coefficient, c^j, causes a decrease in output current, I_j. Nonmonotonicity in an IDAC [26] can mislead the auto-adaptation process of tap coefficients causing performance degradation of FFE.

6. Mitigating FFE Aging

As described in Sec. 3.3, aging may induce nonidealities in the IDAC with the current-switching topology, which can cause the equalization quality of an FFE to drop over time, irrespective of the coefficient selection scheme discussed in Sec. 5.1. In this section, we discuss the limitations of existing calibration methods of IDACs and propose solutions to counter aging-induced performance shifts over time in an FFE, in order to maintain the standard of equalization as the circuit ages.

6.1. Prior works

The basic approach of the calibration techniques of IDAC is to compare the current flowing through each transistor, I_{M_i}, with a reference current, I_{ref}, and tune I_{M_i} to I_{ref} based on the difference from the ideal value. The correction of I_{M_i} is performed either using dynamic storage that requires periodic refreshing or static storage that does not require the data to be refreshed [6]. The dynamic storage-based correction technique applied in [8, 10] uses a gate capacitance that calibrates I_{M_i} through the diode-connected configuration of M_i. After calibration, M_i is driven by the gate capacitance. Such correction methodologies suffer from systematic errors as the configurations M_i are not identical during calibration and operation mode. The static-storage based technique used in [7, 9] avoids the abovementioned systematic error by correcting I_{M_i} in operation mode using a successive approximation register (SAR) and a calibration DAC. However, this technique does not account the mismatch introduced by aging in the asymmetric bias circuit which causes the reference current, I_{ref}, to drift over time.

6.2. Proposed techniques

In this subsection, we propose a novel solution for each of the coefficient selection processes of FFE that utilize the equalization process itself for coefficient adaptation to minimize the impact of IDAC aging in an FFE. Our proposed solutions focus on nullifying the impact of aging-induced error in IDAC through adapting the coefficients to ensure expected equalization. The coefficients of the FFE are

Algorithm 1 Algorithm for obtaining coefficient vector $\mathbf{C}'$

Input: $I^{\tau}_{b,i}\ \forall\ 0 \le i < N, I^{\tau}_{t,i}\ \forall\ 0 \le i < 2^{(N-P)} - 1, -p \le \tau \le q$;
Output: Updated coefficient vector, $\mathbf{C}'$
for $\tau = -p : q : 1$ **do**
  for $i = 0 : 2^{(N-P)} - 2 : 1$ **do**
    $\xi^{\tau}_{t,i} = 0$;
    if $(I^{\tau}_{out} - I^{\tau}_{t,i}) \ge 0$ **then**
      $I^{\tau}_{out} = I^{\tau}_{out} - I^{\tau}_{t,i}$; $\xi^{\tau}_{t,i} = 1$;
    end if
  end for
  for $i = N - 1 : 0 : -1$ **do**
    $\xi^{\tau}_{b,i} = 0$;
    if $(I^{\tau}_{out} - I^{\tau}_{b,i}) \ge 0$ **then**
      $I^{\tau}_{out} = I^{\tau}_{out} - I^{\tau}_{b,i}$; $\xi^{\tau}_{b,i} = 1$;
    end if
  end for
end for

adapted in the operating mode of M_i in IDAC, thus avoiding systematic error suffered by the dynamic-storage based techniques of IDAC correction. Unlike the static-storage based calibration method, the proposed techniques also consider aging of the bias circuit, e.g., diode-connected transistor, M_{ref}. The techniques are described below:

Lone-pulse equalization: In order to achieve correct equalization under aging, we must return the circuit to the original weight vector, $\mathbf{W}$. To achieve this, we dynamically adapt the coefficients $\mathbf{C}$ to a new set,

$$\mathbf{C}' = \left[\xi^{-p}, \cdots, \xi^{0}, \cdots, \xi^{q}\right] \tag{36}$$

Here, a tap, τ, controlled by a coefficient, ξ^{τ}, drives an N-bit segmented IDAC that consists of a P-bit binary-weighted IDAC and a (N–P)-bit unary IDAC with an input of $\xi^{\tau} = [\xi^{\tau}_{b}, \xi^{\tau}_{t}]^T$, such that, $\xi^{\tau}_{b} = [\xi^{\tau}_{b,0}, \cdots, \xi^{\tau}_{b,P-1}]$, $\xi^{\tau}_{t} = [\xi^{\tau}_{t,0}, \cdots, \xi^{\tau}_{t,k}]$, where, $k = 2^{(N-P)} - 2$. The value of N and P can vary from tap to tap.

Note that while I_{bias} can be used as a knob to control I_{tot}, it is not effective against differential aging in each bit position as it cannot control each IDAC block individually, and the transfer ratio remains unchanged even if I_{bias} is adjusted.

We propose a scheme to recalibrate the tap-coefficients of an equalizer after aging that uses lone-pulse equalization technique. Our proposed modification to the FFE architecture is shown in Figure 5(b). We add a coefficient adapter (CA) unit on the Rx side that maps coefficients $\mathbf{C}$ to $\mathbf{C}'$ before transmitting them to the CUM, which stores and applies the tap coefficients as inputs to the IDACs of FFE at the Tx side (Fig. 3). The CA sits on the Rx side in order to incorporate the impact of the channel.

A key observation is that this recalibration is performed very seldom, while the equalizer is on during the entire operation of the circuit. Therefore, recalibrating circuitry can be assumed to be unaffected by aging shifts. The updated coefficients in $\mathbf{C}'$ are determined in four steps as follows:

Step 1: A pulse of amplitude V^{Tx}_{max} at the operating frequency is propagated through the channel. The detected amplitude of the received signal is denoted as V^{Rx}_{max}. Since the transmitted pulse drives the same load, R_{load}, on the Tx side, the current through the R_{load} is I_{tot}, i.e.,

$$V^{Tx}_{max} = I_{tot} \cdot R_{load} \tag{37}$$

Step 2: The Tx side sends a set of one-hot-encoded input signals for each FFE tap, also at the operating frequency. For each tap τ, each input bit in ξ^{τ} is set to 1 in turn; all other tap coefficients are set to 0. On the Rx side, the amplitude of the response to each signal is recorded. We denote the amplitude for the i^{th} bit of the binary-weighted IDAC of tap τ at the Tx and Rx side as $\mathcal{V}^{Tx}_{b,i,\tau} = I^{\tau}_{b,i} R_{load}$ and $\mathcal{V}^{Rx}_{b,i,\tau}$, respectively. Similarly, we denote the amplitude for i^{th} bit of unary IDAC of tap τ at the Tx and Rx side as $\mathcal{V}^{Tx}_{t,i,\tau} = I^{\tau}_{t,i} R_{load}$ and $\mathcal{V}^{Rx}_{t,i,\tau}$, respectively.

Step 3: Using the pulse response amplitudes in Steps 1 and 2, sampled at the Rx side, the CA calculates $I^{\tau}_{b,i}$ for the i^{th} bit of the binary-weighted IDAC of tap τ. Since the channel is a linear system, the ratio of the transmitted signal to the response for a fixed pulse shape is identical. Combining this observation with Eq. (37),

$$\frac{\mathcal{V}^{Tx}_{max}}{\mathcal{V}^{Rx}_{max}} = \frac{\mathcal{V}^{Tx}_{b,i,\tau}}{\mathcal{V}^{Rx}_{b,i,\tau}} \implies \frac{\mathcal{V}^{Rx}_{b,i,\tau}}{\mathcal{V}^{Rx}_{max}} = \frac{\mathcal{V}^{Tx}_{b,i,\tau}}{\mathcal{V}^{Tx}_{max}} = \frac{(I^{\tau}_{b,i} \cdot R_{load})}{(I_{tot} \cdot R_{load})}$$

$$\text{i.e., } I^{\tau}_{b,i} = \left(\mathcal{V}^{Rx}_{b,i,\tau} / \mathcal{V}^{Rx}_{max}\right) \cdot I_{tot} \tag{38}$$

Similarly, the CA calculates $I^{\tau}_{t,i}$ for the i^{th} bit of the unary IDAC of tap τ.

Step 4: For each tap τ, the current corresponding to the i^{th} bit flows through transistor M^{τ}_{i} in Fig. 2. From (3), the output current of tap τ under the aged coefficient vector $\mathbf{C}'$ is:

$$\begin{aligned} I^{\tau}_{out} &= \left[\textstyle\sum_{i=0}^{N-1} \xi^{\tau}_{b,i} \cdot \mathcal{R}'_{b,i} + \sum_{i=0}^{2^{(N-P)}-2} \xi^{\tau}_{t,i} \cdot \mathcal{R}'_{t,i}\right] \cdot I_{bias} \\ &= \textstyle\sum_{i=0}^{N-1} \xi^{\tau}_{b,i} \cdot I^{\tau}_{b,i} + \sum_{i=0}^{2^{(N-P)}-2} \xi^{\tau}_{t,i} \cdot I^{\tau}_{t,i} \end{aligned} \tag{39}$$

The CA then calculates the required weights for equalization. The required current, I^{τ}_{out} for each tap τ is determined by the CG module as described in Sec. 5.1. The pseudocode for this purpose is shown in Algorithm 1 and is easily implemented in the CA at the Rx end for dynamic adaptation.

Adaptive equalization: In comparison to the lone-pulse equalization scheme, the adaptive equalization scheme can automatically tune the tap coefficients to mitigate impact of IDAC aging in an FFE as long as the IDACs show monotonic behavior. However, as explained in Sec. 3.3, a segmented IDAC is susceptible to aging-induced nonmonotonicity due to the partially implemented binary-weighted IDAC architecture. To counter aging in an adaptive equalization scheme, we propose a three step process for selection of P for the IDACs of FFE that will make them robust to aging-induced nonmonotonicity in its lifetime. The steps are:

Step 1: In this step, the worst-case ΔG for each IDAC of the FFE is estimated. To optimize the IDAC sizes in the

FFE, a designer has to estimate the range and distribution of tap-coefficients, $\mathbf{C}$, considering the channel's frequency response, data rate, and environmental conditions. The distribution of $\mathbf{C}$ controls the activity factor, β_1, of each transistor and can be leveraged to estimate worst-case ΔG of an IDAC using Eqs. (19)–(26).

Step 2: ΔG is set to zero through the recalibration scheme considered for the design. In this paper, we consider two-point calibration scheme that sets ΔG to zero by adjusting I_{in} of an IDAC to I'_{in} as described in Appendix B.

Step 3: For each IDAC, minimum DNL_c, DNL^{min}, is estimated for all possible P with Eq. (27), where, $0 \leq P \leq N-1$. Using the DNL^{min} in the range of P, select the largest P with $\text{DNL}^{min} < -1$ for the segmented IDAC implementation to optimize the IDAC structure as well as to avoid aging-induced nonmonotonic behavior in its lifetime.

7. Results

We apply our models to the IDACs and the FFE and illustrate the impact of aging on performance. We also demonstrate how our mitigation strategy can be used to ensure correct FFE behavior over its lifetime. Our results are based on simulations on a commercial 12nm FinFET technology, incorporating device-level aging models from Section 3 into HSPICE.

7.1. IDAC Analysis

Aging-induced ΔV_{th} in the FinFET, $M_{i,j}$, of a current mirror (CM) depends on its activity factor, β_1. Fig. 6(a) compares the ΔV_{th} of M_{ref} and $M_{i,j}$ of a CM over a sweep of β_1 at an operating temperature, T, of 105^oC with $\beta_2 = 1$, i.e., the CM is always active. Transistor aging will add a V_{th} mismatch of 2.75% to 6.99% between M_{ref} and $M_{i,j}$ with respect to $V_{th,\mu}$ in 10 years depending on β_1. The mismatch induces an increase in the transfer ratio, $\Delta\mathcal{R}_{i,j}/\mathcal{R}_{i,j}$, of $M_{i,j}$ over time, as shown in Fig. 6(b) over a sweep of β_1: aging can cause upto 24% increase in the transfer ratio of $M_{i,j}$. The mismatch and transfer ratio shift are lowest for the CM in the current-steering DAC ($\beta_1 = 1$). In addition, all FinFETs in M_i of a current-steering DAC suffer identical ΔV_{th} and ΔR as the stress condition is identical for these FinFETs causing them to age at the same rate. This helps to reset INL and DNL of a current-steering DAC to zero with gain calibration (Appendix B). On the other hand, each FinFET can have different ΔV_{th} and ΔR ($0 \leq \beta_1 \leq 1$) in a current-switching DAC. As a consequence, gain calibration only scales nonlinearities in a current-switching DAC, as we illustrate later in this section. Therefore, *the current-steering configuration is more aging-resilient than the current-switching configuration.* Note that the conclusion regarding the current-steering DAC can be arrived at using manual analysis, and serves as a sanity-check for our method; the quantification for the current-switching DAC is nontrivial and cannot be determined through manual analysis.

In FinFET technology, gate-length can be increased by connecting transistors in series and keeping the same gate connection for those transistors. Fig. 6(c) highlights the impact of gate-length on $\Delta\mathcal{R}_{i,j}$. Aging-induced mismatch and the change in transfer ratio can be reduced by using higher gate-length: a gate length of $5L_0$, instead of L_0, reduces $\Delta\mathcal{R}_{i,j}$ by 45.45%. Hence, *IDACs with transistors of higher gate length are more robust to aging-induced mismatch.* As before, this qualitative conclusion is consistent with manual analysis, but a quantification of the robustness requires our approach.

As explained in Sec. 3, transistor aging will degrade the performance parameters of IDAC. Along with the encoding scheme and implementation topology, the extent of degradation of an IDAC depends on the distribution of the input code that can vary based on the application: for a given channel, IDACs of an FFE that supports a single data rate [27] [28] will have less variations in its tap-coefficients compared to an FFE that supports a band of data rate [29]. In our analyses:

- to illustrate and compare the impact of aging over different implementation topologies, we consider 6-bit IDAC architecture ($N = 6$).
- to analyze the impact of the encoding scheme and position of segmentation in an IDAC implementation, we sweep P. As explained in Sec. 2, the value of P in a segmented IDAC defines the least bit position handled by unary IDAC. For $P = 0$ and $P = N$, the IDAC acts as a unary and a binary-weighted IDAC, respectively. In principle, an IDAC with $P = N - 1$, a segmented IDAC with only one-bit for unary IDAC, has no difference from N-bit binary IDAC. Hence, we illustrate the performance comparison with respect to P in the range of 0 to $N - 1$.
- to analyze the impact of input code distribution on IDAC performance degradation, we consider three classes of input:

(i) unvarying: the input does not vary over time,
(ii) binomially distributed: the input varies around itself following a binomial distribution,
(iii) uniformly distributed: all possible inputs in its range are equiprobable.

Gain: A shift in gain indicates expansion or diminution of I_{out} range of the IDAC causing it to deviate from the ideal behavior. As explained in Sec. 3, M_{ref} of a current mirror (CM) always ages at a higher rate than $M_{i,j}$ in an active IDAC. Hence, $\Delta\mathcal{R}_{i,j}$ always increases over time (Eq. (21)) causing the gain, G, of an IDAC to increase (Eq. (26)). As $M_{i,j}$ in current-steering configuration always goes through maximum stress, aging induces minimum mismatch between M_{ref} and $M_{i,j}$, as explained above, causing minimum gain shift over time irrespective of the input distribution.

For unvarying input, the cumulative mismatch of an IDAC will be highest and lowest if all M_i in IDAC are always in-

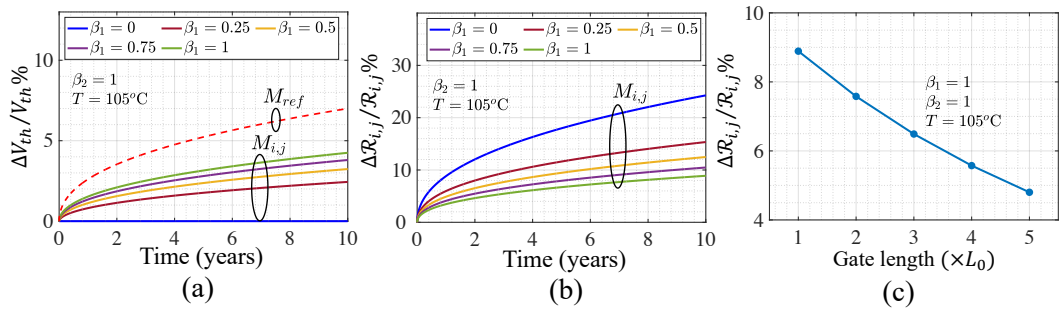

Fig. 6. (a) V_{th} degradation of M_{ref} and $M_{i,j}$ due to aging with varying β_1. (b) Change in transfer ratio of $M_{i,j}$ due to aging with varying β_1. (c) Change in transfer ratio of $M_{i,j}$ with varying gate length, L.

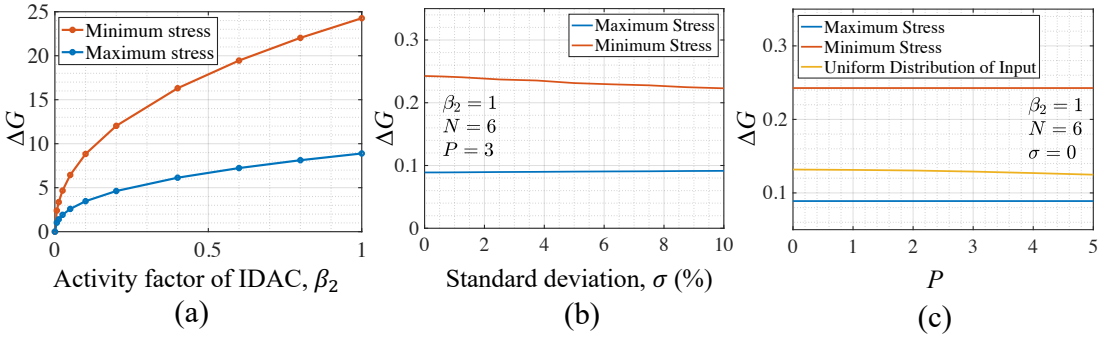

Fig. 7. ΔG for: (a) unvarying input with varying β_2, (b) binomially distributed input with varying σ, (c) uniformly and binomially distributed input with varying P.

active and active, respectively, irrespective of P. For an 6-bit current-switching DAC, in 10 years of continuous aging, ΔG can drift by 8.89% (maximum stress: $c_i = 1 \forall 0 \leq i < N$) to 24.26% (minimum stress: $c_i = 0 \forall 0 \leq i < N$), as shown in Fig. 7(a). As all transistors in CM of a current-steering DAC are always active, *the cumulative mismatch in transistors of a current-steering DAC is the lowest.*

For a binomially distributed input, our analysis in Fig. 7(b) shows that the maximum (minimum) ΔG decreases (increases) by 8.08% (2.92%) if the standard deviation, σ, around an input increases from zero to 10% of all possible inputs as a distribution around an input reduces minimum and maximum stress possible, compared to unvarying input, over the transistors of the current mirror. The maximum and minimum ΔG show negligible sensitivity to P as shown in Fig. 7(c).

For uniformly distributed input, our study shows that ΔG *endures larger shift with a larger unary IDAC segment* (Fig. 7(c)). This happens due to the nonuniform aging of transistors in unary IDAC. In binary-weighted IDAC segment, an uniform distribution of input causes the activity factor, β_1, of all transistors to be 0.5 irrespective of P. On the other hand, an uniformly distributed input causes β_1 of transistor $M_{i,j}$ in unary IDAC to decrease linearly as i increases. Hence, a smaller P causes a larger difference in aging between the $i = 0$ and $i = 2^{(N-P)} - 2$ of unary IDAC segment resulting in a larger ΔG.

In modern chips, ΔG can be recalibrated to zero in IDACs by varying I_{in}. All FinFETs M_i of the CM block age at the same rate in a current-steering DAC as mentioned previously. This causes the transfer ratio of all FinFETs to remain identical, so that calibration through scaling I_{in} to I'_{in} minimizes DNL and INL, explained in Appendix B. However, in a current-switching DAC, FinFETs in the CM block can age at different rate depending on the inputs and its architecture. Consequently, recalibrating ΔG to zero by varying I_{in} may only re-scale the DNL and INL of a current-switching DAC. Hence, we illustrate the impact of aging on INL and DNL over a segmented IDAC with a current-switching configuration only, considering a two-point calibration scheme [30] that sets $\Delta G = 0$ at any given time, through compensating for the errors at minimum and maximum value of c.

INL: INL at an input c, INL_c, of a DAC denotes the deviation of actual output from expected output at c: an increase of $|\text{INL}_c|$ indicates a decrease in precision of a DAC at c. To maintain the expected resolution of a data converter, $|\text{INL}_c|$ is expected to be $\leq \frac{1}{2}$LSB.

Aging-induced INL in a segmented IDAC with a current-switching configuration depends on the difference of β_1 among the FinFETs, $M_{i,j}$, of a current mirror (CM). A smaller difference of β_1 will cause a smaller difference in mismatch, $\Delta[M_{ref}, M_{i,j}]$, and in $\Delta\mathcal{R}'_{i,j}$ as a consequence. Through the two-point calibration scheme (Appendix B), the current through the FinFETs are scaled uniformly by tuning I_{in} to I'_{in} that reduces INL_c. However, such cali-

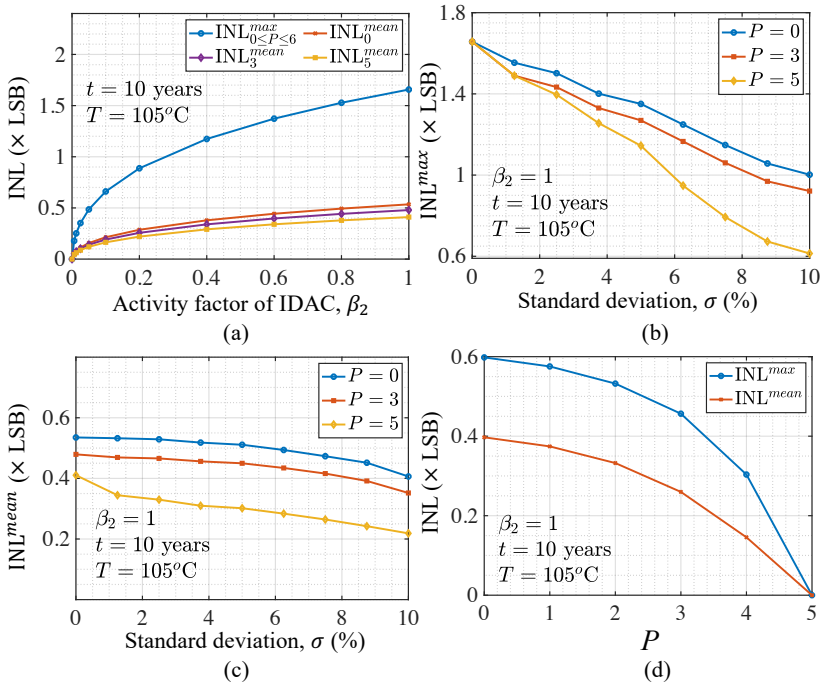

Fig. 8. Comparisons of INL^{max} and INL^{mean} in a segmented DAC with the current-switching topology: (a) unvarying input with varying β_2, (b)–(c) binomially distributed input with varying σ, (d) uniformly distributed input.

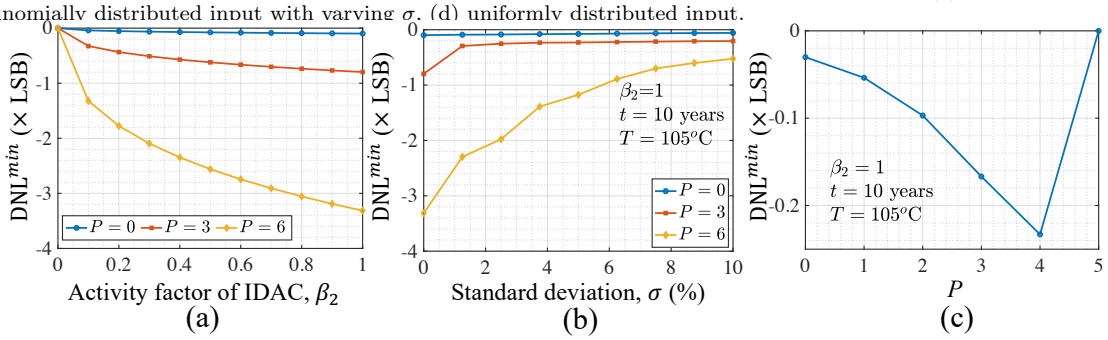

Fig. 9. DNL^{min}(×LSB) comparison of a segmented DAC with the current-switching topology: (a) unvarying input with varying β_2, (b) binomially distributed input with varying σ, (c) uniformly distributed input.

bration only scales down INL_c and has no impact on relative differences among INL_c caused by aging, which only depend on relative differences among β_1 of the FinFETs. To illustrate the aging-induced INL degradation of an IDAC in a lifetime of 10 years, we consider two parameters: maximum $|\text{INL}_c|$, INL^{max}, representing worst case INL and mean $|\text{INL}_c|$, INL^{mean}, representing average INL for all possible inputs.

Unvarying input ages a subset of all FinFETs of the current mirror (CM) only: β_1 is one (zero) if c_i is one (zero). This causes a large induction of INL_{max}, 1.7×LSB, in a 6-bit DAC in 10 years (Fig. 8(a)) if the IDAC is always active, i.e., $\beta_2 = 1$. INL^{max} *does not depend on* P *of a segmented IDAC for unvarying input* as it causes aging in the same number of FinFETs, $M_{i,j}$, irrespective of segmentation, e.g., an unvarying input $c = 33$ will stress 33 FinFETs irrespective of the P of a segmented IDAC. However, this is not the case for INL^{mean} as it also depends on the configuration of the IDAC. Our analysis shows that INL^{mean} decreases if P increases: *a larger unary IDAC in a segmented IDAC causes a larger* INL^{mean}. Fig. 8(a) shows INL^{max} and INL^{mean} with respect to the activity factor of IDAC, β_2, where β_1 of each FinFET is determined by c: INL^{mean} increases at a slower rate than INL^{max} and decreases with an increasing P.

For a binomial distribution of the input, Figs. 8(b) and (c) show INL^{max} and INL^{mean} with a sweep over standard deviation, σ, of the input. *Difference of* β_1 *among the FinFETs,* $M_{i,j}$*, is smaller in a distributed input compared to an unvarying input causing a smaller* INL^{max} *and* INL^{mean} *with a larger* σ. For a given σ, difference in β_1 of FinFETs are smaller among the FinFETs in binary-weighted IDAC than unary IDAC causing it to drop at a higher rate. This causes an smaller INL^{max} and INL^{mean} for $P = 5$ compared to $P = 0$.

For uniformly distributed input, INL^{max} and INL^{mean} both decrease as P increases and become zero at $P = 5$, as shown in Fig. 8(d). An uniform distribution of inputs will

set $\beta_1 = 0.5$ for all FinFETs $M_{i,j}$ of the binary-weighted IDAC segment that causes uniform shift of $\Delta R'_{i,j} \forall M_{i,j}$ in the segment. At $P = 5$, the segmented IDAC acts as binary-weighted IDAC, hence, transfer ratio of all FinFETs in the segmented IDAC will shift by the same amount causing INL_c to increase with c at an uniform rate. Hence, calibrating ΔG to zero also sets all INL_c to zero. On the other hand, in unary IDAC segment, β_1 will linearly reduce as bit position i moves from LSB to MSB causing nonuniform $\Delta R'_{i,j}$ among the FinFETs. As a consequence, unary IDAC segment will have nonzero INL_c for $0 < c < 2^{(N-P)} - 2$ even after gain calibration. A smaller unary IDAC, larger P, will have a smaller β_1 differential between the FinFETs at $i = 0$ and $i = 2^{(N-P)} - 2$ causing INL^{max} and INL^{mean} to decrease with P.

The above analyses indicate that *a binary-weighted IDAC is more robust to aging-induced INL than a unary IDAC.* Hence, the IDAC applications that require high precision over time should consider keeping a larger P for a segmented IDAC design.

DNL: DNL at an input c, DNL_c, indicates the deviation of step size for the input c from ideal step size. A positive (negative) DNL_c indicates the step size at c is larger (smaller) than 1×LSB. Like INL, aging-induced DNL also depends on the difference of β_1 among the FinFETs: a larger difference in β_1 will cause a larger DNL.

For an adaptive equalization scheme, it is critically important that a DAC shows monotonic behavior: the analog output always increases with the digital input. A DAC is monotonic if $\text{DNL}_c \geq -1\times\text{LSB} \forall c$. Given an ideal segmented IDAC, aging can cause negative DNL and induce nonmonotonicity in the worst case. To demonstrate the impact of aging on DNL, we observe the minimum DNL_c for all possible inputs, DNL^{min}, in a lifetime of 10 years. For unvarying input, Fig. 9(a) shows shift of DNL^{min} with the activity factor of IDAC, β_2, for varying P. With increase in P, size of the binary weighted IDAC segments becomes larger that opens up the possibility of larger aging-induced DNL^{mean} in the segmented IDAC. At $P = 5$, *aging can cause nonmonotonicity* in the IDAC even if it is active for $< 10\%$ of its lifetime. This happens at the mid-scale, i.e., $c = 32$, as the input stresses the transistors controlled by MSB only creating significant difference in transfer ratio between $M_{i,j}$ of $i = 5$ and $0 \leq i < 5$.
For a binomial distribution of the input, DNL^{min} drops with increasing σ as difference in β_1 decreases among the FinFETs with an increase in distribution (Fig. 9(b)).
For uniformly distributed input, a larger unary IDAC in the segmented IDAC causes smaller DNL^{min} due to its robustness against DNL (Fig. 9(c)). However, minimum DNL^{min} happens at $P = N-1$: when the segmented IDAC acts completely as binary-weighted IDAC as an uniform input to binary-weighted IDAC sets β_1 of all transistor to 0.5 causing uniform $\Delta R'_{i,j}$. In such case, with calibration, DNL_c for all input also turns to zero.

To summarize the impact of aging on DNL of an ideal N-bit segmented IDAC at $t = 0$: aging will induce DNL over time and the amount of DNL^{min} introduced in the IDAC will depend on P. Unless all FinFETs suffer uniform $\Delta R'_{i,j}$, which is only possible if $P \geq N - 1$ and input is uniformly distributed, gain calibration cannot DNL^{min} to zero and fix aging-induced nonmonotonicity.

7.2. FFE Analysis

In this subsection, we illustrate the impact of aging on different coefficient selection schemes of FFE, described in Sec. 5.1. For this purpose, we consider a 5-to-15 Gb/s NRZ FFE transmitter with a precursor, a main cursor, and a postcursor operating on a channel modeled as a 12" desktop backplane [31]. The tap adaptation ranges of precursor, main cursor, and the postcursor are 16, 64, and 32, respectively (i.e., the coefficients have 4, 6, and 5 bits, respectively). We consider a segmented IDAC for the tap associated with the main cursor and binary-weighted IDAC for the rests. All IDACs are implemented with a current-switching topology.

Fig. 10 illustrates the types of nonideality that can be induced by aging in the IDACs of the FFE in its lifetime of 10 years: aging can cause (a) nonuniform gain among the IDACs of FFE caused by nonuniform aging of IDACs due to the differences in tap-coefficients (Eq. (35)), (b) nonideal INL and DNL, and (c) nonmonotonicity at the worst case due to the nonuniform aging of transistors in the current mirror. These nonidealities degrade the equalization quality of an FFE through shifting effective equalization over time. Fig. 11(a) shows the shifting of weight vector $\text{W}'(t)$ over time due to aging if the FFE operates at 15 GHz frequency. The tap-coefficients are determined using lone-pulse equalization technique (Sec.5.1) and set to $\mathbf{C} = [10, 37, 16]$ at $t = 0$. We also consider that tap-coefficients varies following a binomial distribution with a standard deviation, σ, of 2.5%. Our analysis shows that the weight corresponding to the precursor, main cursor ($P = 6$), and post cursor shift $-1.2\%, -3.17\%, +4.43\%$, respectively, in 10 years. Fig. 11(b) displays the shift of weight associated with main cursor with the position of segmentation, P. Although, increasing P reduces INL^{max} and INL^{mean} (Fig. 8(b)–(c)), the reduction is not significant: at $\sigma = 2.5\%$, INL^{max} and INL^{mean} only decrease around 0.2×LSB if P shifts from zero to five. Hence, effective equalization shows negligible change (0.32%) in the range of P of main cursor. Table 1 compares the horizontal and vertical eye widths at $t = 0$ and $t = 10$ years if the coefficients are set using lone-pulse equalization process: aging degrades horizontal and vertical eye width by 24.49% and 40%, respectively, in 10 years. Fig. 11(c) and (d) show the eye diagram at the receiver end of the equalized data at $t = 0$ and $t = 10$ years, respectively.

Tap-coefficients generated by the lone-pulse equalization scheme depend on the pulse response received at the receiver. Therefore, the scheme will generate the same vector of tap-coefficients, $\mathbf{C}$, if the operating conditions

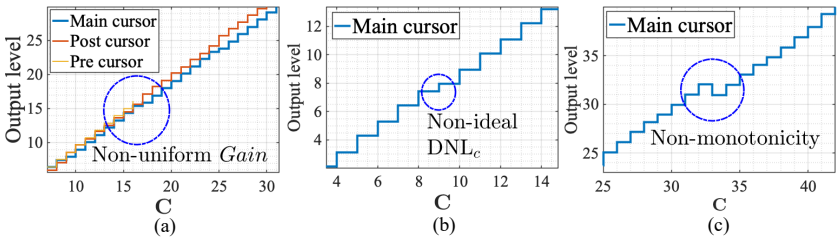

Fig. 10. Segments of the transfer curves that illustrate (a) nonidealities in Gain G, (b) nonidealities in DNL, and (c) nonmonotonicity in an FFE with current-switching DACs.

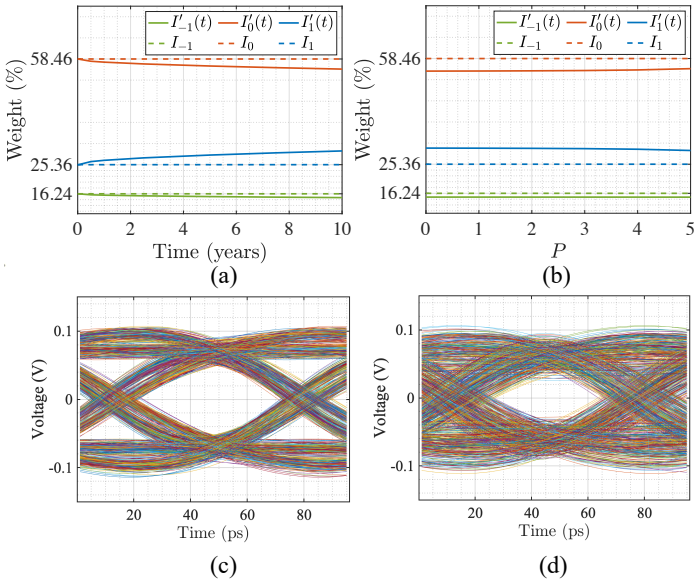

Fig. 11. For a 6-bit segmented DAC with the current-switching topology: (a) change in effective equalization over time, (b) change in effective equalization over P of main cursor, (c) eye diagram at $t = 0$, (d) eye diagram at $t = 10$ years (degraded due to the change in effective equalization).

remain unchanged. However, as shown in Fig. 11, effective equalization will degrade over time, shrinking the eye diagram at the receiver end. To counter this aging effect, we proposed an addition of coefficient adapter (CA) module at the receiver in Sec. 6 that considers IDACs aging in an FFE and adjusts the tap-coefficients generated by the CG, $\mathbf{C} = [10, 37, 16]$, to a new set of tap-coefficients, $\mathbf{C}' = [11, 39, 13]$, to match expected equalization as shown in Fig. 12(a). Fig. 12(b) shows the eye diagram at $t = 10$ years with CA: the eye to be as wide as the unaged circuit. The horizontal and vertical eye widths at $t = 10$ years with CA module are included in Table 1. The bathtub curve of (Fig. 12(c)) shows that after calibration, the BER improves back to the $t = 0$ level.

Table 1: Eye diagram comparisons of data at the receiver end at 15 GHz operating frequency with lone-pulse equalization

Eye diagram widths	$t = 0$ years	$t = 10$ years, without CA	$t = 10$ years, with CA
Horizontal (ns)	49	37	49
Vertical (V)	0.10	0.06	0.10

An FFE with an adaptive equalization scheme will automatically readjust the coefficient from $\mathbf{C}$ to $\mathbf{C}'$ if effective equalization changes due to aging, unless aging causes nonmonotonicity in any of the IDACs of FFE. However, as we proposed in Sec. 6, induction of nonmonotonicity can be avoided with proper selection of P of a segmented IDAC. To demonstrate this, we consider the FFE operation at a 5 GHz frequency that requires $\mathbf{C}$ to be at $[2, 51, 10]$ for optimum equalization of transmitting data. Fig. 13(a) shows how DNL^{min} of the main cursor changes with P. Aging due to the tap-coefficients for optimal equalization at 5 GHz can induce nonmonotonicity in IDAC associated with the main cursor in the lifetime of FFE if $P \geq 4$. Fig. 13(b) shows the dynamic of DNL^{min} shift over the lifetime of FFE. At $P = 4$, nonmonotonicity can be induced in the IDAC at around five years. Fig. 13(c) shows DNL$_c$ at each input c of the main cursor at $t = 5$ years. Operating at 5 GHz can causes nonmonotonicity at $c = \{16, 32, 48\}$. As explained in Sec. 5.1, tap-coefficients are initially set to minimum or maximum value in the adaptive equalization process. With aging-induced nonmonotoncity at $c = \{16, 32, 48\}$, the adaptive equalization process will fail

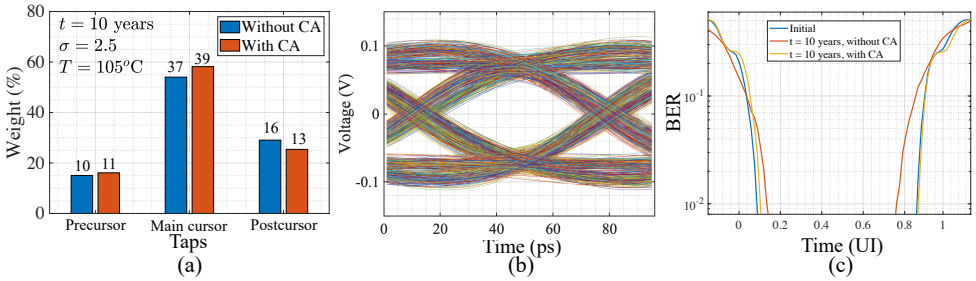

Fig. 12. (a) Comparison of effective equalization of FFE (IDACs in a current-switching configuration) with and without CA module (Fig. 3) after 10 years (respective tap-coefficients are shown at the top of each bar), (b) recovered eye diagram of Fig. 11(b) after coefficient adjustment by CA module, (c) BER comparison.

to reach optimal tap-coefficient for the main cursor if operating frequency changes after five years and the optimal tap-coefficient of the main cursor lies in the range of 17 to 47, e.g., if the operating frequency switches to 15 GHz, adaptive equalization may fail to reach optimal coefficient required for the main cursor. This scenario can easily be avoided if P of the main cursor is set to three, as this will not induce any nonmonotonicity in the lifetime of FFE. Table 2 compares the horizontal and vertical eye widths at $t = \{0, 5\}$ years with $P = \{3, 4\}$ at 15 GHz operating frequency considering the FFE operated at 5 GHz frequency continuously for five years.

8. Conclusion

The paper has presented a modeling study of the impact of mismatch in IDACs, and has demonstrated its application in the analysis of an FFE. Two novel schemes, one for each of two coefficient selection process for the FFE, are presented to counter the impact of IDAC aging. These schemes are shown to be effective against aging-induced FFE performance degradation. Since an IDAC is a commonly used building block in a number of larger circuits and systems, our IDAC aging analysis methodology can potentially be applied to a variety of other applications.

Appendix

A. Proofs of FFE Degradation Results

Impact of Mismatch on Circuit Voltages We first analyze the impact of aging-induced mismatch on IDAC performance. For a FinFET $M_{i,j}$, we denote the shift in threshold voltage due to time-dependent aging as $\Delta V_{th,M_{i,j}}$; similarly we define $\Delta V_{th,M_{ref}}$ for the reference transistor, M_{ref}. Thus, for any transistor M_x,

$$\Delta V_{th,M_x} = V_{th,M_x} - V_{th,\mu} \tag{40}$$

where $V_{th,\mu}$ was defined earlier as the nominal threshold voltage. For a fixed I_{in}, as the diode-connected M_{ref} is in saturation, any change in V_{th} results in an equal rise in V_b:

$$V_{GS,M_{ref}} = V_{DS,M_{ref}} = V_b + \Delta V_{th,M_{ref}} \tag{41}$$

Combining this with Eq. (40), we have:

$$V_{GS,M_{ref}} - V_{th,M_{ref}} = V_b - V_{th,\mu} \tag{42}$$

For all FinFETs of an ON transistor M_i (with $c_i = 1$),

$$V_{GS,M_{i,j}} = V_{GS,M_{ref}} \text{ and } V_{DS,M_{i,j}} = V_d \tag{43}$$

The latter relation arises because these FinFETs operate in the linear region, and V_{th} shift has a negligible effect on the drain voltage. From Eqs. (40), (41), and (43),

$$\begin{aligned} V_{GS,M_{i,j}} - V_{th,M_{i,j}} &= (V_b + \Delta V_{th,M_{ref}}) - (V_{th,\mu} + \Delta V_{th,M_{i,j}}) \\ &= (V_b - V_{th,\mu}) + \Delta[M_{ref}, M_{i,j}] \end{aligned} \tag{44}$$

where $\Delta[M_{ref}, M_{i,j}]$ is the V_{th} mismatch, as defined earlier.

Building upon the above ideas, we now present proofs of the results shown in Section 3.2.

FinFET transfer ratio: When the FinFETs age nonuniformly, we combine Eqs. (8), (41), (42), (43), and (44), to obtain the the transfer ratio for FinFET $M_{i,j}$ as:

$$\mathcal{R}'_{i,j} = \left[1 + \frac{\Delta[M_{ref}, M_{i,j}]}{(V_b - V_{th,\mu})}\right]^{\alpha} \left[\frac{1 + \lambda V_d}{1 + \lambda(V_b + \Delta V_{th,M_{ref}})}\right]$$

Rearranging this and, for small perturbations, using a Taylor series approximation for the first term,

$$\mathcal{R}'_{i,j} = (1 + \alpha K_1 \Delta[M_{ref}, M_{i,j}]) \left[\frac{r}{1 + K_2 \Delta V_{th,M_{ref}}}\right] \tag{45}$$

$$\approx r\,(1 + \alpha K_1 \Delta[M_{ref}, M_{i,j}]) \tag{46}$$

Table 2: Eye diagram comparisons of data at the receiver end at 15 GHz operating frequency with adaptive equalization if the FFE initially operates at 5 GHz for five years

Eye diagram widths	$t = 0$ years	$t = 5$ years, with $P = 4$	$t = 5$ years, with $P = 3$
Horizontal (ns)	49	33	49
Vertical (V)	0.10	0.05	0.10

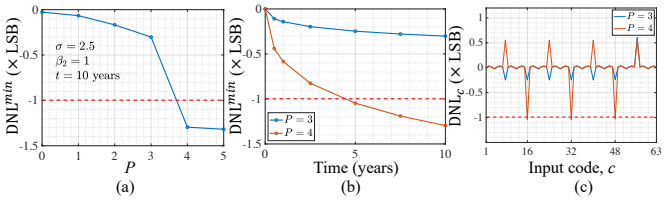

Fig. 13. (a) DNL^{min}, in LSB, after $t = 10$ years with P of a segmented DAC with the current-switching topology associated with the main cursor of FFE, (b) change of DNL^{min} over the lifetime of FFE, (c) comparison of DNL_c at $t = 5$ years for $P = \{3, 4\}$.

Here, r is as defined in Eq. (9), $K_1 = 1/(V_b - V_{th,\mu})$, $K_2 = \lambda/(1 + \lambda V_b)$, The last approximation arises by setting $r' = r/(1 + K_2 \Delta V_{th,M_{ref}}) \approx r$ because both K_2 and $\Delta V_{th,M_{ref}}$ are small. For a representative technology, $\lambda \approx 0.3$, $V_{th,\mu} \approx 0.35$, $V_b - V_{th}$ is 100mV$\sim$200mV, $\Delta V_{th} \sim$ 100mV. Thus, $K_2 \Delta V_{th,M_{ref}} \sim 0.029 \ll 1$.

From Eq. (9), $\Delta\mathcal{R}'_{i,j} = \alpha K_1 r \Delta[M_{ref}, M_{i,j}]$.

Transfer ratio i-th transistor: For the P-bit binary-weighted IDAC ($0 \le i < P$):

$$\begin{aligned}\mathcal{R}'_{b,i} &= \textstyle\sum_{j=0}^{2^i-1} \mathcal{R}'_{ij} = r \sum_{j=0}^{2^i-1} (1 + \alpha K_1 \Delta[M_{ref}, M_{i,j}]) \\ &= 2^i \cdot r + \alpha K_1 r \textstyle\sum_{j=0}^{2^i-1} \Delta[M_{ref}, M_{i,j}] \end{aligned} \tag{47}$$

For the $(N-P)$-bit unary IDAC ($0 \le i < 2^{(N-P)}-1$), each bit controls 2^P transistors irrespective of the bit position i. Hence, for unary IDAC:

$$\begin{aligned}\mathcal{R}'_{t,i} &= \textstyle\sum_{j=0}^{2^P-1} \mathcal{R}'_{ij} = r \sum_{j=0}^{2^P-1} (1 + \alpha K_1 \Delta[M_{ref}, M_{i,j}]) \\ &= 2^P \cdot r + \alpha K_1 r \textstyle\sum_{j=0}^{2^P-1} \Delta[M_{ref}, M_{i,j}] \end{aligned} \tag{48}$$

From Eqs. (10), (11), (47), and (48), we can get Eq. (22) and (23) for the N-bit segmented IDAC.

Finding I_{out}: From Eq. (1), for P-bit binary-weighted IDAC,

$$I'_{out} = I_{in} \textstyle\sum_{i=0}^{P-1} c_{b,i} \mathcal{R}'_{b,i} \tag{49}$$

Together with Eq. (4), (22), and (47), I'_{out} for the binary-weighted IDAC:

$$\begin{aligned}&I_{in} \textstyle\sum_{i=0}^{P-1} c_{b,i} \cdot \left(2^i \cdot r + \alpha K_1 r \sum_{j=0}^{2^i-1} \Delta[M_{ref}, M_{i,j}]\right) \\ &= I_{in} \left(c_b \cdot r + \alpha K_1 r \textstyle\sum_{i=0}^{P-1} c_{b,i} \sum_{j=0}^{2^i-1} \Delta[M_{ref}, M_{i,j}]\right) \\ &= I_{in} \left(c_b \cdot r + \textstyle\sum_{i=0}^{P-1} c_{b,i} \Delta\mathcal{R}'_{b,i}\right) \end{aligned} \tag{50}$$

Similarly, I'_{out} for $(N-P)$-bit unary IDAC:

$$I_{in} \left(c_t \cdot r + \textstyle\sum_{i=0}^{2^{(N-P)}-2} c_{t,i} \Delta\mathcal{R}'_{t,i}\right) \tag{51}$$

Combine Eqs. (13), (50), and (51) to get Eq. (25).

Gain: For the N-bit segmented IDAC, we set $c_{b,i} = 1 \; \forall \; i$ and $c_{t,i} = 1 \; \forall \; i$ in Eqs. (50) and (51), respectively, and add them to obtain the full-scale current after aging, I'_{FS}:

$$\begin{aligned}&I_{in} \left(c_b^{max} \cdot r + \textstyle\sum_{i=0}^{P-1} \Delta\mathcal{R}'_{b,i}\right) + \\ &I_{in} \left(c_t^{max} \cdot r + \textstyle\sum_{i=0}^{2^{(N-P)}-2} \Delta\mathcal{R}'_{t,i}\right) \\ &= I_{FS} + I_{in} \left(\textstyle\sum_{i=0}^{P-1} \Delta\mathcal{R}'_{b,i} + \sum_{i=0}^{2^{(N-P)}-2} \Delta\mathcal{R}'_{t,i}\right) \end{aligned} \tag{52}$$

where c_b^{max} and c_t^{max} represent maximum value of c_b and c_t, respectively, such that, $c^{max} = c_b^{max} + c_t^{max} = 2^N - 1$. Eq. (52) can be used to obtain gain of the N-bit segmented IDAC after aging:

$$G' = \frac{I'_{FS}}{c^{max}} = G + \frac{I_{in}}{2^N - 1} \left(\textstyle\sum_{i=0}^{P-1} \Delta\mathcal{R}'_{b,i} + \sum_{i=0}^{2^{(N-P)}-2} \Delta\mathcal{R}'_{t,i}\right) \tag{53}$$

From Eq. (53), we obtain Eq. (26).

DNL: Shift in the DNL for the segmented IDAC for an input c will depend on the cumulative shift of output current of the binary-weighted IDAC and unary IDAC when input moves to c from $(c-1)$.

$$\begin{aligned}\text{DNL}_c &= (I_c - I_{c-1}) - r \cdot I_{in} \\ &= [I_{c_b} - I_{(c-1)_b}] + [I_{c_t} - I_{(c-1)_t}] - r \cdot I_{in} \end{aligned} \tag{54}$$

Using Eq. (50) for the binary-weighted IDAC,

$$\begin{aligned}&I_{c_b} - I_{(c-1)_b} \\ &= I_{in} \left([c_b - (c-1)_b] \cdot r + \textstyle\sum_{i=0}^{P-1} [c_{b,i} - (c-1)_{b,i}] \Delta\mathcal{R}'_{b,i}\right) \end{aligned} \tag{55}$$

Similarly, for the unary IDAC,

$$\begin{aligned}&I_{c_t} - I_{(c-1)_t} \\ &= I_{in} \left([c_t - (c-1)_t] \cdot r + \textstyle\sum_{i=0}^{2^{(N-P)}-2} [c_{t,i} - (c-1)_{t,i}] \Delta\mathcal{R}'_{t,i}\right) \end{aligned} \tag{56}$$

For the N-bit segmented IDAC, step size in ideal case:

$$\begin{aligned}I_c - I_{c-1} &= I_{c_b} + I_{c_t} - \left[I_{(c-1)_b} + I_{(c-1)_t}\right] \\ &= I_{in} \cdot r \left([c_b + c_t] - [(c-1)_b + (c-1)_t]\right) \end{aligned} \tag{57}$$

As step size for the IDAC in ideal case is $r \cdot I_{in}$, from Eq. (57):

$$[c_b + c_t] - [(c-1)_b + (c-1)_t] = 1 \tag{58}$$

Combining Eqs. (3), (54), (55), (56), (57), and (58), we obtain:

$$\begin{aligned}\text{DNL}_c = I_{in} [&\textstyle\sum_{i=0}^{N-1} [c_{b,i} - (c-1)_{b,i}] \Delta\mathcal{R}'_{b,i} + \\ &\sum_{i=0}^{2^{(N-P)}-2} [c_{t,i} - (c-1)_{t,i}] \Delta\mathcal{R}'_{t,i}] \end{aligned}$$

INL: Using Eqs. (50) and (51), the output current from the segmented IDAC for an input c, I_c, can be calculated as:

$$\begin{aligned} & I_{in}\left[\left(c_b \cdot r + \sum_{i=0}^{P-1} c_{b,i}\Delta\mathcal{R}'_{b,i}\right) + \right. \\ & \qquad \left.\left(c_t \cdot r + \sum_{i=0}^{2^{(N-P)}-2} c_{t,i}\Delta\mathcal{R}'_{t,i}\right)\right] \\ & = I_{in}\left(c \cdot r + \sum_{i=0}^{P-1} c_{b,i}\Delta\mathcal{R}'_{b,i} + \sum_{i=0}^{2^{(N-P)}-2} c_{t,i}\Delta\mathcal{R}'_{t,i}\right) \end{aligned} \tag{59}$$

Following Eq. (59):

$$\mathrm{INL}_c = I_{in}\left(\sum_{i=0}^{P-1} c_{b,i}\Delta\mathcal{R}'_{b,i} + \sum_{i=0}^{2^{(N-P)}-2} c_{t,i}\Delta\mathcal{R}'_{t,i}\right)$$

B. Calibrating Gain of IDAC

Comparing Eq. (53) with (14), $G' > G$ as $\mathcal{R}'_i > \mathcal{R}_i$. In this case, ΔG, DNL_c, and INL_c can be calculated using Eq. (26), (27), and (28) respectively. To set $G' = G$, I_{in} can be calibrated to I'_{in} such that:

$$\sum_{i=0}^{N-1} I'_{in}\mathcal{R}'_i = \sum_{i=0}^{N-1} I_{in}\mathcal{R}_i \Longrightarrow \frac{I'_{in}}{I_{in}} = \frac{\sum_{i=0}^{N-1}\mathcal{R}_i}{\sum_{i=0}^{N-1}\mathcal{R}'_i} \tag{60}$$

For a current-steering DAC, all $M_{i,j}$ face identical stress condition: $V_{GS,M_{i,j}} = V_b$, and $V_{DS,M_{i,j}} = V_d$. This causes an identical mismatch, $\Delta[M_{ref}, M_{i,j}]$, hence identical $\mathcal{R}'_{i,j}$ as a consequence (Eq. 46) in all $M_{i,j} \forall 0 \leq i < N, 0 \leq j < 2^i$. From Eq. (60), G' can be set to G in a current-steering DAC by recalibrating I'_{in} as following:

$$\frac{I'_{in}}{I_{in}} = \frac{(2^N-1)\cdot\mathcal{R}_{i,j}}{(2^N-1)\cdot\mathcal{R}'_{i,j}} \Longrightarrow I'_{in} = \frac{r \cdot I_{in}}{\mathcal{R}'_{i,j}} \tag{61}$$

After such recalibration in a current-steering DAC, DNL_c and INL_c for any c also go to zero:

$$\mathrm{DNL}_c = (I_c - I_{c-1}) - r \cdot I_{in} = \mathcal{R}'_{i,j}.I'_{in} - r \cdot I_{in} = 0$$
$$\mathrm{INL}_c = I_c - c \cdot r \cdot I_{in} = c \cdot \mathcal{R}'_{i,j}.I'_{in} - c \cdot r \cdot I_{in} = 0$$

In a current-switching DAC, stress condition of each M_i varies depending on c_i (Section 2). Hence, $\mathcal{R}'_{i,j}$ corresponding to each $M_i, 0 \leq i < N$ can be different. As a consequence, tuning I_{in} to I'_{in} to set $G' = G$ in a current-switching DAC may not set DNL_c and INL_c to zero for all c.

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