Circuit performance shifts due to layout-dependent stress in planar and 3D-ICs

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***Abstract*—This paper presents an approach for analyzing stress in 2D and 3D integrated circuits (ICs) due to post-manufacturing thermal mismatch. For both 2D-ICs and 3D-ICs, shallow trench isolation (STI) induces thermal residual stress in active silicon. For 3D-ICs, through-silicon vias (TSVs) act as additional source of stress. Together, the sources of stress cause changes in the delay and power of the circuit. We develop an analytical model based on inclusion theory in micromechanics to accurately estimate the stresses and strains induced in the active region by surrounding STI in a layout. The TSV-induced stress depends on the location of the transistor with respect to the TSVs. Therefore, these stresses result in placement-dependent variations in the transistor mobilities and threshold voltages of the active devices, and we propagate these effects to circuit-level performance. At the transistor level, the stress state is translated into mobility and threshold voltage variations using piezoresistivity and band deformation potential models, respectively. At the gate level, the computed changes in transistor electrical parameters are used to predict gate-level delay and leakage power changes for single and multi-fingered layout styles, which are subsequently used to predict circuit-level delay and leakage power for a given placement.**

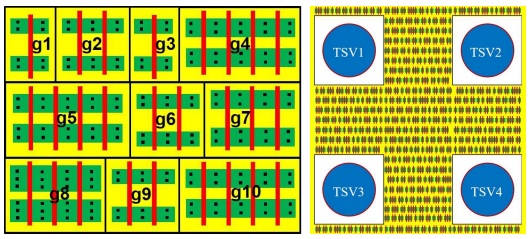
***Key Terms* : Shallow Trench Isolation, 3D-IC, Static Timing Analysis, Finite Element Method**

I. Introduction

Layout-dependent stress effects are an important consideration in both two-dimensional (2D) and three-dimensional (3D) integrated circuits (ICs). In planar 2D transistor technologies, an SiO_2 region, referred to as shallow trench isolation (STI), is employed to electrically isolate active transistors in the layout. In typical process technologies, a layer of STI is grown on a much larger substrate after trench formation, near the surface where transistors are manufactured. Figure 1(a) shows the 2D view of STI in a representative layout. STI is embedded in silicon at a high temperature of 1000°C, but post manufacturing, at circuit operating temperatures, a residual thermal stress is incorporated into silicon due to the coefficient of thermal expansion (CTE) mismatch between SiO_2 and silicon. As shown in [1], the PMOS (NMOS) delay of a CMOS inverter varies by about 25%, depending on the STI environment. In 3D ICs, where one or more die are stacked vertically, STI-induced stress is experienced in each stacked layer, but in addition, another source of stress is related to the through-silicon vias (TSVs) used for vertical interconnects. TSVs are made up of copper and are typically surrounded by a thin dielectric liner layer to improve mechanical reliability. TSVs are manufactured at a temperature of 250°C, and owing to the relatively higher CTE mismatch between copper and silicon, a residual thermal stress is developed in silicon at the much lower operating temperatures. Tungsten can be used as an alternate TSV material to copper due to similar CTE with respect to silicon; this results in smaller magnitude of stress and hence in silicon. However, tungsten suffers from high resistivity compared to copper and can offset the 3D-IC benefits [2]. Thus we focus our analysis on copper TSV-induced stress.

The electrical effect of these unintentional thermal stresses is based on their impact on two transistor electrical parameters, namely the low-field mobility and the threshold voltage. The changes in transistor electrical parameters affect gate-level performance metrics such as gate delay and gate leakage power, which perturb circuit-level performance metrics such as critical path delay and circuit leakage power.

Both STI- and TSV-induced stress effects are highly layout-dependent: shifts in transistor performance depend upon its relative position with respect to the source of stress (e.g., TSV locations and STI geometries) in the layout. For example, STI abuts the transistors and can be in non-uniform shapes, as shown in Figure 1(a). For example, in order to determine the changes in delay due to STI on gate g6, it is necessary to consider the STI contributions from within the gate and also from surrounding gates – specifically, gates g2 through g7, g9, and g10. Figure 1(b) shows a section of a 3D-IC layout with four TSVs with transistors distributed between them. The transistors are separated by STI (yellow regions). Beyond STI-induced stress, each TSV contributes to stress-induced electrical variations in the transistors, whose magnitude depends upon the relative position of the transistor and the TSV.



(a) (b)

Fig. 1. (a) A segment of a circuit layout showing how the STI in adjacent cells, or in gaps between cells, imply that the shape of an STI region depends on the layout of neighboring cells. (b) A layout snippet with four TSVs (blue) with transistors between them separated by STI (yellow). Each TSV spans 7 standard cell rows.

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Layout-dependent stress effects can be captured by either pre-characterization, finite element method (FEM) simulation, using analytical modeling approaches, or through semianalytical approaches where stress effects are simulated for parameterized layout conditions. For STI, finite element method (FEM) based simulations can predict the stress in the layout accurately, but are computationally prohibitive for realistic layouts [1], [3]. Semi-analytical methods precharacterize a large number of layouts and use a fitting function for stress. However, these methods can be impractical due to the high cost precharacterizing a sufficiently large number of layouts, and of storing the characterized data. Analytical models can enable fast analysis on large circuits, but in the past, it has been challenging to build accurate models. However, prior methods [4]–[7] are based on one-dimensional models considering the STI contributions from adjacent standard cells within the same row in row-based placements. Moreover, only a single component of the stress tensor, which is longitudinal to the transistor channel direction, is taken into account while the entire stress tensor needs to be taken into consideration while evaluating changes in circuit performance. The work in [8] uses both longitudinal and transverse direction STI contributions, but is based on an empirically fitted model that is not scalable for non-rectangular shaped active/STI regions. Our work considers both longitudinal and transverse STI regions into account and also takes into the account the entire stress tensor while analytically evaluating changes in transistor performance. This papers delivers an analytical modeling solution for STI-induced stress that is comparable in accuracy with FEA-based modeling and comparable in computational cost of the simpler 1D solution.

TSV-induced stress effects alone have also been analyzed using FEM [9], [10], though neither work related the stress to circuit performance. In [9] it was shown experimentally that PMOS and NMOS transistor mobilities vary in opposite directions depending upon their relative orientation with respect to the TSVs. The work in [11] uses finite element method to record stress and uses it to determine the performance impact on small ring oscillator structures, where the performance impact was small since NMOS and PMOS transistors were closely placed, which resulted in the cancellation of their opposing stresses. The work in [12] and [13] presents analytical methods to analyze circuit performance variations. While the former work considered an inaccurate uniaxial based stress model (only one stress tensor component), the latter presents a detailed model that considers the biaxial nature of TSV-induced stress along with other features such as the thin liner material surrounding the TSV structure.

The effects of STI and TSV have been considered together in the work in [14]. However, the STI model is based on an empirically fitted one-dimensional stress model that considers only one stress tensor component and takes into account STI in the longitudinal direction alone. The TSV-stress model captures the biaxial nature of the stress but is based on a simplistic axisymmetric model that does not consider the liner material, whose impact can be significant [13].

To evaluate the changes in circuit performance metrics due to stress effects, we first need to evaluate the changes in gate performance metrics which are a function changes in transistor electrical parameters, which are in turn a function of the underlying stress tensor components. It should be noted that nonlinear relationships hold between dependent and independent parameters at every stage of translation from stress domain to electrical parameter domain to gate/circuit performance metric domain. Thus linear superposition is not valid in the transistor electrical parameter domain or in the domain of gate/circuit performance metrics. Linear superposition of stress is a standard technique in the field of mechanics to obtain the net stress due to multiple independent sources of stress. It must be noted that stress is represented as a tensor and consequently the individual tensor components from different sources of stress must be added to evaluate the net stress tensor during superposition. This net stress can be used to compute circuit performance by the aforementioned sequence of translations.

In this work, we present an analytical model to accurately capture the effects of STI by considering its three-dimensional structure, and we evaluate circuit performance variations considering both longitudinal and transverse STI contributions. In addition, in 3D-ICs, we combine the STI-induced stress with TSV-induced stress together in a single analysis and evaluate the ensuing circuit performance variations. For TSV-induced stresses, we use the model presented in [13]. In particular,

- we apply micromechanical inclusion based theory to accurately evaluate STI-induced stress. For 3D-ICs using planar transistor technologies, we combine the effects of STI and TSV using linear superposition technique.
- we translate the STI-only and STI+TSV stress models into corresponding transistor mobility and threshold voltage variations.
- we show the impact of STI on circuit critical path delay and leakage power variations for planar ICs and stacked 3D-ICs; for the latter we consider the impact of TSV-induced circuit performance variations together with STI induced effects.

The paper is organized as follows. Section II describes a stress modeling approach for STI and then combines the model with TSV-induced stress for 3D-IC considerations using linear superposition. In Section III, we present electrical models that translate stress into mobility and threshold voltage variations for planar ICs (STI-only) and for 3D-ICs (STI+TSV). In Section IV, we see how all of this information is drawn together to evaluate performance. The results of circuit benchmarks using our methods are presented in Section V for planar and 3D-IC layouts in 45nm, 32nm, and 22nm process technologies, followed by concluding remarks in Section VI.

II. Stress Modeling

Mismatches in the coefficients of thermal expansion (CTEs) result in stresses in transistors that affect their performance. In planar 2D transistor technologies, a significant source of this stress is due to STI, the SiO_2 region of shallow depth embedded in silicon at a high temperature. In 3D-ICs, the stress is induced both due to STI and due to CTE mismatch between the copper TSV and its neighboring materials. TSVs

made of copper are embedded in silicon at a high temperature. In the Manhattan geometries employed in chip design, STI shapes are rectilinear. On the other hand, TSVs are cylindrical in shape, span the entire depth of the substrate, and are often surrounded by a thin layer of dielectric material such as SiO_2 or Benzocyclobutene (BCB). Owing to the different geometrical shapes and manufacturing conditions, STI and TSV may require different paradigms for solving the basic equations of elasticity to determine their respective stress states in the transistor channels.

The magnitudes of the stress contributions from STI and TSV depend upon the corresponding material parameters and respective geometries of the stressors. This section presents and develops models for these stresses. The material parameters used in this work are shown in Table I. While STI regions abut the transistor active regions in the layout, TSVs necessitate a keep-out-zone (KOZ) around it where transistors are not allowed in the layout for mechanical reliability concerns.

TABLE I
PHYSICAL CONSTANTS FOR STRESS COMPUTATION

	E (GPa)	**CTE (ppm/^{o}C)**	ν
Silicon	162.0	3.05	0.28
SiO_2	71.7	0.51	0.16
BCB	3	40	0.34
Copper	111.5	17.7	0.343

The stress state of a mechanical system is defined by three displacement components, six stress components, and six strain components. We begin by presenting the fundamental equations of elasticity and the relation between displacement, stress, and strain. The stress and strain components are obtained by solving the system of elasticity equations with suitable boundary conditions considering the geometry of thermally mismatched materials. Next, we present the STI-induced stress model using a model based on inclusion theory, and then briefly describe the TSV stress model elaborated in [13]. The stress in planar ICs is due to STI alone, while stress in 3D-ICs is obtained by superposition of STI-induced and TSV-induced stress contributions.

Coordinate system: Most integrated circuits are manufactured on wafers with their channels parallel or perpendicular to [110] silicon crystal orientation, which also corresponds to the wafer flat direction [15]. The axis perpendicular to the wafer surface usually corresponds to (001) Si crystal orientation. Thus a natural coordinate system would be along [110], $[\bar{1}10]$ and [001] [15], which corresponds to a 45° rotation of the Cartesian coordinate system. We represent the crystallographic coordinate system using primed notation and the axes are denoted by (x', y', z') in the rest of the paper.

A. Notations and Fundamental Equations of Elasticity

Before we develop the stress model, we describe the notation and the fundamental equations used in describing a stress state. In this paper, all materials are assumed to be isotropic and homogeneous. We employ the standard concise Einstein notation, where repeated indices imply summation, and we represent the three coordinate axes as (x_1, x_2, x_3), respectively. In general, to obtain the stress state of a mechanical system, we need 15 components:

- six unique stress components σ_{ij} (stress tensor),
- six unique strain components ϵ_{ij} (strain tensor), and
- three displacements u_i (displacement tensor)

where $i, j \in \{x_1, x_2, x_3\}$ for any orthogonal coordinate system. The 15 unknowns are determined by solving the following 15 equations:

- 6 stress-strain equations (Hooke's Law):

$$\sigma_{ij} = C_{ijkl}(\epsilon_{kl} - \delta_{kl}\alpha\Delta T) \tag{1}$$

- 6 strain-displacement equations:

$$\epsilon_{ij} = \frac{1}{2}\left(\frac{\partial u_i}{\partial j} + \frac{\partial u_j}{\partial i}\right) + \delta_{ij}\alpha\Delta T \tag{2}$$

- 3 force-balance equations:

$$\frac{\partial \sigma_{ix_1}}{\partial x_1} + \frac{\partial \sigma_{ix_2}}{\partial x_2} + \frac{\partial \sigma_{ix_3}}{\partial x_3} + B_i = 0 \tag{3}$$

Here, $i, j, k, l \in \{x_1, x_2, x_3\}$, δ_{ij} is Kronecker's delta function, α denotes the coefficient of thermal expansion, ΔT refers to the change in temperature, and B_i is the external body force. The values of the physical constants used in this work are given in Table I.

The C_{ijkl} elements here represent the components of the stiffness tensor and is a function of Young's modulus E and Poisson's ratio ν of the material. The nonzero components are given below:

$$\begin{aligned}
C_{1111} = C_{2222} = C_{3333} &= \frac{E(1-\nu)}{(1+\nu)(1-2\nu)} \\
C_{1122} = C_{2233} = C_{1133} &= \frac{E\nu}{(1+\nu)(1-2\nu)} \\
C_{2211} = C_{3322} = C_{3311} &= \frac{E\nu}{(1+\nu)(1-2\nu)} \\
C_{1212} = C_{3131} = C_{2323} &= \frac{E}{2(1+\nu)}
\end{aligned} \tag{4}$$

The solution of Equations (2) and (3) depends upon the geometry and boundary conditions of the mechanical system. The Equation (1) purely depends upon the material under consideration.

When the body forces $B_i, i \in \{x_1, x_2, x_3\}$ are zero, it can be shown that the displacements or stresses can be represented in terms of a function Φ that satisfies the relation:

$$\nabla^4 \Phi = 0 \tag{5}$$

The solution to the system of elasticity equations can be found in terms of a *biharmonic function*, Φ, that satisfies the specified boundary conditions of the system. A biharmonic [harmonic] function is a function whose fourth [second] order partial derivative is zero.

B. STI Stress Model

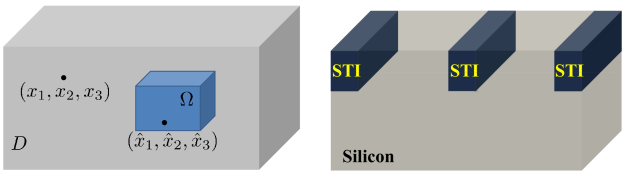
As stated earlier, STI is embedded in silicon at a high temperature of 1000°C and thus contributes to a residual thermal stress in silicon post manufacturing at room temperature. Owing to the very high initial temperature, the temperature differential remains fairly constant in the range of circuit operating temperatures. STI abuts the transistor

active regions and can be considered as the negative image of the rectangular active regions in the layout. STI can be in arbitrary rectilinear shapes, but STI can be divided into non-intersecting cuboidal shapes whose stress contributions are linearly superposed. Therefore, the fundamental problem relates to obtaining the stress distribution in silicon due to a cuboidal-shaped STI. This can be achieved by solving the fundamental equations of elasticity in three dimensions while applying suitable boundary conditions. Although closed-form solutions have been obtained for basic two-dimensional geometries using simplifications, it is unwieldily to directly solve the system of elasticity equations for a three-dimensional structures such as the STI. Alternatively, we can make use of the fact that in the absence of external body forces, the system of equations reduce to a biharmonic form as shown in Equation (5). This useful property has been employed in micromechanical stress modeling to deduce the stress state for complex geometries. In a displacement formulation [stress formulation] the displacement [stress] is equated to the second partial derivative of a biharmonic function that satisfies the boundary conditions [16]. Once the displacement [stress] is known, the other unknowns of the stress state can be determined from Equations (1), (2), and (3). The Galerkin vector function satisfies the biharmonic criteria and is used in the displacement formulation paradigm to evaluate the stress state. The Galerkin vector function is a combination of primitive potential functions accounting for volume and shape changes of the mechanical system.

1) The Inclusion Problem in Micromechanics: In this work, we work directly with three-dimensional cuboidal shapes by employing *inclusion theory* from micromechanics [17] to estimate the stresses and strains in the active silicon arising due to thermal mismatches with cuboidal STI shapes that have finite sizes in three dimensions. In micromechanics, an inclusion is a subdomain with an initial strain embedded in a larger domain, either having similar or dissimilar mechanical properties. However, general STI geometries may have arbitrary three-dimensional rectilinear shapes, as observed in Figure 1(a). It is a common practice [18] in micromechanics to divide an arbitrary shaped inclusion into smaller substructures and use linear superposition to find the total stress. Accordingly, a general STI geometry will be represented as a union of smaller cuboidal shapes, and the stress and strain contributions from these shapes can be superposed. In elasticity, a nucleus of strain is a singular point in an elastic medium, where an applied force results in displacements and stress in the rest of the medium. By knowing the solutions of such nuclei of strain, we can construct the overall stress solution due to an arbitrary shaped inclusion; the inclusion is treated as a collection of continuous nuclei of strain. This is analogous to finding the electric field due to an arbitrary charge distribution based on the point charge solution.

In continuum mechanics, inelastic strains are those that occur even in the absence of external body forces and thus can never be removed. Residual strains such as thermal mismatch strains, initial strains, and misfit strains (due to crystal defects) are examples of inelastic strains. In micromechanics such strains as termed as eigenstrains [17]. The six possible eigenstrains in any coordinate system (x_1, x_2, x_3) are denoted by e_{ij} for $i, j \in \{x_1, x_2, x_3\}$.

Furthermore, any subdomain Ω having an initial nonzero eignenstrain, embedded in a domain D with zero initial eigenstrains, and either having similar or dissimilar mechanical properties, is known as a mechanical inclusion. Figure 2(a) shows an example of a cuboidal inclusion embedded in a semi-infinite space. A homogeneous (inhomogeneous) inclusion is one with domain D and subdomain Ω having similar (dissimilar) mechanical properties. The domain has typically much larger dimensions as compared to the subdomain. The inclusion problem in micromechanics finds the stress state of such a system. There has been a rich body of work on this class of problems in micromechanics and several useful solutions have been proposed [18]–[21].



(a) (b)

Fig. 2. (a) A general inclusion in half-space. (b) STI as a cuboidal inclusion.

Shallow trench isolation (STI) is made up of SiO_2 and is embedded in silicon at a high temperature of 1000°C. The thickness of STI is of the order of few hundreds of nanometers, while the thickness of silicon substrate is typically of the order of several tens or hundreds of micrometers. Figure 2(b) shows three STI inclusions in silicon.

After manufacturing, owing to the CTE mismatch, seen in Table I, between Si and SiO_2, there is a residual thermal stress induced in active silicon. Compared to when it was manufactured, STI is comparatively smaller in volume to the silicon substrate and causes inelastic thermal strains, and it can be considered as an inhomogeneous inclusion within Si. In general, an STI structure is in the form of an arbitrary rectilinear shape, and we decompose this shape STI into elementary cuboidal shapes and superpose known solutions for cuboidal inclusion problems. Thus, we can treat STI as a cuboidal inclusion and obtain the effective eigenstrains in silicon by following a series of fictitious mechanical operations, as is the case with most inhomogeneous inclusion problems [17].

The procedure for analyzing an STI inclusion within silicon is summarized below:

1) We first conceptually "remove" the STI from substrate at $T = 1000$°C and allow both STI and the silicon substrate to undergo thermal contraction to room temperature, i.e., 25°C. This implies that ΔT = 975°C can be used in the stress formulation. The thermal strains in STI and silicon are $\epsilon_{ij}^{T(SiO_2)} = \delta_{ij}\alpha^{SiO_2}\Delta T$ and $\epsilon_{ij}^{T(Si)} = \delta_{ij}\alpha^{Si}\Delta T$, respectively. Since the inclusion (STI) as well as the domain (silicon) undergo free thermal contractions, the stresses in both materials are zero.
2) Next, we apply a fictitious tensile force of $F_{ij}^{SiO_2} = C_{ijkl}^{SiO_2}\epsilon_{ij}^{T(SiO_2)}$ on the STI inclusion and a fictitious

compressive force of $-F_{ij}^{Si} = -C_{ijkl}^{Si}\epsilon_{ij}^{T(Si)}$ on silicon to bring them to original shapes.

3) The SiO_2 is now considered to be welded back into the silicon and the fictitious forces are removed and are replaced by an effective force applied on the insides of the silicon domain of $\Delta F_{ij} = F_{ij}^{Si} - F_{ij}^{SiO_2}$. ΔF_{ij} is the equivalent force applied by a homogeneous inclusion with a initial strain.
4) The equivalent eigenstrain due to this equivalent force in silicon is given by $e_{ij}^{Si} = {C_{ijkl}^{Si}}^{-1}\Delta F_{ij}$.

The strain thus obtained is used to compute the overall stress using the fundamental solutions for different types of nuclei of strain.

2) Solution due to nuclei of strain: The inclusion in a domain is treated as a collection of nuclei of strain. In the thermal stress problem due to STI, silicon undergoes shape changes and volume changes. The nuclei of strain corresponding to the resultant displacements in the domain (silicon) can be enumerated as:

- Unit double force without moment: Two equal and opposite forces acting at a point along a coordinate axis direction results in stretching or shrinking of the elastic medium about the point along the axis direction.
- Unit double force with moment: Two equal and opposite forces orthogonal to each other acting at a point in the inclusion along mutually perpendicular coordinate axes directions, results in twisting of the elastic medium about the point.
- Center of dilation: Three mutually perpendicular unit double forces acting at a point results in expansion or contraction (changes in volume) of the elastic medium about the point without shape changes.

In micromechanics, there are known solutions to the three fundamental nuclei of strain accounting for shape and volume changes. The individual solutions due to the nuclei of strain are obtained from the Galerkin vector potential function which satisfies the biharmonic property. It can be recalled that, in the absence of body forces, the system of elasticity equations are reduced to a biharmonic equation as described in Section II-A Using displacement formulation in displacement potential theory, The displacement [stress] can be expressed as a second [third] partial derivative of the Galerkin vector potential function. The volumetric integral of the fundamental solutions about the inclusion geometry results in the final stress solution in the elastic medium. The strain components can then be obtained by applying Hooke's Law in Equation 1.

In a general coordinate system, any point can be represented by a tuple (x_1, x_2, x_3) and the corresponding position vector is denoted by $\mathbf{x}$. The points in an inclusion are known as source points and the points in the domain are known as observation points. We are interested in computing the stress state at the observation points. Let $(\hat{x}_1, \hat{x}_2, \hat{x}_3)$ denote a point in the source subdomain; the corresponding position vector is denoted by $\hat{\mathbf{x}}$. The elastic displacements u_i and stress components σ_{ij} due to eigenstrains $e_{ij}, i, j \in \{x_1, x_2, x_3\}$ in terms of a Galerkin vector function $\mathbf{\Phi}(\mathbf{x})$ are given by [18]:

$$\begin{aligned} 2\mu u_i(\mathbf{x}) &= 2(1-\nu)\Phi_{i,jj} - \Phi_{k,ki} \\ \sigma_{ij}(\mathbf{x}) &= \nu\Phi_{k,kmm}\delta_{ij} - \Phi_{k,kij} \\ &\quad +(1-\nu)(\Phi_{i,kkj} + \Phi_{j,kkj}), \mathbf{x} \notin \Omega \\ \sigma_{ij}(\mathbf{x}) &= \nu\Phi_{k,kmm}\delta_{ij} - \Phi_{k,kij} \\ &\quad +(1-\nu)(\Phi_{i,kkj} + \Phi_{j,kkj}) \\ &\quad -2\mu e_{ij} - \lambda e_{kk}\delta_{ij}, \mathbf{x} \in \Omega \end{aligned} \tag{6}$$

Here, μ and λ are the elastic Lamé constants given in Table II. The Galerkin vector function $\mathbf{\Phi}(\mathbf{x})$ is biharmonic and satisfies $\nabla^4\mathbf{\Phi}(\mathbf{x}) = 0$, and is a function of elementary Galerkin vectors composed of biharmonic and harmonic potential functions. It is chosen so that it satisfies two primary boundary conditions of the inclusion problem:

- all components of stress should vanish at infinite distance from the inclusion, $\sigma_{ij}^D(\infty) = 0$ for $i, j \in \{x_1, x_2, x_3\}$.
- there should be a displacement continuity across the inclusion and domain boundary. $u_i^\Omega = u_i^D$ for every $i \in \{x_1, x_2, x_3\}$.

TABLE II
STRESS AND STRAIN TENSOR COMPONENTS

Stress components used in mobility computations

$$\sigma_{x'x'} = C^\sigma\Big[(2+4\nu^{Si})\phi_1 + (6-4\nu^{Si}-8(\nu^{Si})^2)\bar{\phi}_1 + 2\nu^{Si}\phi_2 + 2\nu^{Si}\phi_3 - 2\nu^{Si}\bar{\phi}_2 - 2\nu^{Si}\bar{\phi}_3\Big]_{x'-a_2,y'-b_2,z'\pm c_2}^{x'-a_1,y'-b_1,z'\pm c_1}$$

$$\sigma_{y'y'} = C^\sigma\Big[(2+4\nu^{Si})\phi_2 + (6-4\nu^{Si}-8(\nu^{Si})^2)\bar{\phi}_2 + 2\nu^{Si}\phi_1 + 2\nu^{Si}\phi_3 - 2\nu^{Si}\bar{\phi}_1 - 2\nu^{Si}\bar{\phi}_3\Big]_{x'-a_2,y'-b_2,z'\pm c_2}^{x'-a_1,y'-b_1,z'\pm c_1}$$

$$\sigma_{x'y'} = C^\sigma\Big[(2+2\nu^{Si})\chi + (6-2\nu^{Si}-8(\nu^{Si})^2)\bar{\chi} - \psi - (3-4\nu^{Si})\bar{\psi} + 4(1-2\nu^{Si})(1-\nu^{Si})\bar{\eta}\Big]_{x'-a_2,y'-b_2,z'\pm c_2}^{x'-a_1,y'-b_1,z'\pm c_1}$$

Strain components used in threshold voltage computations

$$\epsilon_{xx} = \frac{1}{2E^{Si}}[(1-\nu^{Si})(\sigma_{x'x'} + \sigma_{y'y'}) + (1+\nu^{Si})(\sigma_{x'y'}]$$

$$\epsilon_{yy} = \frac{1}{2E^{Si}}[(1-\nu^{Si})(\sigma_{x'x'} + \sigma_{y'y'}) - (1+\nu^{Si})(\sigma_{x'y'}]$$

$$\epsilon_{xy} = \frac{(1+\nu^{Si})}{2E^{Si}}[\sigma_{y'y'} - \sigma_{x'x'}];\ \epsilon_{zz} = \epsilon_{zx} = \epsilon_{zy} = 0.$$

Elementary functions and constants

$$\phi_1 = \tan^{-1}\left(\frac{\xi_2\xi_3}{\xi_1 r}\right); \phi_2 = \tan^{-1}\left(\frac{\xi_1\xi_3}{\xi_1 r}\right); \phi_3 = \tan^{-1}\left(\frac{\xi_1\xi_2}{\xi_3 r}\right)$$

$$\bar{\phi}_1 = \tan^{-1}\left(\frac{\xi_2\bar{\xi}_3}{\xi_1\bar{r}}\right); \bar{\phi}_2 = \tan^{-1}\left(\frac{\xi_1\bar{\xi}_3}{\xi_1\bar{r}}\right); \bar{\phi}_3 = \tan^{-1}\left(\frac{\xi_1\xi_2}{\bar{\xi}_3\bar{r}}\right)$$

$$\chi = \log(r+\xi_3); \bar{\chi} = \log(\bar{r}+\bar{\xi}_3);$$

$$\psi = \frac{\xi_1^2+\xi_2^2}{r(r+\xi_3)} + \frac{\xi_3}{r}; \bar{\psi} = \frac{\xi_1^2+\xi_2^2}{\bar{r}(\bar{r}+\bar{\xi}_3)} + \frac{\bar{\xi}_3}{\bar{r}}; \bar{\eta} = \frac{\xi_1^2+\xi_2^2}{2(\bar{r}+\bar{\xi}_3)^2} + \frac{\bar{\xi}_3}{\bar{r}+\bar{\xi}_3}$$

$$r = \sqrt{\xi_1^2+\xi_2^2+\xi_3^2}; \bar{r} = \sqrt{\xi_1^2+\xi_2^2+\bar{\xi}_3^2};$$

$$\xi_1 = x' - \hat{x}'; \xi_2 = y' - \hat{y}'; \xi_3 = z' - \hat{z}'; \bar{\xi}_3 = z' + \hat{z}'$$

$$C^\sigma = \frac{\mu e^{Si}}{8\pi(1-\nu^{Si})}$$

$$e^{Si} = \frac{1-2\nu^{Si}}{E^{Si}}\Big(\frac{E^{Si}\alpha^{Si}\Delta T}{1-2\nu^{Si}} - \frac{E^{SiO_2}\alpha^{SiO_2}\Delta T}{1-2\nu^{SiO_2}}\Big)$$

$$\mu^M = \frac{E^M}{2(1+\nu^M)}; \lambda^M = \frac{E^M\nu^M}{(1+\nu^M)(1-2\nu^M)}, \text{for} M \in \{Si, SiO_2\}$$

A general solution for a cuboidal inclusion in a half-space has been presented in [18]. The work presents a detailed math-

ematical framework based on Galerkin vector formulation. The half-space (semi-infinite) solutions are usually a combination of two sub-problems: a physical inclusion in an infinite space with a prescribed eigenstrain, and a fictitious "image" inclusion in the infinite space whose eigenstrain is chosen to recover the half-space condition. In [18], the Galerkin vector potential function is represented as a volumetric integral of elementary potential functions, integrated over the dimensions of the physical and the "image" inclusions. The general solution in [18] can predict the stress state at every point in the half-space domain for an any given eigenstrain tensor. For the STI-induced thermal stress problem, further simplifications are possible based on two observations:

- For a thermal stress problem, only the normal components of the eigenstrain tensor are present, $e_{ij}^{Si} \neq 0$ for $i = j$; zero otherwise.
- Since STI is near the surface of silicon and electrical current flows near the device surface, $z_1 = 0$ for the observation points.

Making use of these ensuing simplifications, we obtain closed-form expressions for the major stress and strain components used in computing electrical variations as seen in Section III. As pointed out in Section III-A, since integrated circuits are manufactured in the primed coordinate system, (x_1, x_2, x_3) can be replaced by (x', y', z') to represent the stress and strain tensor components in this primed system. The strain components in Cartesian coordinate system can be obtained by Hooke's Law and by appropriate coordinate transformations. For a cuboidal inclusion whose coordinates are described by the closed intervals, $\hat{x}' \in [a_1, a_2]$, $\hat{y}' \in [b_1, b_2]$, and $\hat{z}' \in [c_1, c_2]$, the final closed-form expressions are given in Table II in terms of elementary functions and constants. Since the Galerkin vector potential is a volumetric integral, the final expressions for the stress components $\sigma_{x'x'}$, $\sigma_{y'y'}$, and $\sigma_{x'y'}$ are of the form $[\sigma]_q^p = \sigma(p) - \sigma(q)$, where the superscript p [subscript q] corresponds to the upper-limit [lower-limit] of the volumetric integral. The positive sign in the limits of integration for z' correspond to set of functions $f \in \{\phi_1, \phi_2, \phi_3, \chi, \psi\}$ and correspond to the physical inclusion, while negative sign is used for the set of functions $\bar{f} \in \{\bar{\phi_1}, \bar{\phi_2}, \bar{\phi_3}, \bar{\chi}, \bar{\psi}, \bar{\eta}\}$ and correspond to the image inclusion.

To obtain the overall STI impact, we divide the STI in the transverse and longitudinal directions around an active region into non-intersecting cuboidal shapes and use the solution presented in Table II. The STI along [perpendicular to] the transistor current carrying direction is treated as longitudinal [transverse] component. We apply linear superposition and add all contributions from the adjoining STI to find the total stress and strains:

$$\sigma_{ij}^{STI} = \sum_{STI} \sigma_{ij}^{Si}; \qquad \epsilon_{ij}^{STI} = \sum_{STI} \epsilon_{ij}^{Si} \tag{7}$$

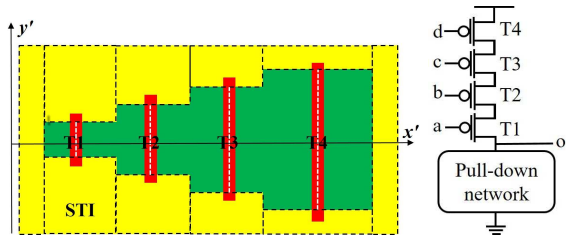
3) Comparison with the Finite Element Method: To verify the accuracy of the analytical stress model and the validity of linear superposition we perform finite element (FE) simulations using ABAQUS [22] on representative active silicon regions surrounded by STI (SiO_2) on all sides. To demonstrate the effectiveness of the superposition we use an irregular shaped active region as shown in Figure 3(a). We consider four diffusion connected transistors T1, T2, T3, and T4. This structure can be the pull-up network of a 4-input NOR gate with progressive sizing whose schematic is shown in Figure 3(b). In Figure 3(a), each active region (green) is about 250 nm wide. The electrical widths or the physical heights of the transistors are: W(T1) = 100nm, W(T2) = 200nm, W(T3) = 300nm, and W(T4) = 400nm. The channel length is 50nm. The boundary of the STI is 1600nm $\times$ 1200nm. We decompose these STI regions into ten smaller cuboids as shown in Figure 3(a). The stress is probed under the channel region below the poly (red) along the electrical width direction (dotted white line). We then apply our model described in Section II-B2 and use linear superposition to add contributions from each STI cuboid. Figures 4(a) and 4(b) show the resultant stress components $\sigma_{x'x'}$ and $\sigma_{y'y'}$, respectively, from FEM (dotted curves) and the analytical model (solid curves). From the two sub figures, the minimum, maximum, and average errors in stress between analytical model and FEM are found to be 0.01MPa, 32MPa, and 10MPa, respectively. Since the STI-induced stress is eventually translated into changes in delay, it is instructive to observe the error in estimating the delay instead. We consider the layout in Figure 3(a) to represent the layout of a 4-input NOR-gate shown in Figure 3(b). The magnitude of error in evaluating rise-time delay of each of the PMOS transistors, in 45nm technology with a supply voltage of 1V, is shown in Table III. The NOR-gate has a fan-out-of-four load. In Table III, D_{nom} corresponds to the nominal delay without stress effects, ΔD_{fem} corresponds to the change in delay using stress from FEM, and ΔE_{model} corresponds to the error in evaluating delay using stress from the analytical stress model compared to using stress from FEM. We can observe that the error in evaluating delay using the stress from the analytical model is well below 1%. This demonstrates that the analytical model provides very good accuracy while evaluating circuit performance. In addition, the time taken to evaluate the analytical stress for each transistor equals 0.46ms, which translates to 1.5ms for the structure shown in Figure 3(a). The corresponding FEM analysis for this representative structure takes about 80 minutes on a single 64-bit Intel® Xeon® CPU X5675 running at 3GHz. Thus, evaluating the analytical model is several orders faster than using FEM. Thus, our analytical model provides a good match even for non-rectangular active or STI regions and lends to faster analysis for large layouts. We have shown a comparison with FEM for a relatively small structure where FEM computations can be completed in a reasonable time (for large structures such as the 27K gate layout in Section V, it is impractical to evaluate the run-time).

TABLE III
ERROR IN DELAY ESTIMATION OF 4-INPUT NOR GATE

$Transistor$	$T1$	$T2$	$T3$	$T4$
D_{nom} (ps)	58.2	62.62	65.57	66.94
ΔD_{FEM} (%)	20.4%	19.1%	19.2%	18.7%
ΔE_{model} (%)	-0.2%	-0.3%	-0.3%	-0.2%

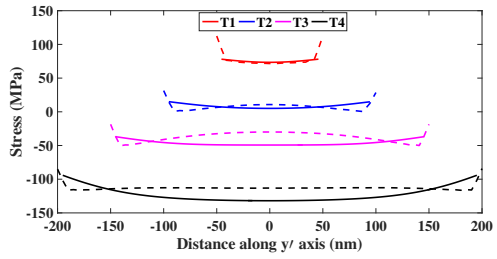
C. TSV-induced stress modeling

A TSV is typically made up of copper owing to its low resistivity, and is cylindrical in shape [23]. Often, the TSV

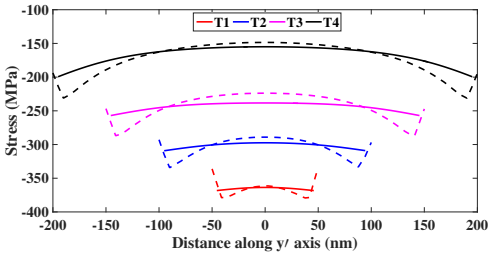


(a) (b)

Fig. 3. (a) An irregular shaped active region in STI. The STI is fragmented into smaller cuboids (rectangles in 2D) around the active regions. (b) Representative schematic of a 4-input NOR gate.



(a)



(b)

Fig. 4. Solid [dashed] lines showing our [FEM] model. (a) $\sigma_{x'x'}$ (b) $\sigma_{y'y'}$

is surrounded by a thin liner made up of SiO_2 or BCB (Benzocyclobutene). The cylindrical TSV structure along with the liner are embedded in silicon at a high temperature of 250°C. Post manufacturing, at room temperature, owing to the CTE mismatch between copper TSV, liner, and silicon a residual thermal stress exists in silicon.

In principle, the TSV can also be considered as a cylindrical inclusion and similar principles can be applied to evaluate the stress in silicon. However, the modeling approach requires complex numerical evaluations using elliptical integrals. On the other hand, we use a straightforward application of basic equations of elasticity using a 2D-axisymmetric assumption. Here, the TSV is modeled as a long concentric lined copper cylinder surrounded by silicon. The stress state can be evaluated across any 2D cross-section and thus is known as 2D-axisymmetric model. The 2D-axisymmetric assumption is reasonable since the height of a TSV is considerably larger than the diameter of the TSV the stress distributions is to be evaluated near the surface of the silicon alone where transistors channels reside. The finite size of the structure and the free surface condition of substrate are recovered by superposing a Boussinessq-solution which deals which stress in a semi-infinite space (half-space) when forces are applied on its surface.

In [13], a complete stress model is presented considering the interactions between various materials. First, the stress distributions are obtained in cylindrical coordinates using 2D-axisymmetric assumption and superposed with Boussinesq-type solution to make the surface of the silicon traction-free ($\sigma_{zz} = 0$). The stresses in cylindrical coordinates are then translated to crystallographic axes i.e., primed coordinate system. Let $(\overline{x'}, \overline{y'})$ denote the center of a TSV near the surface ($\overline{z'} = 0$) in the primed coordinate system. Similarly, let (x',y') be a point of interest in silicon. The stress distributions in silicon in the primed coordinate system are given as [13]:

$$\begin{aligned} \sigma^{TSV}_{x'x'} &= -\sigma y'y' = K\frac{\tilde{x}^2 - \tilde{y}^2}{(\tilde{x}^2+\tilde{y}^2)^2} \\ \sigma^{TSV}_{x'y'} &= K\frac{2\tilde{x}\tilde{y}}{(\tilde{x}^2+\tilde{y}^2)^2} \\ \sigma^{TSV}_{z'z'} &= \sigma^{TSV}_{x'z'} = \sigma^{TSV}_{y'z'} = 0 \end{aligned} \tag{8}$$

where $\tilde{x} = x' - \overline{x'}$ and $\tilde{y} = y' - \overline{y'}$. The parameter K captures the dimensions of the TSV+liner and the material property differences between TSV, liner, and silicon. This parameter contains terms that arise from summing the 2D-axisymmetric and Boussinesq solutions; a complete description of this parameter is given in [13]. This model is applicable to any cylindrical-shaped TSV technology. The corresponding strain distributions can be obtained by applying stress-strain relationships given in Equation (1). It can be noted that stress due to TSV in transistor channels depends upon the relative positions of transistors and the TSVs in the layout. Thus, TSV-induced stress is also placement dependent.

D. Stress in 2D and 3D integrated circuits

The individual stress contributions due to STI and TSV have been discussed so far. In planar 2D-ICs, STI is the primary contributor of placement dependent stress, while in 3D-ICs, both STI-induced and TSV-induced stresses contribute to stress in transistor channels. Thus, the stress and strain components in 2D-ICs σ^{2D}_{ij} and ϵ^{2D}_{ij} are given by:

$$\begin{aligned} \sigma^{2D}_{ij} &= \sigma^{STI}_{ij} \\ \epsilon^{2D}_{ij} &= \epsilon^{STI}_{ij} \end{aligned} \tag{9}$$

where $(i,j) \in \{x', y', z'\}$. The terms σ^{STI}_{ij} and ϵ^{STI}_{ij} correspond to the STI induced stress alone given in Equation (7). Similarly, the stress distributions in 3D-ICs σ^{3D}_{ij} and ϵ^{3D}_{ij} are obtained by linear superposition of STI and TSV contributions as:

$$\begin{aligned} \sigma^{3D}_{ij} &= \sigma^{STI}_{ij} + \sigma^{TSV}_{ij} \\ \epsilon^{3D}_{ij} &= \epsilon^{STI}_{ij} + \epsilon^{TSV}_{ij} \end{aligned} \tag{10}$$

Here σ^{TSV}_{ij} and ϵ^{TSV}_{ij} are the stress and strain components due to TSV, respectively, and are given in Equation (8).

III. Electrical Effects of STI-induced Stress

Applied mechanical stress causes changes in transistor electrical properties, specifically in the *mobility* and the *threshold voltage*. Mobility variations are caused by the piezoresistive

behavior of silicon, while threshold voltage variations occur due to changes in electronic band potentials due to applied stress. The induced changes in the mobility and threshold voltage can be expressed in terms of the stress and strain tensor, which characterize the mechanical stress as described in Section II. In planar/2D ICs, the electrical variations are primarily due to STI-induced thermal mismatch stress. On the other hand, in 3D-ICs, the combined effects of STI and TSV contribute to overall electrical variations.

A. Variation of Mobility with Stress

According to piezoresistivity, an applied mechanical stress causes changes in resistivity and hence the mobility of the transistors. The piezoresistive behavior of silicon is highly dependent upon the crystallographic orientation of silicon. A complete mathematical model for piezoresistivity has been presented and demonstrated in silicon in [15]. The relative change in mobility for transistors oriented along [110] crystallographic direction is given as:

$$\frac{\Delta\mu'}{\mu'} = \pi'_{11}\sigma^{IC}_{x'x'} + \pi'_{12}\sigma^{IC}_{y'y'} \tag{11}$$

Here, π'_{11} and π'_{12} are the piezoresistive coefficients in $[110]-[\bar{1}10]$ coordinate system. The values of the piezoresistive coefficients are given in Table IV. The terms $\sigma^{IC}_{x'x'}$ and $\sigma^{IC}_{y'y'}$ are two primary stress components where $IC \in \{2D, 3D\}$. The stress distributions in 2D-ICs and 3D-ICs are given in Equation (9) and Equation (10), respectively.

TABLE IV
PIEZORESISTIVITY COEFFICIENTS (x10^{-12} Pa^{-1}) IN [100] SI [10]

	π_{11}	π_{12}	π_{44}	π'_{11}	π'_{12}	π'_{44}
NMOS	1022.0	−537.0	136.0	310.5	174.5	1559.0
PMOS	−66.0	11.0	−1381.0	−717.5	662.5	−77.0

B. Variation of Threshold Voltage with Stress

According to deformation potential theory [24], [25], mechanical strain in the channel causes shifts and splits in conduction and valence band potentials. This results in corresponding shifts in the threshold voltage of the transistors and can be attributed to changes in silicon electron affinity, band gap, and valence band density-of-states. The changes in conduction and valence band potentials can be expressed as [24]:

$$\begin{aligned}
&\Delta E_C^{(i)}(\epsilon) = \Xi_d\left(\epsilon_{x'x'} + \epsilon_{y'y'} + \epsilon_{z'z'}\right) + \Xi_u\epsilon_{ii}, i \in \{x', y', z'\} \\
&\Delta E_V^{(hh,lh)}(\epsilon) = a\left(\epsilon_1 + \epsilon_2 + \epsilon_3\right) \\
&\pm\sqrt{\frac{b^2}{4}(\epsilon_{x'x'} + \epsilon_{y'y'} - 2\epsilon_{z'z'})^2 + \frac{3b^2}{4}(\epsilon_{x'x'} - \epsilon_{y'y'})^2 + d^2\epsilon^2_{x'y'}}
\end{aligned} \tag{12}$$

Here, $\Delta E_C^{(i)}$ is the change in the conduction band potential energy in the carrier band number i. The term E_V^{hh} (E_V^{lh}) denotes the heavy-hole (light-hole) valence band potential. The positive (negative) sign is used for E_V^{hh} (E_V^{lh}). The terms Ξ_d and a are the hydrostatic deformation potential constants and the terms Ξ_u, b, and d are the shear splitting deformation potential constants whose values are given in Table V. The terms $\epsilon_i, i \in \{1, \cdots, 6\}$ correspond to the six strain components in the Cartesian coordinate system, and correspond to $\epsilon_{x'x'}$, $\epsilon_{y'y'}$, $\epsilon_{z'z'}$, $2\epsilon_{y'z'}$, $2\epsilon_{z'x'}$, and $2\epsilon_{x'y'}$, respectively. The expressions for strain components in 2D-ICs and 3D-ICs are given in Equation (9) and Equation (10), respectively.

TABLE V
BAND EDGE DEFORMATION POTENTIAL CONSTANTS [24]

Ξ_d (eV)	Ξ_u (eV)	a (eV)	b (eV)	d (eV)
1.13	9.16	2.46	−2.35	−5.08

The threshold voltage is a function of band-gap potential and thus can be expressed as a function of the changes in conduction band and valence band potentials. In this work, the changes in the electronic band potentials are dependent on the STI-induced stains. Ignoring the changes in the densities of states whose contributions are negligible [25], we have

$$\begin{aligned}
q\Delta V_{thp} &= m\Delta E_V - (m-1)\Delta E_C \\
q\Delta V_{thn} &= m\Delta E_C - (m-1)\Delta E_V
\end{aligned} \tag{13}$$

where ΔV_{thp} and ΔV_{thn} are the changes in PMOS and NMOS threshold voltages, respectively, $q = 1.6 \times 10^{-19}$C is the electron charge, and m is the body-effect coefficient and takes values 1.3−1.4. ΔE_C is the minimum of the changes in conduction band potentials, ΔE_C^i and ΔE_V denotes the maximum of the changes in valence band potentials, $\Delta E_V^{hh} and \Delta E_V^{lh}$.

C. Application of STI-induced electrical variation models

The electrical variation models discussed above are now applied to a minimum sized inverter in 22nm technology. Figure 5 shows the layout of an inverter with STI around it fragmented into non-intersecting cuboidal shapes. In the figure, regions I, II, and V correspond to transverse STI; regions III and IV represent longitudinal STI. For a given standard cell layout, the STI in the middle of PMOS and NMOS transistors (region V) remains the same size while the lateral and vertical dimensions of longitudinal STI (regions III and IV) and transverse STI (regions I and II) can vary depending upon the placement of its neighboring standard cells.

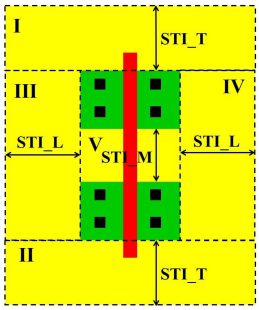


Fig. 5. Layout of an inverter with STI. The PMOS well is not shown here. Here STI_T [STI_L] denotes transverse [longitudinal] STI. STI_M is a fixed dimension STI in between NMOS and PMOS.

Figure 6 shows the range of mobility variations experienced by PMOS and NMOS transistors in a typical 22nm inverter by varying the sizes of longitudinal and transverse STI. Similarly, Figure 7 shows the range of threshold voltage variations

in PMOS and NMOS transistors of the 22nm inverter with varying longitudinal and transverse STI conditions. Note that the dimensions of the middle STI remains unchanged. An *isolated* transistor [standard cell] with no immediate neighboring transistors [standard cells] corresponds to the case with large longitudinal and transverse STI. On the other hand, a transistor [standard cell] in a *closely-packed* layout corresponds to the case with minimal dimensions of surrounding longitudinal and transverse STI components. In each of the sub-figures of Figures 6 and 7, the bottom left corner corresponds to a *closely-packed* layout scenario, while the top right corner corresponds to an *isolated* layout scenario. In general, most of the standard cells in a layout will have STI conditions between the two extreme scenarios. The analytical models presented in this work are applicable to an arbitrary layout condition. From the figure, we can conclude the following:

- By observing the scales of the PMOS and NMOS mobility variations in Figure 6(a) and Figure 6(b), respectively, we can observe STI-induced stress can result in mobility improvements or degradations in PMOS transistors, while NMOS transistors undergo mobility degradation alone. From Figure 6(a), at minimum transverse STI conditions, PMOS experiences only mobility improvements with increasing longitudinal STI. With increasing transverse STI, PMOS can experience mobility degradations (at comparatively smaller longitudinal STI conditions) and diminishing mobility improvements as longitudinal STI contribution increases. For NMOS transistors, the mobility degradation is a weak function of transverse STI, while it is a strong function of longitudinal STI; the greater the longitudinal STI, greater the NMOS mobility degradation.
- By observing the signs of the threshold voltage variation in Figure 7, we can conclude that both NMOS (negative threshold voltage changes) and PMOS (positive threshold voltage changes) transistors experience threshold voltage improvements due to surrounding STI. Moreover, the magnitudes of threshold voltage improvements in both PMOS and NMOS transistors is proportional to the amount of STI surrounding the transistors in the layout. The improvements in threshold voltage indicate increase in standard cell leakage power due to STI.

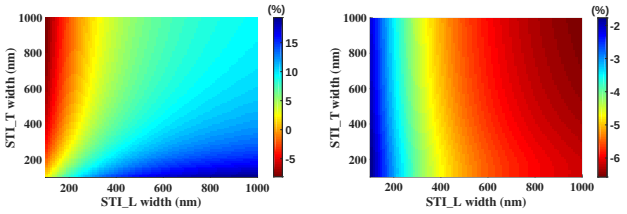


Fig. 6. STI-induced (a) PMOS and (b) NMOS mobility variations.

IV. Circuit Performance Evaluation

Using the methods described in Sections II and III, for a given layout, the changes in the device mobility and threshold voltage can be computed for each transistor. The electrical

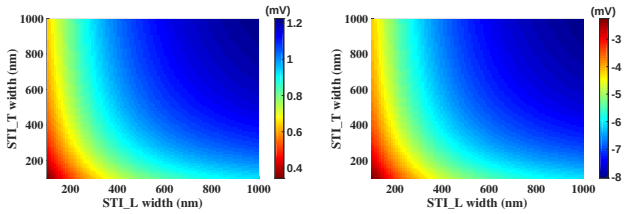


Fig. 7. STI-induced (a) PMOS and (b) NMOS threshold voltage variations.

variations in planar [3D] ICs is due to STI alone [STI+TSV]. We compute the average of the electrical variations in the channel along the transistor width, and then evaluate the variations in circuit performance by conducting static timing analysis and leakage power analysis. A logic gate is composed of several transistors. The STI-induced stress can cause unequal magnitudes of electrical variations in each of the transistors within a gate. However, owing to the large size of a TSV (few microns) compared to a logic gate (several nanometers), the magnitudes of electrical variations in individual transistors of a logic gate remains identical. When both TSV and STI effects are taken into account, the electrical variations could be dissimilar in individual transistors.

For a gate with n transistors, the delay under variations in the threshold voltage $V_{th,i}^{str}$ and mobility μ_i^{str} for the i^{th} transistor, $1 \leq i \leq n$, can be computed using a first-order Taylor expansion:

$$D^{str} = D^0 + \sum_{i=1}^{n} \left(\frac{\partial D}{\partial \mu_i}\bigg|_0 \Delta\mu_i^{str} + \frac{\partial D}{\partial V_{th,i}}\bigg|_0 \Delta V_{th,i}^{str} \right) \quad (14)$$

where D^{str} is the total gate delay due to STI-induced and/or TSV-induced stress effects, D^0 is the nominal delay of the gate without any electrical variations, and the partial derivatives of delay with μ_i and $V_{th,i}$ denote the delay sensitivity of the gate to the mobility and threshold voltage, respectively, of transistor i, computed at the nominal point. For better accuracy, we store the piece-wise sensitivity of delay for different ranges of mobility shifts (from -50% to 50% with steps of 25%) and threshold voltage shifts (for every 40mV up to 80mV).

The leakage power of a transistor exponentially increases (decreases) with its decreasing (increasing) threshold voltage. However, for small changes in threshold voltage of a transistor, the gate-level leakage power varies almost linearly. As seen in Figure 7, the range of threshold voltage for NMOS and PMOS transistors in a minimum sized inverter can be upto few millivolts. The combined STI+TSV-induced threshold voltage variations in transistors are typically few tens of millivolts, while the nominal threshold voltage of a transistor is about 400 mV in this work. Thus the leakage power of a gate under unequal changes in threshold voltages of n transistors of a gate can also be computed using a first order Taylor series expansion as:

$$L_{gate}^{str} = L_{gate}^{0} + \sum_{i=1}^{n} \frac{\partial L_{gate}}{\partial V_{thi}}\bigg|_0 \Delta V_{thi}^{str} \quad (15)$$

where L_{gate}^{str} is the leakage power of a gate under STI-induced and/or TSV-induced stress and L_{gate}^{0} is the nominal leakage power of the gate under no stress. The partial derivative of L_{gate} with V_{thi} represents the sensitivity of the leakage current of the gate to changes in the threshold voltage of transistor

i, evaluated at the nominal point. For better accuracy, we use piece-wise sensitivity for threshold voltage shifts between different ranges (every 40mV) of threshold voltage shifts. Our relative error in computing leakage power of standard cells in this work is under 1%.

For a given placement, we use the analytical framework developed so far to compute the circuit performance as follows:

- From the layout information for a circuit, we recover the STI configuration affecting the transistors within each standard cell. We then compute the stress using the models in Section II. In 3D-ICs, we linearly superpose the contributions from different TSVs in the layout with the STI contribution. In planar 2D-ICs, STI is the dominant source of stress. The STI-induced stress and strain components are computed using Equation (9). On the other hand, in 3D-IC circuits, both STI and TSV act as stressors and the resultant stress/strain components are evaluated using Equation (10).
- Based on the stress computations, we then proceed to compute the changes in mobility and threshold voltage for every transistor using Equations (11) and (13), respectively.
- Knowing the changes in electrical parameters of individual transistors in a logic gate, we compute the delay and leakage power using Equations (14) and (15), respectively.
- We then perform static timing analysis and leakage computation to evaluate changes in path delays and circuit leakage power, respectively.

V. Results

Both STI-induced and TSV-induced stress contributions are layout dependent and depend upon the relative placement of the transistors with respect to the stressors. Note that we model the exact layout conditions to compute the stress in the transistor channels and do not rely upon the extreme scenarios. The stress is translated into changes in transistor electrical parameters which are in turn used to evaluate changes in gate delay and leakage power. The STI-induced and TSV-induced stress models are presented in Section II. The changes in transistor electrical parameters are subsequently translated into the changes in gate performance metrics as delineated in Section III and Section IV, respectively. In this section, we present circuit performance variations in planar 2D-ICs [3D-ICs] due to STI-induced [STI+TSV-induced] stress. We implemented the techniques in this work in C++, and the circuit performance analysis is done on a 64-bit Red-Hat Server with 3.4 GHz Intel® Core™i7-3700 processor.

We apply our techniques on a set of IWLS benchmarks in 45nm, 32nm, and 22nm technology nodes. We use 45nm Nangate standard cell library as a reference and scale the dimensions of the transistors and the layouts of the standard cells using standard Dennard scaling rules for 32nm and 22nm. We first present the impact of STI alone in planar circuits and later add the effects of TSVs in 3D-ICs on 22nm circuits. The attributes of the benchmark circuits are shown in Table VI. We use Capo [26] to place the circuits. Note that the placement of the standard cells is different between 45nm, 32nm, and 22nm layouts. For the purpose of demonstrating the effects of TSV-induced stress, we consider the entire circuit resides in a single tier of a 3D-IC. We place the 22nm circuits about a regular grid of TSVs. The TSV dimensions are chosen based on the work in [23]. In general, the methods presented in this work are applicable to multiple tier 3D-IC placements too. The average time taken to evaluate the stress from both STI and TSV using analytical models is about 3.4ms for each standard cell logic gate within the inner loop of the static timing analysis engine. Thus, using the analytical models, it would take about 92s to evaluate the stress in the entire layout for the largest benchmark circuit ethernet with about 27K gates. In the rest of the section, the terms Di and Li [ΔDi and ΔLi] denote the nominal [stress-induced changes in] path delay and circuit leakage power, respectively, corresponding to the ith circuit-level analysis.

TABLE VI
IWLS circuit benchmarks

Circuit	Index	# Gates	Height × Width (μm×μm)		
			45nm	32nm	22nm
ac97_ctrl	C1	9047	134×180	96×83	67×58
aes_core	C2	11346	149×131	107×92	75×64
des	C3	4443	93×110	67×58	47×40
ethernet	C4	27060	230×201	165×141	115×98
i2c	C5	1110	47×42	34×30	24×21
mem_ctrl	C6	8860	132×117	95×82	66×57
pci_bridge32	C7	9988	139×156	100×86	70×60
spi	C8	3216	79×88	57×50	40×34
systemcdes	C9	2600	71×85	51×45	36×31
usb_funct	C10	10667	145×127	104×89	73×62

A. Effects of STI-induced stress in planar circuits

Shallow trench isolation lies in the immediate vicinity of the transistor and can affect the transistor delays of circuits by modulating its electrical parameters. The effects of STI on circuit critical path delay and leakage power in 45nm, 32nm, and 22nm layouts are shown in Table VII. The columns of the table are described below:

- **45nm layouts**: The columns $D1$ and $L1$ correspond to the nominal circuit critical path delay and circuit leakage power, respectively, when STI effects are not taken into account. The columns denoted by $\Delta D1$ and $\Delta L1$ represent the changes in circuit critical path delay and circuit leakage power, respectively due to STI-induced stress effects. From the table, the changes in critical path delay [circuit leakage power] attributed to STI effects in 45nm layouts can range from -3.3% to 5.0% [12.1% to 19.6%].
- **32nm layouts**: The columns denoted by $D2$ and $L2$ correspond to the circuit critical path delay and circuit leakage power, respectively, when STI effects are not taken into account. The columns $\Delta D2$ and $\Delta L2$ represent the changes in circuit critical path delay and circuit leakage power, respectively due to STI-induced stress effects. In 32nm circuits, the changes in critical path delay [circuit leakage power] attributed to STI effects can range from -3.1% to 5.6% [9.1% to 14.6%].
- **22nm layouts**: The columns $D3$ and $L3$ represent circuit critical path delay and circuit leakage power, respectively, when STI effects are not taken into account. The columns

denoted by $\Delta D3$ and $\Delta L3$ denote the changes in circuit critical path delay and circuit leakage power, respectively due to STI-induced stress effects in 22nm layouts. From the table, the ranges of changes in critical path delay [circuit leakage power] attributed to STI effects are:-1.4% to 3.2% [16.8% to 20%].

From Table VII we can conclude that:

- The improvements [degradations] in critical path delay changes can be attributed to comparatively greater longitudinal STI [transverse STI] than transverse STI [longitudinal STI] on the standard cells of the critical path. Moreover, as evidenced in Section III-C, the magnitudes of delay improvements are due to the PMOS transistors on the critical path since PMOS transistors alone experience STI-induced mobility improvements in addition to threshold voltage improvements. Moreover, the improvements in NMOS threshold voltage may offset the STI-induced mobility degradations.
- The increase in circuit leakage power can be attributed to the reduction in PMOS and NMOS threshold voltages as seen in Section III-C.

To gain more insight into the delay variations due to STI-induced stress, it is instructive to observe the maximum and minimum changes in delay in the circuits. Table VIII shows the maximum and minimum changes in the 45nm, 32nm, and 22nm circuits. The description of the table and ranges of magnitudes of maximum and minimum changes in path delay can be summarized as follows:

- 45nm layouts: The column denoted by $\Delta D4$ [$\Delta D5$] represents the maximum [minimum] delay change on a path due to STI effects, while the column denoted by $D4$ [$D5$] refers to the delay of the corresponding path when no STI effects are taken into account. The maximum [minimum] changes in path delay can range from 1.1% to 15.7% [-5.0% to -11.5%].
- 32nm layouts: The columns denoted by $\Delta D6$ [$\Delta D7$] and $D6$ [$D7$] represent the maximum [minimum] change in path delay due to STI-induced stress and path delay under no STI effects, respectively. The maximum [minimum] changes in path delay in 32nm circuits can range from 2.9% to 12.1% [-5.7% to -11.1%].
- 22nm layouts: The columns denoted by $\Delta D8$ [$\Delta D9$] and $D8$ [$D9$] represent the maximum [minimum] change in path delay due to STI-induced stress and path delay under no STI effects, respectively. The maximum [minimum] changes in path delay in 22nm circuits can range from 2.5% to 11.7% [-6.0% to -28.6%].

By comparing the path delays in columns $D4$ and $D5$ of 45nm circuits in Table VIII with that of the critical path delay $D0$ in Table VII, we can conclude that the maximum or minimum changes in path delay can be significant and can occur on paths other than the critical path. Thus, it is imperative to take STI-induced stress effects into account while evaluating circuit performance. Similar observations can be made on 32nm and 22nm circuits.

Comparison with 1D STI models: To demonstrate the inaccuracies in using 1D STI models presented in prior works, we present the error in evaluating circuit critical path delay and circuit leakage power by considering longitudinal STI alone in Table IX. The columns $\Delta D10$, $\Delta D11$, and $\Delta D12$ [$\Delta L10$, $\Delta L11$, and $\Delta L12$] denote the error in critical path delay [circuit leakage power] by consider longitudinal STI alone in 45nm, 32nm, and 22nm circuits, respectively, compared to the actual STI model taking into account the STI from both longitudinal and transverse directions. The circuit critical path delay [circuit leakage power] with both longitudinal and transverse STI taken into account in 45nm, 32nm, and 22nm layouts can be obtained from columns $Dk(1 + \Delta Dk)$ [$Lk(1 + \Delta Lk)$] for $k \in \{1, 2, 3\}$, respectively in Table VII. The magnitude of error in 45nm, 32nm, and 22nm layouts in evaluating critical path delay [circuit leakage power] using 1D STI models can range from -2.5% to -5.5%, -2.1% to -4.6%, and -0.1% to 5.4% [-4.9% to -12.9%, -4.7% to -7.6%, and -4.5% to -8.4%] respectively.

The negative magnitude of error in evaluating in critical path delay and circuit leakage power in Table VII, indicates that 1D STI models overestimate the delay improvements and underestimate the leakage power changes. This is because when longitudinal STI effects alone are considered, PMOS mobility improvements alone are taken into account as seen from Figure 6(a) in Section III-C. Furthermore, it can be seen from Figure 7 that threshold voltage improvements are proportional to the STI surrounding the transistor in the layout. Thus, smaller magnitudes of threshold voltage improvements are predicted by the 1D STI model compared to the 3D STI model leading to smaller magnitudes of circuit leakage power.

B. Effects of STI+TSV on 3D-IC circuits

In 3D-IC circuits employing TSVs, both STI-induced stress and TSV-induced stress contribute to circuit performance variations. To demonstrate the combined effects of STI and TSV on circuit performance, we consider the 22nm circuits with a regular array of TSVs inserted in the layout. In addition, we consider two different TSV technologies with a TSV diameter of 5μm and a scaled diameter of 1μm. In both cases, the TSV spacing is chosen such that no more than 15% of the layout is occupied by TSVs. We apply our methods described in this paper to two sets of layouts TSV_5μ_22 and TSV_1μ_22 whose attributes are:

- **TSV_5μ_22 layout:** The TSVs have a diameter of 5μm and a liner thickness of 125nm. The TSV cells have a dimension of 7μm$\times$7μm and they are regularly spaced apart by 7μm.
- **TSV_1μ_22 layouts:** The TSVs have a diameter of 1μm with a liner thickness of 80nm. The TSV cells have a dimension of 1.4μm$\times$1.4μm and they are regularly spaced apart by 2.8μm.

In both the TSV_5μ_22 and TSV_1μ_22 layouts, both STI and TSVs act as stressors and the magnitude of stress in transistor channels depends upon the relative placement of the devices. The layout-dependent stress from both STI and TSVs are computed using Equation (10) and we evaluate the circuit performance outlined in Section IV. The circuit performance variations for the TSV_5μ_22 layouts are presented in

TABLE VII
EFFECTS OF STI ON PLANAR CIRCUITS

Circuit	45nm (vdd = 1.0 V)				32nm (vdd = 0.9 V)				22 (vdd = 0.8V)			
	$D1$ (ps)	$L1$ (μW)	$\Delta D1$ (%)	$\Delta L1$ (%)	$D2$ (ps)	$L2$ (μW)	$\Delta D2$ (%)	$\Delta L2$ (%)	$D3$ (ps)	$L3$ (μW)	$\Delta D3$ (%)	$\Delta L3$ (%)
C1	428	298	-3.3%	13.0%	564	269	-2.7%	12.6%	355	584	0.0%	18.7%
C2	417	226	2.6%	12.1%	488	295	-2.3%	9.1%	293	440	0.3%	16.8%
C3	870	177	0.6%	15.0%	1036	149	1.3%	13.6%	650	355	3.2%	20.0%
C4	643	562	1.6%	12.5%	760	625	-2.5%	11.9%	505	1097	-1.2%	17.3%
C5	388	35	2.3%	13.2%	510	33	-2.5%	13.0%	303	69	-1.0%	19.5%
C6	842	251	-0.1%	13.1%	1007	227	0.6%	14.6%	691	487	-0.3%	19.4%
C7	635	325	-0.2%	12.7%	771	335	-3.1%	9.8%	506	639	1.6%	19.3%
C8	692	117	1.0%	14.0%	768	99	5.6%	14.2%	629	241	-1.4%	19.7%
C9	694	117	5.0%	19.6%	814	97	-2.6%	12.8%	492	233	0.4%	19.9%
C10	624	248	2.4%	12.4%	801	266	-2.5%	12.0%	484	482	1.0%	18.3%

TABLE VIII
DELAY CHANGES UNDER STI-INDUCED STRESS EFFECTS

Circuit	45nm (vdd = 1.0V)				32nm (vdd = 0.9V)				22nm (vdd = 0.8V)			
	$D4$ (ps)	$\Delta D4$ (%)	$D5$ (ps)	$\Delta D5$ (%)	$D6$ (ps)	$\Delta D6$ (%)	$D7$ (ps)	$\Delta D7$ (%)	$D8$ (ps)	$\Delta D8$ (%)	$D9$ (ps)	$\Delta D9$ (%)
C1	108	15.7%	381	-8.7%	126	6.8%	90	-11.1%	271	11.1%	185	-28.6%
C2	173	2.9%	336	-9.5%	33	12.1%	129	-6.2%	168	8.9%	192	-15.6%
C3	354	2.0%	568	-8.1%	292	4.1%	265	-6.4%	492	6.5%	364	-17.9%
C4	434	1.6%	496	-8.9%	252	4.4%	189	-5.8%	252	9.1%	297	-17.5%
C5	192	10.4%	356	-9.0%	136	4.4%	123	-5.7%	249	6.8%	174	-6.9%
C6	473	1.3%	731	-8.1%	234	4.7%	162	-11.1%	230	11.7%	332	-14.8%
C7	350	1.1%	538	-11.5%	148	6.1%	186	-7.5%	252	8.3%	239	-18.4%
C8	476	2.7%	540	-8.1%	279	2.9%	218	-7.8%	448	2.5%	381	-6.0%
C9	458	2.6%	622	-5.0%	291	3.8%	215	-6.5%	305	4.6%	366	-9.8%
C10	289	1.7%	460	-8.3%	102	7.8%	172	-7.6%	377	5.6%	279	-20.1%

TABLE IX
ERROR IN USING 1D STI MODEL

Circuit	45nm (vdd = 1.0V)		32nm (vdd = 0.9 V)		22nm (vdd = 0.8V)	
	$\Delta D10$ (%)	$\Delta L10$ (%)	$\Delta D11$ (%)	$\Delta L11$ (%)	$\Delta D12$ (%)	$\Delta L12$ (%)
C1	-5.5%	-7.4%	-4.4%	-6.8%	-3.4%	-7.4%
C2	-4.4%	-4.9%	-2.1%	-4.7%	-1.4%	-4.7%
C3	-2.5%	-9.1%	-3.6%	-7.5%	-5.4%	-8.3%
C4	-4.3%	-4.9%	-3.2%	-4.9%	-0.4%	-4.5%
C5	-4.8%	-7.2%	-3.4%	-6.8%	-0.7%	-7.8%
C6	-3.0%	-6.7%	-4.5%	-6.8%	-0.1%	-7.2%
C7	-3.3%	-7.0%	-3.3%	-5.8%	-1.9%	-7.5%
C8	-2.6%	-8.1%	-3.5%	-7.6%	-1.0%	-7.8%
C9	-5.2%	-12.9%	-2.9%	-7.6%	-0.4%	-8.4%
C10	-4.9%	-5.5%	-4.6%	-5.8%	-1.6%	-5.8%

Table X. The nominal circuit critical path delay and leakage power with no stress effects are shown in columns $D3$ and $L3$, respectively, in Table VII. In Table X, the column denoted by $\#TSVs$ represents the number of TSVs in the layout. The columns $\Delta D13$ and $\Delta L13$ [$\Delta D14$ and $\Delta L14$] correspond to changes in circuit critical path delay and circuit leakage power, respectively, under STI-induced [TSV-induced] stress alone. The columns denoted by $\Delta D15$ and $\Delta L15$ represent the changes in circuit critical path delay and leakage power, respectively, when both STI-induced and TSV-induced stress effects are taken into account. The column $\Delta D16$ [$\Delta D17$] corresponds to the maximum [minimum] change in path delay under combined STI+TSV effects, while the column $D16$ [$D17$] denotes the nominal path delay when no stress effects are taken into account. It should be noted that stress tensor contributions from different stressors i.e., STI and TSV, must first be superposed before computing changes in circuit performance as outlined in this paper. We refer to this as the $\sum \sigma$ approach. However, if the resultant changes in gate delay or gate leakage power due to different stressors are separately computed and summed together, it may lead to inaccurate estimation of circuit performance. We refer to the latter approach as $\sum \Delta p$ method, indicating that the changes in circuit performance Δp from different sources of stress are summed together while evaluating circuit performance. In Table X, the column denoted by $E_{\sum \Delta d}$ [$E_{\sum \Delta l}$] represents the error in estimating circuit critical path delay [circuit leakage] by adding the respective changes in gate delay [gate leakage] due to STI and TSV, instead of stress superposition followed by circuit evaluation. From the table, we observe that:

- The magnitudes of changes in circuit critical path delay and leakage power under STI-only [TSV-only] stress effects in the TSV_5μ_22 layouts can range from -3.0% to 1.6% [-1.0% to 0.3%] and from 17.5% to 19.0% [5.1% to 7.0%], respectively.
- The changes in critical path delay and leakage power due to combined effects of STI-induced and TSV-induced stress effects can range from -5.6% to 1.6% and from 34.8% to 43.5%, respectively. The maximum [minimum] changes in path delay can range from 11.4% to 31.2% [-10.7% to -36.4%].
- The magnitude of error in estimating circuit critical path delay [circuit leakage power] under the $\sum \Delta p$ approach compared to $\sum \sigma$ approach can range from -1.7% to 3.5% [-8.2% to -12.8%]. The positive [negative] magnitude of error indicates overestimation [underestimation] of circuit performance metrics. Note that the critical paths can be different between $\sum \Delta p$ and $\sum \sigma$ approaches.

From the above observations, we can conclude that:

- By comparing the magnitudes of changes in circuit critical path delay and leakage power under STI-induced, TSV-induced, and STI+TSV-induced stress effects, it can be seen that circuit performance changes due to the combined STI+TSV effects is not a linear sum of STI-

TABLE X
EFFECTS OF STI+TSV ON TSV_5μ_22 LAYOUTS

Circuit	#TSVs	STI effects		TSV effects		STI+TSV effects							
		σ_{STI}		σ_{TSV}		$\sum\sigma = \sigma_{STI} + \sigma_{TSV}$						$\sum\Delta p$	
		$\Delta D13$ (%)	$\Delta L13$ (%)	$\Delta D14$ (%)	$\Delta L14$ (%)	$\Delta D15$ (%)	$\Delta L15$ (%)	$D16$ (ps)	$\Delta D16$ (%)	$D17$ (ps)	$\Delta D17$ (%)	$E_{\sum\Delta d}$ (%)	$E_{\sum\Delta l}$ (%)
C1	50	-1.4%	18.2%	-0.3%	5.4%	-3.9%	35.7%	327	31.2%	154	-36.4%	1.5%	-8.9%
C2	66	-2.7%	17.5%	0.3%	5.8%	-2.0%	36.3%	296	17.9%	114	-34.2%	-1.7%	-9.5%
C3	21	-1.7%	18.7%	-0.6%	5.7%	-3.4%	38.0%	522	11.5%	356	-27.0%	1.3%	-9.8%
C4	153	-0.6%	18.1%	0.2%	5.8%	-3.2%	36.8%	374	27.3%	222	-26.1%	1.0%	-9.5%
C5	6	-1.0%	18.2%	-0.3%	7.0%	-2.3%	43.5%	234	20.5%	201	-14.4%	1.0%	-12.8%
C6	50	-3.0%	18.7%	-0.1%	5.1%	-5.2%	34.8%	465	15.1%	288	-26.7%	1.4%	-8.2%
C7	60	1.6%	18.3%	-0.2%	5.3%	1.6%	34.8%	327	28.1%	241	-24.5%	-0.6%	-8.3%
C8	18	-1.3%	18.7%	-0.8%	5.4%	-4.3%	36.2%	316	11.4%	372	-18.5%	1.3%	-8.8%
C9	15	-0.2%	19.0%	-0.6%	6.1%	-1.8%	39.9%	339	12.7%	419	-10.7%	1.2%	-10.6%
C10	66	-1.2%	17.9%	-1.0%	5.7%	-5.6%	36.2%	292	22.6%	271	-30.3%	3.5%	-9.3%

only and TSV-only stress effects. Thus, when analyzing layout-dependent stress in 3D-ICs, we must first superpose the STI-induced and TSV-induced stress and then evaluate the circuit performance.

- By comparing the ranges of maximum and minimum changes in path delay i.e., columns $\Delta D16$ and $\Delta D17$, respectively, with that of the changes in critical path delay we can conclude that paths other than the critical path can undergo significant changes in path delay.
- In the $\sum\Delta p$ approach, the circuit path delay may be overestimated or underestimated compared to the true $\sum\sigma$ approach. Moreover, the leakage power of the circuit is underestimated in the $\sum\Delta p$ approach. This is because, the magnitude of change in transistor threshold voltage by superposing stress from STI and TSV is larger than individual changes in threshold voltage due to STI-induced and TSV-induced stress alone. Since leakage power is an exponential function of transistor threshold voltage, it can result in underestimation when individual leakage contributions from STI-induced and TSV-induced stress effects are summed together.

In the interest of space, rather than providing a full table, we summarize the effects of STI-induced and TSV-induced stress on TSV_1μ_22 layouts as follows:

- The corresponding number of TSVs in the TSV_1μ_22 layouts labelled C1 through C10 are: 525, 663, 240, 1560, 60, 510, 576, 168, 126, and 592. The TSV_1μ_22 layouts have a larger number of TSVs compared to that of TSV_5μ_22 layouts, shown in column #TSVs of Table X, due to the relatively smaller size of TSVs.
- The magnitudes of changes in circuit critical path delay and leakage power under STI-induced [TSV-induced] stress effects in the 22nm 3D-IC layouts can range from -2.5% to $0\%\%$ [-0.8% to 0.8%] and from 16.9% to 19.1% [3.2% to 4.1%], respectively.
- The combined effects of STI-induced and TSV-induced stress, using $\sum\sigma$ approach, in the TSV_1μ_22 layouts on circuit critical path delay [circuit leakage power] can range from -5.5% to 2.3% [27.8% to 31.6%]. The maximum [minimum] changes in path delay can range from 3.8% to 14.4% [-9.0% to -26.4%].
- The magnitude of error in estimating circuit critical path delay [circuit leakage power] using $\sum\Delta p$ approach compared to $\sum\sigma$ approach can range from -3.0% to 2.2% [-4.8% to -7.3%]. Here negative [positive] magnitude of error indicates underestimation [overestimation] of the corresponding circuit performance metric.

Based on the observations in TSV_1μ_22 layouts, we can conclude the following:

- Similar to TSV_5μ_22 layouts, the combined effects of STI+TSV-induced stress effects on circuit performance of TSV_1μ_22 layouts can be significant compared to when STI-induced or TSV-induced stress effects alone are taken into account.
- The TSVs of diameter 1μm induces a smaller magnitude of stress compared to TSVs of 5μm diameter [13]. However, owing to smaller size of TSVs in the TSV_1μ_22 layouts, more number of TSVs can be packed into the layout and can result in similar shifts in circuit performance compared to TSV_5μ_22 layouts.
- Using $\sum\Delta p$ approach can lead to underestimation or overestimation in circuit critical path delay; the leakage power is underestimated. In addition, the critical path under the erroneous $\sum\Delta p$ approach can be different than the stress superposition approach.

Finally, to consider the importance of our combined analysis over separate STI- or TSV-stress-based analysis, we ranked the top 500 critical paths between STI-only, TSV-only and STI+TSV analysis runs for each of the benchmark circuits in the TSV_5μ_22 circuits. By comparing the critical paths and their corresponding rank, we reach the following conclusions:

- For the TSV_5μ_22 circuits, the number of unique paths that appear in the top 500 critical paths of the STI+TSV analysis compared to STI-only [TSV-only] analysis can range from 4.8% to 97.4% [9.4% to 37%]. The corresponding numbers for the TSV_1μ_22 circuits were from 6.4% to 94.6% [6.8% to 58.0%].
- For the TSV_5μ_22 circuits, the number of paths with identical ranks between STI+TSV and STI-only [TSV-only] analysis can range from 0.2% to 5.8% [0% to 2.6%]. The corresponding numbers for the TSV_1μ_22 circuits were 0% to 4.6% [0% to 3.2%]

Thus, to accurately evaluate the circuit performance variations due to layout dependent STI-induced and TSV-induced stress effects, the stress/strain tensor components from respective sources of stress must first be superposed.

VI. Conclusion

We have presented an approach for analyzing the circuit-level impact of unintentional stress, caused by differential coefficients of thermal expansion between both STI and TSVs and their surrounding materials. An accurate model for STI-related stress is proposed. It is shown that STI-induced stress in 2D circuits can cause significant shifts in performance, and in 3D circuits, this stress in conjunction with TSV-induced stress plays an important role. The electrical shifts cannot be obtained by superposing the corresponding shifts due to STI and TSV alone; instead, the stress components must be superposed and translated to obtain the circuit-level shift.

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