# Incorporating Hot Carrier Injection Effects into Timing Analysis for Large Circuits

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***Abstract*—This paper focuses on hot carrier (HC) effects in modern CMOS technologies and proposes a scalable method for analyzing circuit-level delay degradations in large digital circuits, using methods that take abstractions up from the transistor level to the circuit level. We begin with an exposition of our approach for the nominal case. At the transistor level, a multi-mode energy-driven model for nanometer technologies is employed. At the logic cell level, a methodology that captures the aging of a device as a sum of device age gains per signal transition is described, and the age gain is characterized using SPICE simulation. At the circuit level, the cell-level characterizations are used in conjunction with probabilistic methods to perform fast degradation analysis. Next, we extend the nominal-case analysis to include the effect of process variations. Finally, we show the composite effect of these approaches in the presence of other aging variations, notably bias temperature instability (BTI), and study the relative impact of each component of aging on the temporal trends of circuit delay degradations. The analysis approaches for nominal and variational cases are both validated by Monte Carlo simulation on various benchmark circuits, and are proven to be accurate, efficient and scalable.**

***Index Terms*—Hot Carrier Effects, Timing Analysis, Circuit Reliability, Aging, Process Variations, Bias Temperature Instability**

## I. Introduction

HOT carrier (HC) effects in MOSFETs are caused by the acceleration of carriers (electrons or holes) under lateral electric fields in the channel, to the point where they gain high enough energy and momentum (and hence they are called *hot* carriers) to break the barriers of surrounding dielectric, such as the gate and sidewall oxides [1]. The presence of hot carriers triggers a series of physical processes that affects the device characteristics under normal circuit operation. These effects cumulatively build up over prolonged periods, causing the circuit to age with time, resulting in performance degradations that may eventually lead to circuit failure.

The phenomenon of HC effects is not new: it was a significant reliability issue from the 1970s to the 1990s, when circuits operated under high supply voltages (2.5–5V), which led to a high lateral electric field in the MOSFET channel. The effects of HCs were mitigated by the introduction of special process techniques such as lightly doped drains (LDDs). The traditional theory of HC mechanisms was based on a field-driven model, in which the peak energy of carriers (electrons or holes) is determined by the lateral field of the channel [2]. This was based on the theory of the so-called lucky electron model, capturing the confluence of events due to which an electron is "lucky" enough to do damage – to gain energy from the channel field, to be redirected towards the silicon/oxide interface, and to avoid energy-robbing collisions along the way.

Extrapolating this theory, it was expected that at today's supply voltages, HC effects would almost disappear as carriers cannot gain enough energy when the electric field is reduced to these levels. However, experimental evidence on nanoscale technologies shows that this is not true, and hot carrier degradation remains significant for MOSFETs at lower voltages [3]. Moreover, these issues are projected to worsen in future generations of devices.

The rate of hot carrier generation increases with time $t$ as $t^{1/2}$. Since the multiplicative constant for this proportionality is relatively small, in the short-term, HC effect is overshadowed by bias temperature instability (BTI) effects, which increase as $t^n$, for $n \approx 0.1$–$0.2$, but with a larger constant multiplier. However, in the long term, the $t^{1/2}$ term dominates the $t^n$ term, making HC effects particularly important for devices in the medium to long term. It has been shown in [4], for example, that HC effects can contribute to 40-80% of all aging after 10 years of operation. Therefore, HC effects are a significant factor in the short term and are dominant in applications with longer lifetimes, such as embedded/automotive applications and some computing applications.

Recently, newer energy-driven theories [5]–[7] have been introduced to overcome the limitations of the lucky electron model, and to explain the mechanism of carriers-induced degradation for short-channel devices at low supply voltages. These theories have been experimentally validated on nanometer-scale technologies. The energy-driven framework includes the effects of electrons of various levels of energy, ranging from high-energy *channel hot carriers* (CHCs) to low-energy *channel cold carriers* (CCCs). Under this model, injection is not necessary for the device degradation, and carriers with enough energy can affect the Si–$SiO_2$ interface directly. However, much of the published circuit-level work on HC effects is based on the lucky electron model, which is effectively obsolete.

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Existing work on HC degradation analysis of digital circuits can be divided into to two categories. The first is based on device-level modeling/measurement tied to circuit-level analysis, including [8], commercial software such as Eldo using computationally-intensive simulations, and [4], which predicts the lifetime of a ring oscillator using measured data. While these methods are flexible enough to accept new models and mechanisms, they are not scalable for analyzing large circuits.

Methods in the second category are based on a circuit-level perspective, using statistical information about device operation to estimate the circuit degradation. In [9], a hierarchical analysis method for delay degradation, based on a simple device-level HC model, was proposed. The work in [10] defined a duty factor to capture the effective stress time for HC effects, which assumes constant HC stress during signal transitions and models the duty factor to be proportional to the transition time. The characterization of HC degradation is performed in the device level and only considers the switching transistors, with other transistors in the stack ignored. Then signal probability (SP) and transition density (TD) is utilized for aging analysis. While these works are usually efficient and scalable to large digital circuits, they use over-simplistic models for device aging and cell characterization, and therefore cannot achieve the high accuracy provided by methods in the first category, especially for nanometer-scale technologies. Extending these methods to energy-driven models, including CHC and CCC, is highly nontrivial, and is certainly not a simple extension.

Beyond the issue of using better modeling techniques for analyzing the nominal case, it is also important to consider the effects of process variations, which significantly affect circuit timing in digital circuits [11] in current and future technologies. Since HC effects are closely dependent on the circuit operation and device stress conditions, they is also affected by process variations. The interaction between HC effects and process variations has gained increasing attentions in recent years. However, most of the published works only focus on device-level analysis [12], [13] or small-scale digital circuit [14], and the proposed methods are usually based on LEM model with HSPICE or Monte Carlo simulation, and are not scalable to large digital circuits. Statistical analysis of aging has also been considered in [15], [16], which focus purely on BTI aging. This paper addresses HC degradation and uses the Gaussian model for process variations and first-order model for timing degradation and constructs an efficient approach for HC degradation analysis that is scalable to large circuits.

This paper provides a third path for CHC/CCC degradation analysis for large digital circuits, and makes the following contributions:

- Instead of using a simple empirical degradation model [9], or a device model assuming constant stress during transition [10], our method is built upon the newer multi-mode energy-driven degradation model [6], [7].
- It introduces the novel concept of age gain (AG) to capture the amount by which a transistor ages in each signal transition, and develops a quasistatic approach for accurate analysis of AG.
- It performs cell-level characterization of AG, in which the AGs of all transistors in a logic cell corresponding to a signal transition event is computed simultaneously, instead of only considering switching transistors [10].
- It utilizes signal statistics, leveraged from techniques for power estimation, to perform circuit-level degradation analysis. The multilevel hierarchy of modeling and analysis enables both high accuracy and great scalability of the proposed approach.
- It demonstrates that the circuit delay degradation has a slight but negligible deceleration effect due to the degradation of signal transition, in contrast to the significant acceleration effect predicted in [10]. The work in [10] assumes HC aging to be proportional to the transition time, which increases with aging; however, this is not entirely accurate since slower transition times excite fewer energetic carriers and actually cause *less* damage.
- The proposed approach for circuit degradation analysis using the energy-driven model is extended at the cell-level modeling and circuit-level analysis to incorporate the impact of process variations on both device aging and circuit timing. The variation-aware circuit degradation analysis is fitted into the statistical static timing analysis (SSTA) framework, with good accuracy and scalability.

Our work bridges the wide chasm between the tremendous advances at the device level with the much simpler models that are currently used at the circuit level. Our approach maintains accuracy and scalability at all levels of design, employing accurate modeling and characterization at the device and cell levels, and a scalable algorithm at the circuit level. We begin with an approach for analyzing the nominal case, neglecting the effects of variations. At the *transistor level*, we employ the energy-driven model for device aging [6], [7], as outlined in Section II. At the *logic cell level*, we characterize (offline) the device age gain per signal transition for cells within a library using SPICE simulations, as described in Section III. At the *circuit level*, the signal probability and activity factor are utilized to perform fast degradation analysis, based on the cell-level characterization, as explained in Section IV. Next, we extend the engines developed above to include the impact process variations on both HC aging and circuit timing, as discussed in details in Section V. The proposed analysis approaches for both nominal and variational cases are validated by Monte Carlo simulation on various benchmark circuits, and is demonstrated in Section VI to be accurate, efficient and scalable. The paper ends by presenting concluding remarks in Section VII.

As in other work considering hot and cold carriers, we refer to the CHC/CCC problem under all energy modes as "hot carrier"/"HC" degradation, but it is implicit that the CCC case is also included.

## II. CHC/CCC Aging: Device Models

### A. Traditional Mechanisms

The traditional lucky electron model for HC degradation was based on *direct electron excitation* (DEE), i.e., the theory

of impact ionization and interface trap generation due to broken Si–H bonds [1], based on a set of chemical reactions. Let us denote the silicon-hydrogen bonds at the surface as $\equiv$ $\mathrm{Si}_s\mathrm{H}$, where the subscript $s$ denotes the surface, i.e., the oxide-substrate interface, with three other bonds ("$\equiv$") connected to other silicon atoms in the substrate, One of the reactions that causes HC injection involves trap generation by electrons ($e^-$) that breaks the silicon-hydrogen bond, i.e.,

$$\equiv \mathrm{Si}_s\mathrm{H} + e^- \quad \rightarrow \quad \mathrm{Si}^* + \mathrm{H} \tag{1}$$

Another is related to trap generation by electrons and holes ($h^+$) as they interact with hydrogen atoms ($H$) and molecules ($H_2$), i.e.,

$$\begin{aligned} e^- + h^+ + \mathrm{H}_2 \quad &\rightarrow \quad 2\mathrm{H} \\ \equiv \mathrm{Si}_s\mathrm{H} + \mathrm{H} \quad &\rightarrow \quad \mathrm{Si}^* + \mathrm{H}_2 \end{aligned} \tag{2}$$

It is also possible for holes to break the $\equiv \mathrm{Si}_s - \mathrm{H}$ bound.

### B. Energy-driven Mechanisms

From an energy perspective, hot electrons change the distribution of the electron energy distribution function (EEDF). The expression

$$\text{Rate} \; = \int f(E)S(E)dE \tag{3}$$

describes the hot carrier rate, where $f$, the EEDF, and $S$, the interaction cross section or scattering rate, are functions of energy $E$. It has been shown that the dominant energies associated with this integrand are at a set of "knee" points in either $f$ or $S$. There are four major mechanisms that affect the above rate [5], [6]:

- In the field-driven paradigm of the lucky electron model, $f$ has no significant knee, and the dominant energies are driven by the $S$ function. This is the first mechanism, and its effect is decreasing in nanometer-scale technologies.
- In addition, there are knees in the EEDF beyond the range of the lucky electron model. It has been shown that the EEDF has a significant knee at the point at which there is a steep potential drop at the drain, corresponding to the potential from the drain to the channel pinch-off point, $V_{EFF}$, and a second knee is seen at about $2V_{EFF}$ due to *electron-electron scattering* (EES).
- The third mechanism, linked to high-energy carriers, is through *single vibrational excitation* (SVE) due to energy transfer to the phonon system, adding to energy from lattice vibrations.
- Finally, there is evidence that the bonds may be broken by *channel cold carrier* (CCC) effects, through a fourth mechanism corresponding to *multiple vibrational excitation* (MVE). This corresponds to direct excitation of the vibrational modes of the bond by multiple carrier impacts, each of which individually have low energy, but which can cumulatively break the bond [17]. MVE degradation is strongly correlated to the current, i.e, the number of electrons "hitting" the bond per second.

The energy-driven theory for HC generation [6] uses quantum-mechanical models to explain the process of carriers gaining energy, through three different mechanisms: (1) *High-energy channel hot carriers* based on direct electron excitation (DEE), consistent with the Lucky Electron Model (LEM), and on the SVE mechanism, (2) *Medium energy electrons* based on the EES mechanism, and (3) *Channel cold carriers* based on the MVE mechanism, which creates lower-energy carriers that cause degradations.

### C. Device Aging Model

The degradations of the saturation drain current, $\Delta I_{\text{on}}/I_{\text{on}}$, of a transistor due to HC effects follow a power model [7]:

$$(\Delta I_{\text{on}}/I_{\text{on}})_j = A(\text{age}_j)^n \tag{4}$$

The exponent $n$ is widely accepted to be 0.5 over a range of processes. The value of $A$ can be obtained from device-level experiments, e.g., from the plots in [7]. The age function of a MOSFET is given by

$$\text{age} = t/\tau = R_{\text{it}}t \tag{5}$$

where $R_{\text{it}}$ can be interpreted as the *rate of aging* over time, and corresponds to the rate of interface trap generation. The quantity $\tau$ is its inverse and is referred to as the device lifetime. Over the years, considerable effort has been expended in characterizing $R_{it}$ at the device level. Under the classical field-driven LEM scenario, this has the form:

$$R_{\text{it(LEM)}} = \frac{1}{\tau} = K\left(\frac{I_{ds}}{W}\right)\left(\frac{I_{bs}}{I_{ds}}\right)^m \tag{6}$$

The more accurate multi-mode energy-driven model for HC degradation for fine-geometry CMOS devices changes this to [7]:

$$\begin{aligned} R_{\text{it}} = \frac{1}{\tau} \quad = \quad & C_1\left(\frac{I_{ds}}{W}\right)\left(\frac{I_{bs}}{I_{ds}}\right)^m + C_2\left(\frac{I_{ds}}{W}\right)^{a_2}\left(\frac{I_{bs}}{I_{ds}}\right)^m \\ & + C_3\, V_{ds}^{\frac{a_3}{2}}\left(\frac{I_{ds}}{W}\right)^{a_3}\exp\left(\frac{-E_{emi}}{k_BT}\right) \end{aligned} \tag{7}$$

The three terms in the expression correspond to degradation in the high-energy mode (corresponding to LEM), the medium-energy mode, and through channel cold carriers, respectively.

The relation between $R_{it}$ and $I_{ds}/W$ in Equation (6) is linear, and experimental data [6], [7] show that this is grossly incorrect. The nonlinear model in Equation (7) shows excellent fits to experimental measurements, and therefore our analysis is based on this model.

HC degradation has positive dependence on temperature, and a corner-based approach with worst-case temperature is used in this work. If more information about thermal characteristics is available, this model can easily be extended.

## III. Cell-level Characterization

The device-level models outlined in the previous section provide a means for computing the aging due to CHC/CCC effects. To determine their effects on the circuit, our approach begins by building a cell-level characterization technique for the standard cell library that computes the delay drift over time. The remainder of this section describes the precharacterization method: we begin by determining the aging effect on each transistor of a library cell, and then compute its effect on the cell delay.

### A. Transistor Age Gain Per Transition

For most of the time during the operation of a digital circuit, the MOS transistors in the circuit are in off or triode state, where there is minimal HC degradation. The period during which there is a sufficient number of carriers in the channel, with various levels of energy, corresponds to only the active (switching) state, and it is sufficient for only this state to be considered in analyzing HC degradation at the transistor level.

Therefore, HC aging does not occur over all time, and the defect generation rate function in Equation (7) becomes time-varying, and can be written as $R_{\text{it}}(t)$. Fig. 1 shows the $R_{\text{it}}(t)$ of the NMOS transistor in an inverter with a rising input signal: notice that the value is zero outside the transition, and contains non-zero components from medium energy and cold carriers over the period of transition. The medium energy component shows two peaks in the beginning and end of transition due to the peaks of $I_{bs}/I_{ds}$, while the cold carriers component has one peak near the end of transition due to the peak of $I_{ds}$. The active state of a logic cell can be characterized using the input signal transition time and output load capacitance. For example, a faster transition results in higher-energy carriers, while a slower transition to a larger load may result in a larger volume of lower-energy carriers.

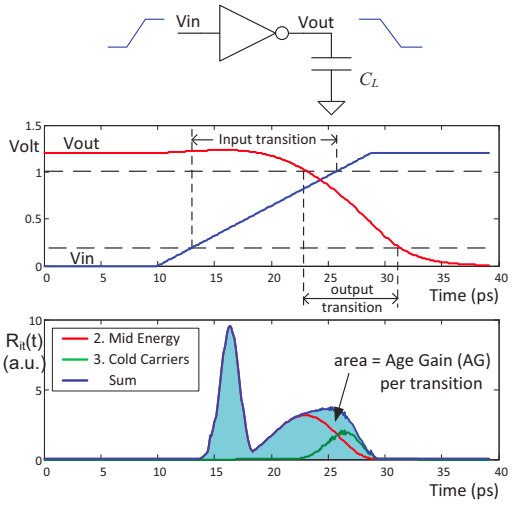


Fig. 1. An example that shows the age function, $R_{\text{it}}(t)$, during a signal transition of an inverter.

It is important to note that, unlike NBTI, HC effects do not experience recovery effects, and the application of HC stress results in monotone aging. We introduce a term, called the age gain (AG) per transition of a MOSFET, to capture the effect of degradation due to HC aging as a result of each transition that the MOSFET undergoes. The age function, which increases monotonically over the life of a device, is the sum of AGs of all transitions:

$$\text{age} = \sum_{\text{all transitions}} \text{AG} \tag{8}$$

We compute the AG using a a quasistatic approach: such methods have been accepted for HC analysis [18]. With this approach, the device AG over each transition period with time-dependent aging rate is computed as the integral of the aging rate function $R_{\text{it}}(t)$, as shown below,

$$\text{AG} = \int_{\text{tran}} R_{\text{it}}(t)\text{dt} \tag{9}$$

Here, tran stands for the interval of a specific transition, and $R_{\text{it}}(t)$ is defined in Equation (7) with time-dependent operation voltages and currents. The integral computes the age gain associated with one specific transition and uses the quasistatic approach to approximate the integral as a finite sum.

The paper uses simple ramps signal for age and timing characterization and does not include the case of non-monotonic transitions based on the following considerations: (1) non-monotonic transitions due to crosstalk from another signal means the transitions of these two signal happen at the same time, which is a relatively rare event; and (2) unlike timing analysis which focuses on the worst case, aging and degradation is a long term cumulative process so occasional random crosstalk only has limited effects (unless it happens regularly between two correlated signals). However it is feasible to extend the framework proposed in this paper to include the effect of non-monotonic signals due to crosstalk, as long as the typical non-monotonic input patterns can be provided for cell level characterization. Then at circuit level a probabilistic method can be utilized to calculate the circuit degradation under the random non-monotonic signals.

### B. Library Characterization

For a digital circuit, the AG calculations can be characterized at the cell-level as a part of library characterization. Under a specified input signal type (rise or fall), a transition time, and an output load capacitance, the time-varying voltages and currents of all MOS transistors inside the logic cell can be computed using SPICE transient analysis. The AG of each transistor is computed by the numerical integration of $R_{\text{it}}(t)$ in Equation (7), as given by (9).

Examining the procedure outlined above, it is easy to see that for library-based digital circuits, where all logic cells are from a cell library, the degradation of HC effect can be precharacterized for cells in the library and stored in a look-up table (LUT). Fig. 2 illustrates how a NAND2 cell may be characterized, by enumerating the signal input pin, the signal type, the transition time denoted as $tr$, and the output load denoted as $C_L$. Note that a transistor can experience age gain even if there is no transition on its gate input: for example, for a two-transistor NMOS pulldown in the NAND2 cell, a transition that turns on the upper input, while the lower input is already on, can cause an increase in AG for the lower transistor. We capture such effects in our model. For example, for each case shown in the figure with specified $tr$ and $C_L$, the AGs of all four transistors in the NAND2 cell are computed simultaneously.

The LUT of each cell $i$ outputs the AGs of all transistors $j$ inside the cell, and has five input parameters as expressed in Equation (10), where $k$ stands for the input pin with signal

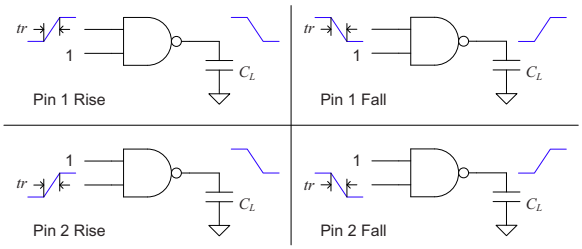


Fig. 2. Characterization of a NAND2 cell. The number of simulations required for characterization is identical to those of timing characterization.

transition[1], $r/f$ for the transition type (rise or fall), $inp$ for the input vector of the remaining input pins (if more than one input vector can make pin $k$ critical), $tr_k$ for the input transition time on pin $k$ and $C_L$ for the load capacitance.

$$\left\{\text{AG}_{j,k}^{r/f}\right\}_{j\in\text{cell } i} = \text{LUT}_{\text{AG}}(k, r/f, inp, tr_k, C_L) \tag{10}$$

**Characterization cost:** The number of simulations required to characterize AG is *identical* to that required for timing characterization: in fact, the same simulations are used, but additional currents/voltages are monitored, followed by a post-processing phase in which mathematical operations (such as numerically integration) are performed on this data to compute AG. Therefore, the number of simulations is $O(N_{\text{cell}})$, where $N_{\text{cell}}$ is the number of cells, and so is the storage complexity of the LUT.

The effect of aging on a transistor is to alter its saturation drain current $I_{\text{on}}$. This in turn affects key performance parameters such as the propagation delay and output signal transition time of a logic cell that the transistor lies in. Given that the aging perturbations are small, we use first-order models for these relationships, as is done in other variational methods [19]. The propagation delay $d_i$ and signal transition $tr_i$ of cell $i$ are modeled using the following linear relationship with the $\Delta I_{\text{on}}/I_{\text{on}}$ of transistors $j$ inside cell $i$:

$$d_i = d_{i0} + \sum_{j\in\text{cell } i} S_{ij}^{d}(\Delta I_{\text{on}}/I_{\text{on}})_j \tag{11}$$

$$tr_i = tr_{i0} + \sum_{j\in\text{cell } i} S_{ij}^{tr}(\Delta I_{\text{on}}/I_{\text{on}})_j \tag{12}$$

The propagation delay $d_i$, signal transition time $tr_i$, and their sensitivities $S_{ij}^{d}$ and $S_{ij}^{tr}$ to the transistor $\Delta I_{\text{on}}/I_{\text{on}}$ values are calculated using standard techniques. The sensitivity computations have been incorporated into design flows already, in the context of SSTA, and we use a very similar approach here. Take $S_{ij}^{d}$ for example, in our experiment it is characterized using following first-order approximation,

$$S_{ij}^{d} = \frac{d_i(\mu_j = 0.95\mu_0) - d_i(\mu_j = \mu_0)}{0.05}. \tag{13}$$

Here the approximation of mobility degradation $\Delta\mu/\mu = \Delta I_{\text{on}}/I_{\text{on}}$ is used for device model in SPICE analysis. As pointed out earlier, these correspond to the same SPICE simulations that are used for AG characterization, although different results are extracted from the simulations. The results are stored in LUTs, expressed as follows:

$$d_i = \text{LUT}_{d}(k, r/f, inp, tr_k, C_L) \tag{14}$$

$$\{S_{ij}^{d}\}_j = \text{LUT}_{S_d}(k, r/f, inp, tr_k, C_L) \tag{15}$$

$$tr_i = \text{LUT}_{tr}(k, r/f, inp, tr_k, C_L) \tag{16}$$

$$\{S_{ij}^{d}\}_j = \text{LUT}_{S_{tr}}(k, r/f, inp, tr_k, C_L) \tag{17}$$

As stated earlier, the computations of these LUTs has similar complexity as that of AG characterization. Moreover, there are established methods for computing each one of these, as they are used in variational/statistical analysis.

## IV. Circuit-Level Analysis of HC Degradation

Given a set of precharacterized cells, our task at the circuit level is to efficiently use this information to perform scalable circuit-level analysis using these accurate models. Our analysis consists of four steps, described in this section: first, finding the distribution of the signal transition time at each node; second, calculating the AG for all gates in a circuit, considering their context in the circuit; third, using this information to analyze device aging; and fourth, analyzing the delay degradation of the circuit.

### A. Distribution of Signal Transition Time

Due to the discrete nature and finite (but potentially large) number of signal paths in digital circuit, the signal transition time, $tr(q)$, at a certain node $q$ has a discrete probability distribution, $\Pr(tr(q))$, which is nonzero at all values of $tr(q) \in \mathbf{Tr^{(q)}}$, where $\mathbf{Tr^{(q)}}$ stands for the set of all possible $tr$ values of node $q$.

We assume that the signal transition times of the primary inputs is known (and assumed to be constant). The signal transition distribution of all internal nodes can be calculated either using Monte Carlo simulation, or using a probabilistic method. Here, we introduce a transition propagation (TP) method to calculate the transition time distribution (rise and fall separately) at each node, which is similar in spirit as static timing analysis (STA), but calculates the complete distribution information of transition time using signal probability (SP) and activity factor (AF), instead of just solving for the longest delay and transition time, as in conventional STA.

As each gate $q$ is processed in topological order, given the distribution of transition times at each input pin of the gate, we use the $\text{LUT}_{tr}$ in Equation (16) to compute the distribution of $tr(q)$ at the output. A single transition at the output of $q$ can be triggered under a number of different logical input conditions. We enumerate these conditions for each gate, which correspond to enumerating, for each input pin $k$, the set

[1]As in static timing analysis, we operate under the single input switching (SIS) assumption, i.e., the signal transition for a logic cell is triggered by one signal. This can be extended to the multiple input switching (MIS) scenario, where more than one signal arrives during the transition using methods similar to those used for timing characterization. However, given that the age function is computed cumulatively over long periods of time and that the probability of MIS is typically much lower than that of SIS, the SIS assumption gives an adequate level of accuracy. Further improvements in accuracy here are likely to be overshadowed by modeling errors at the device level.

of noncontrolling inputs that allow a transition at $k$ to become a transition at $q$. Under each condition, we compute $tr(q)$ using $\text{LUT}_{tr}$, and $\Pr(tr(q))$ using the activity factor (AF) of the corresponding input transition and the signal probability (SP) of the nontransitioning inputs.

The enumeration over all patterns on a gate is not expensive for a gate with a reasonable number of inputs; however, we must also perform an enumeration over all transition times. In principle, this could lead to state explosion as the number of possible elements of $\mathbf{Tr}^{(\mathbf{q})}$ are enumerated. To control this, we use data binning to reduce the number of data points that represent the distribution by approximating it with a discrete distribution over a smaller number of points, denoted as $\mathbf{Tr_s}$. We find that the error due to this approximation is negligible.

*Theoretically*, it is necessary to analyze the distribution of $tr$ at each circuit node and to use this result for AG calculation. However, as will be shown in Section VI-A, the error of using a single value of $tr$ from STA result is very small compared with using this full $tr$ distribution, since this is already a second-order effect; moreover, the actual distribution of $tr$ tends to have a small standard deviation and the $tr$ from STA result gives a close approximation. In the following work (e.g., the variation-aware analysis in Section V-D) the value of $tr$ from STA can be used safely to reduce complexity.

### B. Mean AG Calculation in Digital Circuits

As discussed in Section III-A, device aging in a library cell is modeled using age gain per transition $\text{AG}_{j,k}^{r/f}$ and characterized using a quasistatic approach at the cell-level. At the circuit level, since each input pin $k$ of a logic cell $i$ has different probability distribution of transition time $tr_{r/f}$ (r/f for rise and fall), computed using the results of the method in Section IV-A, the age gain from each rise or fall signal on pin $k$ also has a unique distribution.

Unlike the case of static timing analysis (STA) for delay analysis, where the focus of the analysis is to determine the slowest path, the aging analysis must consider the average operational conditions (and then find the slowest path in the circuit at various points in time). Therefore the mean value of the age gain distribution is calculated as shown in Equation (18), where the new term $\text{AG}_{k,j}$ is defined as the mean age gain of transistor $j$ per input signal cycle (including one rise and one fall signal) on pin $k$.

$$\begin{aligned} \text{AG}_{k,j} &= \text{AG}_{k,j}^{r} + \text{AG}_{k,j}^{f} \qquad (18)\\ \text{where}\quad \text{AG}_{k,j}^{r} &= \sum_{tr_r \in \mathbf{Tr_s}} \text{AG}_{k,tr_r,j}^{r} \cdot \Pr(tr_r) \\ \text{AG}_{k,j}^{f} &= \sum_{tr_f \in \mathbf{Tr_s}} \text{AG}_{k,tr_f,j}^{f} \cdot \Pr(tr_f) \end{aligned}$$

where $\mathbf{Tr_s}$ is the approximate discretized version of $\mathbf{Tr}$. Here $\text{AG}_{k,j}$ is calculated as the sum of the mean age gain per rise signal, $\text{AG}_{k,j}^{r}$, and mean age gain per fall signal $\text{AG}_{k,j}^{f}$, which are computed separately using age gain per transition under specific transition time $tr_r$ and $tr_f$ from the cell-level AG LUT in Equation (10), and the signal transition time distribution in Section IV-A.

### C. Analysis of Device Aging

The circuit-level device aging analysis is performed based on analysis of the device age gain per signal cycle in the above section, and the statistical estimation of signal cycles in a given period of circuit operations. All signal paths (instead of only critical ones in STA) are considered in the device aging analysis, because all signal propagations affect the device aging. If a circuit is $V_{dd}$-gated or power-gated, the device aging model incorporates this effect using signal statistics, as shown below.

During a time period $t$ of circuit operation, the age of a transistor $j$ in a digital circuit is the accumulation of age gains (AGs) due to signal cycles on its input pins that occurred from time 0 to $t$. Since we have already obtained the mean AG per signal cycle in Equation (18), the device age function can be written as the number of signal cycles on each pin $k$ times AG per cycle of $k$, summed for all input pins of cell $i$ (where transistor $j$ belongs), as follows:

$$\text{age}_j(t) = \sum_{k \in \text{pin}_i} N_k \cdot \text{AG}_{k,j} = \sum_{k \in \text{pin}_i} \eta_k \cdot t \cdot \text{AG}_{k,j} \quad (19)$$

Here $\text{AG}_{k,j}$ stands for the mean age gain of transistor $j$ per cycle of input signal on pin $k$; $N_k$ stands for the number of signal cycles on pin $k$ during time period of $t$, and $\eta_k = N_k/t$ is defined as the rate of effective signal cycle on input pin $k$, that causes cell switching. The value of $\eta_k$ can be obtained using the statistical information of signal probability (SP) and activity factor (AF) as

$$\eta_k = f_{\text{ref}} \cdot \text{AF}_k \cdot \Pr_{k\ \text{critical}} \qquad (20)$$

Here, $f_{\text{ref}}$ is the frequency of reference clock, $\text{AF}_k$ is the activity factor of the $k^{\text{th}}$ input pin of cell $i$, i.e., the average number of signal transition cycles in a reference clock cycle [20], and $\Pr_{k\ \text{critical}}$ is the critical probability of pin $k$, i.e., the probability that the cell output is dependent on the input logic of pin $k$:

$$\Pr_{k\ \text{critical}} = \text{Prob}(\text{output}(\text{pin}_k = 0) \neq \text{output}(\text{pin}_k = 1)) \quad (21)$$

This can easily be calculated using the joint signal probability of the input pins (computed from the Monte Carlo-based SP simulations described in Section VI) and the truth table of the logic cell.

### D. Analysis of Circuit Delay Degradation

The circuit delay degradation analysis is performed based on the models discussed in the previous sections, and static timing analysis (STA) is performed using a PERT-like traversal [11] to calculate the delay of the fresh and the aged circuits.

Since the HC aging is dependent on the signal transition as modeled in Section III-A, an initial STA of the fresh circuit is necessary for calculating the HC aging, based on which the circuit delay degradation after a period of operation can be computed by doing STA again with aged device parameters.

HC effects can slow down the signal transition during the aging process, which in turn reduces the age gain per transition, further slowing down HC-based circuit aging. Therefore,

in principle, the circuit delay degradation is generally a *decelerating* process, as will be pointed out in Section VI, and it may need iterations for accurate analysis that recalculate the slowdown in signal transition times in multiple steps and update the age gains. Our experimental results in Section VI explore a *one-step* method (where the signal transition times at $t = 0$ are used throughout the simulation) with a *N-step* iterative method (where the transition times are updated N times through the life of the circuit). The experimental results in Section VI-A demonstrate that in practice this deceleration effect of aging is quite insignificant and can be safely ignored, so that the degradation analysis can be performed efficiently without iterations[2].

The degraded critical path delay $D$ in a digital circuit is given by

$$D = \sum_{i \in \text{path}} d_{i0} + \sum_{i \in \text{path}} \Delta d_i = D_0 + \Delta D \tag{22}$$

The cell-level delay degradation $\Delta d_i$, which is modeled as a linear function of all transistor degradation $\Delta I_{\text{on}}/I_{\text{on}}$ in Equation (11), can be derived as following using the models of $\Delta I_{\text{on}}/I_{\text{on}}$ and $\text{AG}_{k,j}$ in Equation (4) and (18).

$$\begin{aligned} \Delta d_i &= \sum_{j \in \text{cell } i} S_{ij}^d \cdot A \cdot (\text{AR}_j^{(i)} \cdot t)^n \quad (23) \\ \text{where} \quad \text{AR}_j^{(i)} &= \sum_{k \in \text{pin}_i} \eta_k^{(i)} \text{AG}_{k,j}^{(i)} \end{aligned}$$

Therefore the critical path delay degradation is

$$\Delta D = At^n \sum_{i \in \text{path}} \sum_{j \in \text{cell } i} S_{ij}^d \cdot (\text{AR}_j^{(i)})^n \tag{24}$$

Equation (24) indicates that the path delay degradation of digital circuits has a power function versus time, with the same exponent $n$ as the power model of device degradation in Equation (4). However, since devices on different paths have different rate of aging, the longest-delay path may change after a period of degradation, as will be shown in the experimental results in Section VI-A.

## V. Variation-aware Hot Carrier Aging Analysis

In Sections III and IV, we had developed machinery for analyzing circuit delay degradation due to HC effects for the nominal case. In this section, we extend the proposed HC aging and circuit degradation analysis approach to incorporate the effects o process variations. We begin by presenting the underlying models used to represent process variations. Next, we modify the previously described transistor-level model and cell-level characterization approaches for HC aging to incorporate the effects of variations. Finally, we devise an efficient method for performing circuit-level delay degradation analysis due to HC effects under process variations. As will be demonstrated in our results in Section VI-B, the impact of process variations on aging are significant.

[2]Other authors [10] have found nontrivial *acceleration* effects of HC degradation, mainly due to the inaccuracy of their model assumption of constant HC stress during signal transitions (in contrast to our time-varying model illustrated in Fig. 1).

### A. Modeling Process Variations

The variations of the process parameter created at the fabrication time can be classified as lot-to-lot, die-to-die (D2D), and within-die (WID) variations, according to their scope; they can also be divided as systematic and random variations by the cause and predictability. Usually WID variations exhibit spatial dependence knows as spatial correlation, which need be considered for accurate analysis.

This paper employs a widely-used model for process variations: a process parameter $X$ is modeled as a random variable about its mean, $X_0$, as [21]:

$$\begin{aligned} X &= X_0 + X_g + X_s + X_r \quad (25) \\ \sigma_X^2 &= \sigma_{X_g}^2 + \sigma_{X_s}^2 + \sigma_{X_r}^2 \end{aligned}$$

Here, $X_g$, $X_s$, and $X_r$ stand for the global part (from lot-to-lot or D2D variations), the spatially correlated part (from WID variation), and the residual random part, respectively. This model assumes all the devices on the same die have the same global part $X_g$. The spatially correlated part is captured by a grid-based model similar to [11]. The entire circuit is divided into equally-sized grids by its geometry layout. All transistors within the same grid have the same spatially correlated part $X_s$, and the transistor parameters in different grids are correlated, with the correlation coefficient falling off with the distance increasing. The random part $X_r$ is unique to each transistor in the circuit.

In this paper we consider the variations in the transistor width ($W$), the channel length ($L$), the oxide thickness ($T_{ox}$), as well as shifts in the threshold voltage $V_{th}$ due to random dopant fluctuations (RDFs). In other words, for each device, $X$ represents elements of the set $\{W, L, T_{ox}, V_{th}\}$. As in the large body of work on SSTA, we assume Gaussian-distributed parameters for each of these process parameters, with $W$ and $L$ exhibiting spatial correlation, and $T_{ox}$ and $V_{th}$ being uncorrelated from one device to the next. The essential idea can be extended to incorporate other types of variations into the formulation. The spatial correlation can be extracted as a correlation matrix using model proposed in [22], and then processed using principal components analysis (PCA) to reduce the data dimension. The value of the process parameter in each grid is expressed as a linear combination of the independent principal components. Notationally, each process parameter $X$ is expressed as a vector in a random space, with basis $\mathbf{e} = [\mathbf{e}_g, \mathbf{e}_s, \mathbf{e}_r, \epsilon]^{\mathbf{T}}$, as

$$\begin{aligned} X &= X_0 + \Delta X = X_0 + \mathbf{k}_X^{\mathbf{T}} \mathbf{e} \quad (26) \\ &= X_0 + \mathbf{k}_{Xg}^{\mathbf{T}} \mathbf{e}_g + \mathbf{k}_{Xs}^{\mathbf{T}} \mathbf{e}_s + \mathbf{k}_{Xr}^{\mathbf{T}} \mathbf{e}_r + k_\epsilon \epsilon \\ \sigma_X^2 &= \mathbf{k}_X^{\mathbf{T}} \mathbf{k}_X, \quad \text{cov}(X_i, X_j) = \mathbf{k}_{Xi}^{\mathbf{T}} \mathbf{k}_{Xj} - k_{\epsilon_i} k_{\epsilon_j} \end{aligned}$$

Here, $\mathbf{e}_g = [e_{Wg}, e_{Lg}]^{\mathbf{T}}$ is the basis for global part ($T_{ox}$ variation is considered purely random hence does not have global and spatial parts), $\mathbf{e}_s = [e_1, ..., e_t]^{\mathbf{T}}$ is the basis of principal components for the spatially correlated part, where $t$ is the number of dimensions after the PCA processing, and $\mathbf{e}_r = [\epsilon_1, ..., \epsilon_m]^{\mathbf{T}}$ is the basis of random part. Its dimension, $m$, will depend on the implementation of the SSTA algorithm, and can vary from constant to linear (of circuit size), as will

be discussed later in this paper. The random part vector $\mathbf{k}_r$ can be implemented using a sparse data structure. The Gaussian variable $\epsilon \sim N(0,1)$ is a separate independent random part for use in circuit-level timing analysis.

### B. Transistor-Level Aging Model under Variations

The variations in the process parameters corresponding to the transistor width, $W$, length, $L$, and oxide thickness, $T_{ox}$, originate in the fabrication process, and are "baked in" (i.e., remain constant) for each manufactured circuit through its lifetime. Under these process variations, the *rate of aging* defined in (7) will be affected by the fluctuation of the process parameters as well as the input/output conditions, and can be updated as

$$R_{\text{it}}^{\text{var}} = R_{\text{it}} + f(\mathbf{\Delta X}) + g(\mathbf{\Delta Y}) \tag{27}$$

Here $\mathbf{\Delta X} = \{\Delta W_j, \Delta L_j, \Delta T_{ox,j}\}, j \in$ cell $i$ is the fluctuation vector of process parameters of all transistors within the logic cell $i$, and $\mathbf{\Delta Y}$ is the fluctuation vector of circuit-specific conditions, including input signal transition time $\Delta tr$ and load capacitance $\Delta C_L$, which come from the process variations of transistors in the fanin/fanout cells in the circuit.

Using the quasistatic approach in (9), the transistor age gain per signal transition under process variation is

$$\begin{aligned} \text{AG}^{\text{var}} &= \int_{\text{tran}} R_{\text{it}}^{\text{var}}(t)\text{dt} \\ &= \text{AG}_{\text{nom}} + F(\mathbf{\Delta X}) + G(\mathbf{\Delta Y}) \end{aligned} \tag{28}$$

Here $F(\mathbf{\Delta X})$ and $G(\mathbf{\Delta Y})$ are the integral of $f(\mathbf{\Delta X})$ and $g(\mathbf{\Delta Y})$, respectively, and they stand for the variation of *age gain* per signal transition due to the process parameters $\mathbf{\Delta X}$ and circuit-specific conditions $\mathbf{\Delta Y}$, respectively.

### C. Cell-Level Model and Characterization under Variations

Our cell-level modeling and characterization under process variations consists of two parts: transistor age gain characterization and cell timing characterization.

Following the quasistatic approach (28), we use first-order Taylor expansion to model the device age gain of one signal transition event under process variations as follows:

$$\text{AG}^{\text{var}} = \text{AG}_{\text{nom}} + F(\mathbf{\Delta X}) + G(\mathbf{\Delta Y}), \tag{29}$$

$$\begin{aligned} \text{where } F(\mathbf{\Delta X}) &= \sum_{j \in \text{cell } i} \frac{\partial \text{AG}}{\partial W_j}\Delta W_j + \sum_{j \in \text{cell } i} \frac{\partial \text{AG}}{\partial L_j}\Delta L_j \\ &\quad + \sum_{j \in \text{cell } i} \frac{\partial \text{AG}}{\partial T_{ox,j}}\Delta T_{ox,j} \end{aligned} \tag{30}$$

$$G(\mathbf{\Delta Y}) = \frac{\partial \text{AG}}{\partial tr}\Delta tr + \frac{\partial \text{AG}}{\partial C_L}\Delta C_L \tag{31}$$

The nominal value $\text{AG}_{\text{nom}}$ and its sensitivities $\partial \text{AG}/\partial(\cdot)$ to the variational parameters are all characterized by HSPICE simulation in a manner similar to Section III-B, and the results are stored in LUTs for the use of circuit-level analysis. The variational parameters $\Delta W_j$, $\Delta L_j$, $\Delta T_{ox,j}$ and $\Delta tr$ are Gaussian random variables in vector form in the random variable space $\mathbf{e}$, as defined in (26). The load capacitance $C_L$ has following relationship with the process parameters of the fanout transistors

$$C_L = K \sum_{k \in \text{Fanout}(i)} \frac{W_k L_k}{T_{ox,k}} \tag{32}$$

Under assumption of $\sigma/\mu$ being a relatively small value (e.g. $< 10\%$), which is true for reasonable processes, their product and quotient can be approximated as a Gaussian random variable in the same space $e$, using the linear approximation based on moment matching method discussed in Appendix D. In this manner, $C_L$ is also expressed as a vector in the RV space $\mathbf{e}$. The input signal transition time $\Delta tr$ will be modeled in the cell timing characterization below in (35). Based on these models, the transistor age gain under variations, which depends linearly on these parameters as (29), can also be presented as a Gaussian random variable in the space $\mathbf{e}$.

The transistor drain current degradation, modeled by (4), is a power function of age

$$(\Delta I_{\text{on}}/I_{\text{on}})_j = A(\text{age}_j)^n \tag{33}$$

with the exponent $n \approx 1/2$. Since the transistor age calculated by (19) is a Gaussian random variable in the space $\mathbf{e}$, its power function can also be approximated as Gaussian in the same RV space using methods proposed in Appendix C, using the mean and variance computed by Appendix A or B.

The cell timing characterization under process variations is performed based on following first-order model of propagation delay $d_i$ and output signal transition time $tr_i$,

$$d_i = d_{i0} + \sum_{X \in P_i} \frac{\partial d_i}{\partial X}\Delta X \tag{34}$$

$$tr_i = tr_{i0} + \sum_{X \in P_i} \frac{\partial tr_i}{\partial X}\Delta X \tag{35}$$

Here, $P_i = \{W_j, L_j, T_{ox,j}, (\Delta I_{\text{on}}/I_{\text{on}})_j, V_{th,j}\}, j \in$ cell $i$ are the process and aging parameters of the transistors in the cell that are considered for timing variation and degradation, and $\partial d_i/\partial(\cdot)$ are the corresponding sensitivities to these parameters. These sensitivity values are computed using HSPICE analysis and stored in a look-up table for the use of circuit level timing analysis.

### D. Circuit-Level Analysis under Variations

Under process variations, the circuit-level delay and degradation analysis is based on the SSTA framework proposed in [11], which handles all cell delays, arrive times, and signal transitions as Gaussian random variables in the space $\mathbf{e}$, and performs $\mathrm{sum}$ and $\mathrm{max}$ operations in space $\mathbf{e}$ while performing a PERT-like traversal to calculate the total delay.

As in the nominal case discussed in Section IV-D, an initial SSTA of fresh circuit is performed to calculate the signal transition of all nodes, from which the device aging under process variations is calculated for a given period of operation time. Then SSTA is performed again with degraded device parameters to calculate the circuit delay. The results from the nominal case analysis already demonstrate the approximation of using signal transition $tr$ from STA results, and using 1-step analysis are both very accurate. Meanwhile when process

variations are considered, their impact on transition time $tr$ is a second-order effect, and a small change due to variations will have a very diluted impact on delay degradation. Therefore in the variational case we keep using $tr$ value from SSTA results instead of the full distribution, and using a 1-step analysis to effectively reduce runtime while maintaining accuracy.

In SSTA, the way of handling the random part $\mathbf{k}_{Xr}^{\mathbf{T}}\mathbf{e}_r$ could affect the runtime and accuracy of the results. Since the random parts come from the process parameters of different devices in the circuit and are independent with each other, when calculating the signal arrival time through a circuit traversal, the size of the random parts can grow significantly, resulting in quadratic complexity for runtime and storage. A simple remedy is to merge the random part $\mathbf{k}_{Xr}^{\mathbf{T}}\mathbf{e}_r$ of each random variable into a separate scalar term $k_\epsilon\epsilon$. This method greatly reduces the time and storage complexity, but the accuracy is slightly affected due to the path reconvergence in the circuit topology which introduces correlations to the random parts. In [23] a better trade-off between accuracy and complexity was proposed by removing smaller elements in the random vector $\mathbf{k}_{Xr}$ using preset threshold and merge them into the separate term $k_\epsilon$. We use this method to handle the random part and the results in Section VI-B verify that it is accurate and efficient.

## VI. Experimental Results

The proposed method for delay degradation analysis of digital circuit is applied to the ISCAS85 and ITC99 benchmark circuits for testing. The circuits are mapped to a subset of the Nangate 45nm open cell library [24] using ABC [25], with placement carried out using a simulated annealing algorithm. The cell-level library characterization was performed using HSPICE simulation and 45nm PTM model [26]. The circuit-level analysis was implemented in C++ and run on a Linux PC with 3GHz CPU and 2GB RAM. The parameters $a_2$, $a_3$ and $m$ of the device-level HC model in Equation (7) is from [7]. The coefficients $C_1$, $C_2$ and $C_3$ for different energy-driven modes have arbitrary units (a.u.) and are selected empirically according to the $\tau$ vs $I_{ds}/W$ plot in [7]. The parameter $A$ in Equation (4) also has a.u..

### A. Results of Nominal Degradation Analysis

The cell-level characterization of transistor age gain, as well as the degradation of cell delay and output transition is performed using HSPICE simulation with the enumeration of all signal input cases for each cell. In nominal case (where the process variations are not included), the characterization of the library which contains 55 logic cells takes 1 hour and 52 minutes of runtime and 8.4MB of hard drive storage (in ASCII format). This is $1.9\times$ runtime and $5.9\times$ storage overhead compared with timing characterization (Equations (14–17)), which is well within reasonable range.

Fig. 3 plots the curves of the NMOS transistor age gain (AG) versus the input signal transition $tr$ of an inverter with a rising input signal, under different load capacitance $C_L$. The figure indicates that the input signal transition generally causes more damage to the transistor (larger AG) when the load $C_L$ is

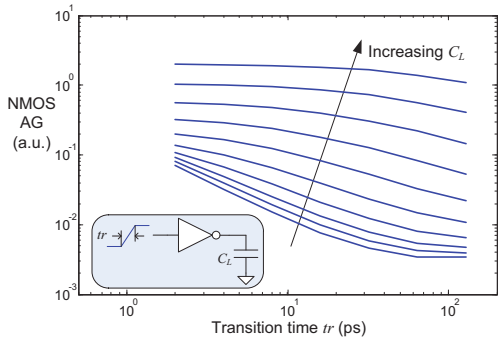


Fig. 3. Age gain versus signal transition time and load capacitance.

large, or when the transition $tr$ is small. This is explained by the fact that HC degradations are caused by the charge carriers flowing through the channel, and larger load $C_L$ requires more charge to be moved, while smaller transition $tr$ makes the carriers moving faster, thus causing more damage. This result is consistent with the data presented in [8]. In other transition cases, with different cells and input signals, the AG vs. $tr$ and $C_L$ plots may be slightly different, but all have a trend similar to Fig. 3. Specifically, for the small range in which the transition time increases as a result of aging (<2%), the AG generally reduces slightly, i.e., aging slightly decelerates with time.

Fig. 4 shows a plot of the circuit degradation analysis result of the $N$-step method discuss in Section IV-D with $N$ set from 1 to 256. The plot indicates that the overall error between 1-step and $N$-step is very small ($< 1\%$), and that $N$=64 is an adequate step number for the balance between runtime and accuracy. Therefore in the following analysis $N$=64 will be used for the $N$-step method.

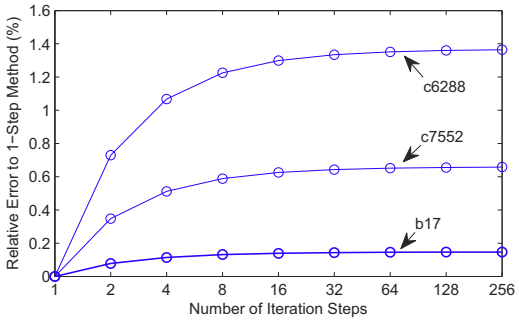


Fig. 4. Circuit degradation analysis with different number of iterations.

The results of the proposed approach for circuit degradation analysis under HC effects are presented in Table I for different benchmark circuits. The sizes of the circuits range from 221 cells (c432) to 20407 cells (b17). Three methods are implemented and applied on each benchmark: the first is a Monte Carlo (MC) simulation to calculate the circuit degradation by stressing the circuit using 10000 random input signal transitions; the second is the proposed analysis approach using one-step approximation that ignores the deceleration of aging, and the third incorporates the deceleration process using $N$-step method, updating the aged $tr$ at 64 time points over

the life of the circuit (see Section IV-D for details). The signal probability (SP) and activity factor (AF) data for the latter two methods is obtained using Monte Carlo method with 10000 random input transition samples. The circuit degradations are calculated at $t$=10000 (a.u.) with reference clock $f_{\text{ref}}$=1GHz, input SP=0.5 and AF=0.05.

In Table I, the first column lists the benchmark circuit name, the second and third columns list the number of cells and the fresh delay of the circuit, the fourth column lists the runtime of SP and AF calculation, and the remaining columns show the runtime and circuit delay degradation obtained using the three methods. The results show that the one-step analysis and 64-step analysis yield very close results (<1% relative error), and that the error between using the full $tr$ distribution ($\Delta D$) and using a single $tr$ value from the STA result ($\Delta D_{tr}$) is negligible, demonstrating that the effect of $tr$ distribution and its dynamics on the circuit degradation is very small and can be safely ignored to reduce computation. The error between one-step analysis and MC is small (3.3% relative error) while the one-step method has much lower runtime, indicating the proposed analysis method is efficient and accurate compared with Monte Carlo simulation.

The last column shows a comparison with a simple duty-factor based scheme, similar to [10]. Note that in contrast with this method, our approach performs quasistatic analysis with newer energy-driven model, which captures the time-varying HC stress, and indicates that the transistor AG decreases when signal transition slows down (Fig. 3). In addition, [10] uses an empirical device HC model which only considers the switching transistors and ignores the other transistors in the stack which also experience current stress. Our approach perform the device degradation analysis in the cell level, and the AG of all transistors in a logic cell is computed simultaneously. The results in the last column assume constant HC stress through signal transitions, ignores non-switching transistor degradation, and uses worst-case transition time. Experimental results of all tested benchmarks show errors of $-44\%$ to $+64\%$ for this method. It is clear that the use of such simplifying assumptions, commonplace in all prior work on large-scale circuits, results in serious errors.

It is important to note that the SP and AF analysis take more time than the HC degradation calculation; however (a) this computation is a common overhead shared by other circuit analyses, such as power estimation, oxide reliability, BTI degradation, etc., and should not be counted solely towards the proposed approach, and (b) our implementation uses Monte Carlo simulation to generate these probabilities; faster graph traversal based methods may also be used.

Fig. 5 shows the circuit delay degradation versus time on a logarithm scale for benchmark c1908 using both the proposed analysis method (one-step) and MC simulation. The results from these two approaches match well with each other, and the delay degradation is a power function of time with exponent 0.5 before $t$=10000 (a.u.). After that the delay degradation is no longer a power function and increases at a faster rate since the critical path may change, as discussed in Section IV-D.

An examination of the degradation of $tr$ confirms that the effects of aging deceleration are negligible. Fig. 6 shows the

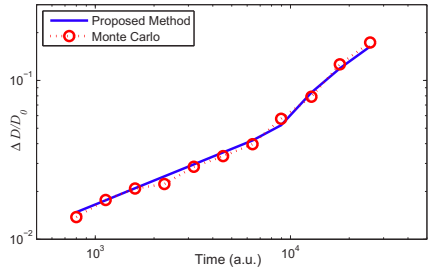


Fig. 5. Circuit delay degradation versus time.

histograms of the degradation $\Delta tr/tr_0$ of benchmark c7552, where $tr_0$ is the signal transition time of a node in the fresh circuit, and $\Delta tr$ is the transition increment of each node at $t$=10000 (a.u.). The histograms of rise and fall signal transition degradation are plotted separately. We can see that although the circuit has nearly 13% delay increasing, the degradation of transition time is only around 5% in average, which causes very small impact on AG, according to the AG/$tr$ curves in Fig. 3. This explains the fact that in Table I, the results of $\Delta D$ using 1-step analysis and 64-step analysis are very close. In contrast, the simply duty factor model assumes constant HC stress in the off-to-on transition, leading to the result that the transition time degradation elevates the duty factor and accelerate circuit degradation, which is incorrect.

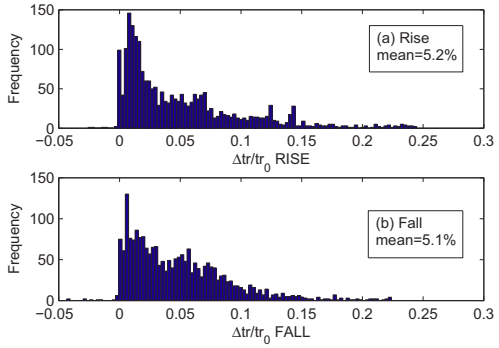


Fig. 6. Histogram of transition time degradations.

We further examined the effect of $tr$ distribution due to different signal paths. Section IV-A has discussed that theoretically it is necessary to calculate full $tr$ distribution at each circuit node for AG calculation. We captured the $tr$ distribution of all primary output nodes in benchmark c7552 in MC simulation. Results show the actual $tr$ distribution has a very small standard deviation (average $\sigma_{tr}/\mu_{tr}$=1.34%), and its mean value is very close to the STA result (average $\mu_{tr}/tr_0$=0.98). This explains the results in Table I that using $tr$ approximation from STA (column $\Delta D_{tr}$) yields very high accuracy. The above observations and conclusions on $tr$ distribution are based on the widely used benchmarks which should represent the typical behaviors of digital circuits. However there may still be certain situations in real designs that are not covered by this paper, for example, some circuits may show wide transition distributions in the internal nodes. In this case, it is fairly easy to incorporate the distribution into

TABLE I
RUNTIME AND DEGRADATION COMPARISON OF DIFFERENT METHODS FOR NOMINAL CASE HC AGING ANALYSIS

| Circuit | Size | Fresh | SP/AF | 1-step Analysis | | | 64-step Analysis | | Monte Carlo (MC) | | SimpleDF |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | (#Cells) | Delay | $T_{exe}$ | $T_{exe}$ | $\Delta D$ | $\Delta D_{tr}$ | $T_{exe}$ | $\Delta D$ | $T_{exe}$ | $\Delta D$ | $\Delta D_{\text{err}}$ |
| c1908 | 442 | 835ps | 1.5s | 0.080s | 135ps | 136ps | 4.6s | 134ps | 2.1s | 135ps | 13.6% |
| c2670 | 759 | 1228ps | 2.1s | 0.120s | 134ps | 134ps | 7.3s | 134ps | 2.1s | 138ps | 24.9% |
| c3540 | 1033 | 1397ps | 4.0s | 0.230s | 425ps | 425ps | 13.4s | 424ps | 6.4s | 439ps | -22.9% |
| c5315 | 1699 | 1133ps | 5.7s | 0.260s | 80ps | 80ps | 14.6s | 80ps | 8.3s | 82ps | 56.1% |
| c6288 | 3560 | 2579ps | 30.8s | 0.640s | 489ps | 488ps | 37.4s | 483ps | 55.9s | 500ps | 42.7% |
| c7552 | 2361 | 1209ps | 9.6s | 0.350s | 138ps | 137ps | 20.3s | 137ps | 17.9s | 152ps | 1.2% |
| b14 | 4996 | 2586ps | 60.7s | 1.010s | 789ps | 790ps | 58.6s | 789ps | 74.7s | 766ps | -44.4% |
| b15 | 6548 | 2628ps | 90.4s | 1.330s | 574ps | 574ps | 77.5s | 573ps | 100.2s | 609ps | -24.2% |
| b17 | 20407 | 3201ps | 320.6s | 4.120s | 131ps | 130ps | 237.5s | 130ps | 343.6s | 135ps | -28.9% |
| b20 | 11033 | 2586ps | 171.2s | 2.170s | 502ps | 501ps | 124.6s | 502ps | 189.4s | 495ps | -7.1% |
| b21 | 10873 | 2837ps | 162.1s | 2.000s | 269ps | 269ps | 116.1s | 269ps | 179.8s | 262ps | 8.2% |
| b22 | 14794 | 2845ps | 232.9s | 2.740s | 325ps | 326ps | 158.3s | 325ps | 254.8s | 335ps | -36.6% |
| Average Error to MC | | | | | 3.3% | 3.4% | | 3.6% | | | |

the proposed algorithm and will not significantly degrade the computational complexity.

### *B. Results for Variation-Aware Degradation Analysis*

With the consideration of process variations, the library characterization of timing, aging and their sensitivities to process parameters using HSPICE takes 4 hour and 27 minutes of runtime and 21.3MB of hard drive storage (in ASCII format). This is $4.5\times$ runtime and $15.1\times$ the storage overhead compared with the basic timing characterization required for the nominal case (Equations (14–17)), which is reasonable.

The process variations in parameters $W$, $L$, and $T_{ox}$ are set to $3\sigma$=4% of their mean values [27]. The $V_{th}$ variation due to RDF is dependent on the device size [28]. It has a Gaussian distribution with mean value $\mu = 0$, and standard variation

$$\sigma_{V_{th}} = \sigma_{V_{th0}} \sqrt{\frac{W_0 L_0}{WL}} \tag{36}$$

in which $\sigma_{V_{th0}}$ is the RDF-induce threshold standard deviation of a minimum-sized device ($W_0$ by $L_0$). The value of $\sigma_{V_{th0}}$ is dependent on process parameters and the doping profile. Here we assume $3\sigma_{V_{th0}} = 5\%$ of the nominal $V_{th}$. The parameter variations of $W$ and $L$ are split into $20\%$ of global variation, $20\%$ of spatially correlated variation and $60\%$ of random variation, while the variations of $T_{ox}$ and $V_{th}$ are fully random. The grid-based spatial correlation matrix is generated using the distance based method in [22], with the number of grids growing with circuit size, as shown in Table II. We have used the same assumptions for operation time, frequency, and input SP/AF as the nominal case in previous section.

Based on the conclusions from the experimental results of nominal case in previous section, we use the $tr$ value from SSTA results as an valid alternative of full $tr$ distribution, and 1-step method instead of multi-step iterative calculation of circuit aging, in order to reduce the runtime of the variation-aware analysis of circuit degradation under HC effect.

The proposed analytical approach is verified by Monte Carlo (MC) simulation. For the variational case, the MC simulation is performed by generating 5000 circuit samples with randomized process parameters, then for each circuit sample with the parameters determined, calculating the HC aging and delay degradation of using the proposed analytical method for nominal case. Using this simulation scheme is based on the consideration that the proposed analytical method for nominal case has already been verified by MC simulation in Section VI-A, and performing a full MC simulation with both randomized process parameters and input vectors will be too time-consuming and impractical.

The proposed approach for variation-aware circuit degradation analysis under HC effects are presented in Table II for different benchmark circuits. Three methods for circuit degradation analysis are implemented and compared. The first is denoted as Variational Analysis 1 (VA1), which simply combines nominal case HC aging analysis and SSTA with process variations, without considering the impacts of process variations on HC aging (i.e., the $F(\mathbf{\Delta X}) + G(\mathbf{\Delta Y})$ term in (28)). The second, denoted as Variational Analysis 2 (VA2), is similar to VA1 but does include the impacts of process variations on HC aging (the $F(\mathbf{\Delta X})+G(\mathbf{\Delta Y})$ term). The last one is a Monte Carlo (MC) simulation with the same assumptions as VA2. The runtime, mean and standard deviation (SD) value of the circuit delay degradation $\Delta D$ for these three methods are listed in Table II, along with the fresh delay and delay degradation of the nominal case.

The VA2 results matched the MC simulation very well, with a 1.6% average error in $\mu_{\Delta D}$ and 4.1% average error of $\sigma_{\Delta D}$), and much lower runtime, indicating the proposed variation-aware degradation analysis approach VA2 is accurate and efficient. In comparison, the VA1 method, which ignores the interaction between process variations and HC aging, has much shorter runtime than VA2, has close $\mu_{\Delta D}$ results as compared to VA2 and MC (4.1% error to MC), but large errors on $\sigma_{\Delta D}$ (23.9% to MC).

Fig. 7 shows the probability distribution function (PDF) of circuit delay of benchmark b21 at $t$=10000 (a.u.). The visual match of VA2 and MC verifies that the circuit delay under HC aging and process variation effects follows Gaussian distribution with its mean and SD accurately predicted by proposed VA2 approach. The result from VA1 has noticeable error compared with VA2 and MC. These results indicate that VA2 has much better accuracy and should be used for degradation analysis in the variational case. However in the scenario of runtime in higher priority than accuracy, VA1 can be used instead.

TABLE II
RUNTIME AND DEGRADATION COMPARISON OF VARIATION-AWARE HC AGING ANALYSIS METHODS

| Circuit | Size | | Nominal Delay | | Variational Analysis 1 | | | Variational Analysis 2 | | | Monte Carlo (MC) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | #Cells | #Grids | Fresh | $\Delta D$ | $T_{exe}$ | $\mu_{\Delta D}$ | $\sigma_{\Delta D}$ | $T_{exe}$ | $\mu_{\Delta D}$ | $\sigma_{\Delta D}$ | $T_{exe}$ | $\mu_{\Delta D}$ | $\sigma_{\Delta D}$ |
| c1908 | 442 | 9 | 835ps | 136ps | 2.2s | 127ps | 15.1ps | 17.5s | 140ps | 12.4ps | 233s | 140ps | 12.4ps |
| c2670 | 759 | 16 | 1228ps | 134ps | 3.8s | 133ps | 23.6ps | 33.5s | 141ps | 21.2ps | 401s | 138ps | 20.6ps |
| c3540 | 1033 | 16 | 1397ps | 425ps | 6.3s | 410ps | 27.6ps | 56.9s | 429ps | 17.1ps | 688s | 428ps | 16.1ps |
| c5315 | 1699 | 16 | 1133ps | 80ps | 8.3s | 82ps | 22.6ps | 71.0s | 86ps | 20.9ps | 817s | 84ps | 21.7ps |
| c6288 | 3560 | 64 | 2579ps | 488ps | 19.1s | 444ps | 44.4ps | 171.4s | 508ps | 33.7ps | 1926s | 507ps | 35.1ps |
| c7552 | 2361 | 36 | 1209ps | 137ps | 10.9s | 145ps | 25.5ps | 93.7s | 149ps | 22.4ps | 1098s | 148ps | 21.7ps |
| b14 | 4996 | 81 | 2586ps | 790ps | 29.1s | 808ps | 58.8ps | 287.0s | 810ps | 42.9ps | 3084s | 808ps | 44.9ps |
| b15 | 6548 | 100 | 2628ps | 574ps | 40.3s | 584ps | 53.6ps | 400.7s | 591ps | 42.7ps | 4272s | 586ps | 38.5ps |
| b17 | 20407 | 361 | 3201ps | 130ps | 128.9s | 135ps | 58.5ps | 1317.6s | 146ps | 56.3ps | 13286s | 135ps | 58.0ps |
| b20 | 11033 | 169 | 2586ps | 501ps | 64.5s | 493ps | 52.5ps | 657.1s | 512ps | 45.1ps | 6653s | 507ps | 43.1ps |
| b21 | 10873 | 169 | 2837ps | 269ps | 61.8s | 269ps | 53.8ps | 598.6s | 285ps | 48.2ps | 6353s | 281ps | 45.7ps |
| b22 | 14794 | 225 | 2845ps | 326ps | 84.6s | 334ps | 57.2ps | 829.9s | 334ps | 48.0ps | 8605s | 328ps | 47.3ps |
| Average Error to MC | | | | | | 3.6% | 23.9% | | 1.6% | 4.1% | | | |

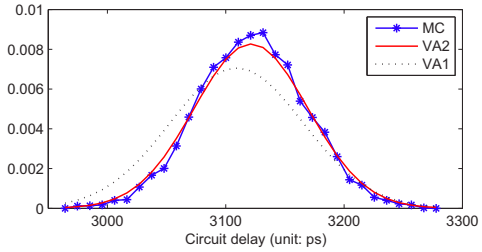


Fig. 7. The circuit delay PDF of benchmark b21 under variations.

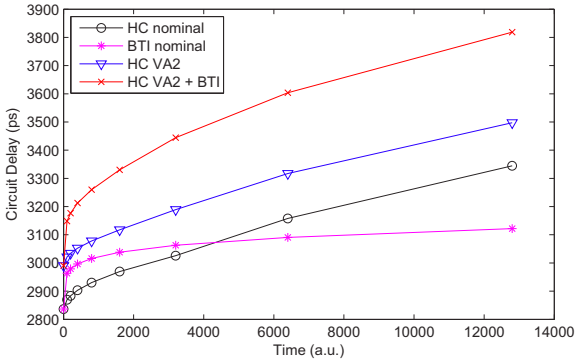


Fig. 8. Degradation vs. time of b21 for different degradation components.

### C. Delay degradation under both HC and BTI effects

To provide a holistic picture, we now show the impact of aging due to all major reliability issues. In addition to HC effects, the analysis of bias temperature instability (BTI) effects is also added to determine circuit delay degradation. For BTI, we follow the SP/AF based modeling and analysis approach proposed in [20], and the assumption of the relative relationship between HC and BTI effect is based on the results of [4]. For simplicity the BTI degradation is considered for nominal case, with the time exponent assumed to be $n$=1/6. The effect of HC aging and BTI degradation on circuit timing are combined using a superposition model, where the cell delay and signal transition are calculated using first-order approximation:

$$\Delta d_i = \sum_{j\in \text{cell } i} S^d_{ij,\text{HC}}(\Delta I_{\text{on}}/I_{\text{on}})_j + \sum_{j\in \text{cell } i} S^d_{ij,\text{BTI}}\Delta V^{(j)}_{\text{th}} \quad (37)$$

$$\Delta tr_i = \sum_{j\in \text{cell } i} S^{tr}_{ij,\text{HC}}(\Delta I_{\text{on}}/I_{\text{on}})_j + \sum_{j\in \text{cell } i} S^{tr}_{ij,\text{BTI}}\Delta V^{(j)}_{\text{th}} \quad (38)$$

Fig. 8 plots the circuit delay degradation as a function of time for nominal HC aging, nominal BTI degradation, HC aging under process variations using VA2 (results shown as $\mu + 3\sigma$ values), and the total delay degradation. The results indicate that BTI is the dominant aging effect in the early lifetime of digital circuit but grows slower with time, while HC effect begins low but grows faster, and surpasses BTI effect in the late lifetime. This is in consistent with the fact that HC effect has a larger time exponent (∼1/2) than the BTI effect (∼1/6).

Fig. 9 shows the bar plot of the circuit delay degradations (normalized to fresh delay) of different benchmark, due to the effect of process variations (PV), BTI, and HC, at time points of 100, 500, and 4000 (a.u.), representing the early, medium and late lifetime scenarios. The plot indicates that while effect of PV remain at the same level, the BTI effect dominates the early stage and the HC effect dominates the late stage of the circuit lifetime.

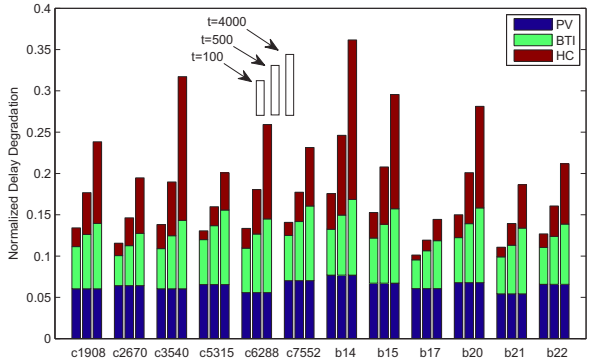


Fig. 9. Circuit degradation components from process variations (PV), BTI effects, and HC effects.

## VII. Conclusion

This paper focuses on the HC effect in large scale digital circuits, and proposes scalable approaches for analyzing CHC/CCC-induced delay degradation, with innovations in analysis at the transistor, cell, and circuit levels. The proposed approaches can handle nominal case and variation-aware case, both validated by Monte Carlo simulations on benchmark circuits and are shown to be efficient and accurate.

The interactions between process variations and HC effects are investigated and discovered to have nonnegligible impact to the circuit degradation, and need to be included in the analysis. The deceleration dynamics of HC aging, as well as its dependence on signal transition distributions are discovered to be negligible, thus can be approximated using simple alternatives so that the computational complexity could be effectively reduced.

## Appendix A
## Square root of a Gaussian RV

For $x \sim N(\mu_x, \sigma_x^2)$, given $\mu_x \gg \sigma_x > 0$ so that $x > 0$ is always true, its square root $y = x^n$, $n = \frac{1}{2}$ can be approximated as another Gaussian distribution $y \sim N(\mu_y, \sigma_y^2)$, with its mean $\mu_y$ and variance $\sigma_y^2$ calculated as follows.

Since $x = y^2$, we have

$$E(x) = E(y^2) \tag{39}$$
$$E(x^2) = E(y^4) \tag{40}$$

As both $x$ and $y$ have Gaussian distribution,

$$\mu_x = \mu_y^2 + \sigma_y^2 \tag{41}$$
$$\mu_x^2 + \sigma_x^2 = \mu_y^4 + 6\mu_y^2\sigma_y^2 + 3\sigma_y^4 \tag{42}$$

The mean and variance of $y$ is solved to be

$$\mu_y = \left(\mu_x^2 - \frac{1}{2}\sigma_x^2\right)^{\frac{1}{4}} \tag{43}$$
$$\sigma_y^2 = \mu_x - \left(\mu_x^2 - \frac{1}{2}\sigma_x^2\right)^{\frac{1}{2}} \tag{44}$$

## Appendix B
## Power Function of a Gaussian RV

In the case of $n$ is a real number with arbitrary value[3], the relation $y = x^n$ can be rewritten as

$$y = \exp\left(n \ln\left(x\right)\right) \tag{45}$$

In [29], $q = n\ln(x)$ is approximated as Gaussian with

$$\mu_q = n\left(2\ln\mu_x - \frac{1}{2}\ln\left(\sigma_x^2 + \mu_x^2\right)\right) \tag{46}$$
$$\sigma_q^2 = n^2\left(\ln\left(\sigma_x^2 + \mu_x^2\right) - 2\ln\mu_x\right) \tag{47}$$

Therefore $y = \exp(q)$ has a lognormal distribution with

$$\mu_y = \exp\left(\mu_q + \frac{1}{2}\sigma_q^2\right) \tag{48}$$
$$\sigma_y^2 = \left(\exp\left(\sigma_q^2\right) - 1\right)\exp\left(2\mu_q + \sigma_q^2\right) \tag{49}$$

This lognormal distribution is approximated as Gaussian, with the same mean and variance.

[3]The HC time exponent is generally modeled to be $1/2$, however the exact value may vary for a specific technology.

## Appendix C
## Linear Approximation of $x^n$

For $y = x^n$ in which $x$ is a Gaussian RV with a RV space expression, we want to approximate $y$ as a Gaussian RV in the same space in order to simplify the circuit analysis. In this scenario, $y$ is approximated as a linear relation with $x$,

$$y \doteq k \cdot x + c \tag{50}$$

Since $x$ and $y$ are both Gaussian with known or derived mean and variance, the value of $k$ and $c$ are

$$k = \frac{\sigma_y}{\sigma_x} \tag{51}$$
$$c = \mu_y - \frac{\mu_x\sigma_y}{\sigma_x} \tag{52}$$

Experiments have shown that for $\sigma_x \leq 0.1\mu_x$, Gaussian distribution is a good approximation for $y = x^n$, and the proposed methods calculate its mean and variance with very good accuracy. For $n =$ 0.3–0.7, the error of $\mu_y$ and $\sigma_y$ is less than 1% for $\sigma_x = 0.1\mu_x$.

## Appendix D
## Product and Division of Gaussian RVs

For $y = x_1x_2$ (or $x_1/x_2$), where $x_1 \sim N(\mu_{x_1}, \sigma_{x_1}^2)$ and $x_2 \sim N(\mu_{x_2}, \sigma_{x_2}^2)$ are Gaussian random variables with correlation coefficient $\rho_{x_1,x_2}$, it can be approximated as Gaussian in following steps. First, $y$ is rewritten as

$$y = \exp(q), \tag{53}$$
$$\text{where } q = \ln x_1 \pm \ln x_2 \tag{54}$$

Using method from [29], $\ln x$ is approximated as a linear function of $x$, we can get the approximation

$$q \doteq k_1x_1 \pm k_2x_2 + c_1 \pm c_2, \tag{55}$$

in which $k_1$, $k_2$, $c_1$, and $c_2$ is obtained as

$$k_i = \sqrt{\ln\left(\sigma_{x_i}^2 + \mu_{x_i}^2\right) - 2\ln\mu_{x_i}}/\sigma_{x_i} \tag{56}$$
$$c_i = 2\ln\mu_{x_i} - \frac{1}{2}\ln\left(\sigma_{x_i}^2 + \mu_{x_i}^2\right) - \mu_{x_i}k_i. \tag{57}$$

So $q$ is Gaussian with mean and variance

$$\mu_q = k_1\mu_{x_1} \pm k_2\mu_{x_2} + c_1 \pm c_2 \tag{58}$$
$$\sigma_q^2 = k_1^2\sigma_{x_1}^2 + k_2^2\sigma_{x_2}^2 + 2k_1k_2\sigma_{x_1}\sigma_{x_2}\rho_{x_1,x_2} \tag{59}$$

Alternatively, the mean and variance of $q$ can be obtained directly by using the random space interpretation of $q$. The rest is similar to previous section where a lognormal RV is approximated as Gaussian. Since $y = \exp(q)$ is lognormal with mean $\mu_y$ and variance $\sigma_y^2$ following (48,49), it is approximated as Gaussian using linear function

$$y \doteq kq + c$$
$$= k(k_1x_1 \pm k_2x_2 + c_1 \pm c_2) + c, \tag{60}$$
$$\text{where } k = \frac{\sigma_y}{\sigma_q}, c = \mu_y - \frac{\mu_q\sigma_y}{\sigma_q} \tag{61}$$

Experiments have verified that for $\sigma_x \leq 0.1\mu_x$, Gaussian distribution is a good approximation for $y = x_1x_2$ (or $x_1/x_2$), and the proposed methods calculate its mean and variance with very good accuracy. This method can easily extend to the case of product of three or more Gaussian random variables.

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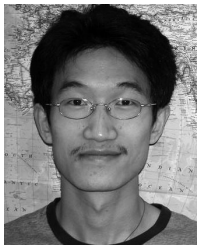

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