Spin-based Quantum Dot Quantum Computing in Silicon

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The spins of localized electrons in silicon are strong candidates for quantum information processing because of their extremely long coherence times and the integrability of Si within the present microelectronics infrastructure. This paper reviews a strategy for fabricating single electron spin qubits in gated quantum dots in Si/SiGe heterostructures. We discuss the pros and cons of using silicon, present recent advances, and outline challenges.

1. INTRODUCTION

The seminal paper by Loss and DiVincenzo[1] outlined essential components of quantum dot quantum computing (QDQC): (1) spin qubits in single electron dots, (2) qubit initialization by thermalization in a magnetic field, (3) qubit rotations performed using electron spin resonance (ESR), (4) two-qubit gates enabled by electrostatic control of exchange coupling in neighboring dots, and (5) readout by spin-charge transduction. Subsequent theoretical work has shown that two-qubit gates can be sufficiently fast (sub-nanosecond),[2,3] and that these same interactions can be harnessed for single-qubit rotations,[4,5] albeit with some encoding overhead. The most challenging aspect of scalable QDQC is fast readout: spin-dependent

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tunneling schemes have been proposed,[6,7] as well as microwave-enabled, fast initialization and readout in a closed dot.[8]

Quantum dots in semiconductors have a long history, much of which is reviewed in the excellent book.[9] An important step forward for quantum computing was the realization of dots in GaAs containing controlled numbers of electrons as few as 0 and 1.[10–12] Spin spectroscopy has been performed in dots, indicating that they are indeed viable candidates for qubits.[13–15] More recently, the ability to readout a single spin inside a quantum dot was demonstrated by Elzerman *et al.*[16] These and other important advances are reported in the paper by Engel, Kouwenhoven, Loss, and Marcus of this volume.

Many techniques developed in atomic physics can be directly adapted for quantum dots, at least in principle. Examples include readout and initialization,[8] as well as a recent proposal by Lukin and coworkers to enable long-range interactions between quantum dots.[17] However, the flexibility of quantum dots comes at the price of embedding the qubits in a solid matrix, with consequent issues related to decoherence. For this reason, materials properties are crucial for quantum dot-based devices. A major motivation for the development of the silicon quantum dot architecture is that the materials properties of silicon result in unusually long electron spin coherence times.

2. STRAINED SILICON QUANTUM DOT QUBITS

Here we outline the main challenges to QDQC in silicon, and we describe solutions for many of these problems. We discuss six critical areas: growth of strained silicon, silicon two-dimensional electron gas (2DEG) based quantum dots, valley degeneracies and their consequences, tolerance to impurities, decoherence, and bandwidth concepts at both high and low frequency limits.

2.1. Strained Silicon Growth

Unlike the AlGaAs system, SiGe structures inherently involve strain, as the lattice parameter of Ge is 4% larger than that of Si. Thus, $Si_{0.75}Ge_{0.25}$ strain-relaxed buffer layers provide a template for silicon growth resulting in silicon with biaxial tensile strain of about 1%. As a result, the cubic symmetry of Si is broken and the six conduction band valleys are no longer degenerate. In the case of biaxial tensile strain, the two perpendicular Δ_2 valleys having electrons with a light in-plane effective mass are lower in energy than the four in-plane Δ_4 valleys with a

heavy in-plane effective mass, and the energy level of the lowest two Δ_2 valleys is lower than that of the conduction band in bulk SiGe. Thus, the quantum well formed in such a strained Si layer is occupied by light effective mass electrons. Because of the large energy splitting of the conduction band valleys, intervalley scattering is also reduced, resulting in higher electron mobility.

One challenge in attaining high mobility Si/SiGe heterostructures is to minimize the threading dislocation density arising from the lattice mismatch between Si and SiGe. Since bulk SiGe substrates are not available, structures with strained Si layers having a high mobility two-dimensional electron gas are achieved by first growing a strain-relaxed SiGe buffer layer on a Si(001) substrate, which provides a "virtual substrate" for the growth of a pseudomorphic Si layer under biaxial tensile strain. When a $Si_{0.7}Ge_{0.3}$ layer is grown directly on Si(001), strain-induced roughening occurs, leading to the random nucleation of misfit dislocations and a threading dislocation density on the order of 10^{10} cm^{-2}.[18] In contrast, at lower mismatch strain, e.g., SiGe $x = 0.15$, the surface remains flat and dislocation nucleation takes place by a multiplication mechanism that results in much lower threading dislocation densities. The strain-relaxed buffer layer typically used for modulation-doped field-effect transistors (MODFETs) is a thick structure in which the Ge concentration is increased linearly or in small steps up to 25 or 30% plus a thick uniform composition $Si_{0.7}Ge_{0.3}$ layer. Grading allows dislocation nucleation to occur at low mismatch strain and threading dislocation densities are reduced to the 10^5–10^8 cm^{-2} range, depending on the grading rate and growth conditions.[18] A strained Si quantum well is grown on this virtual substrate and is then modulation doped by capping with a thin intrinsic alloy layer, followed by a P-doped alloy layer, and finally a thin Si layer as shown in Fig. 1(a). For some experiments, the strained Si quantum well is grown with isotopically pure ^{28}Si.

To obtain high mobility, scattering must be minimized. Scattering is induced by local changes in electric field and strain, as well as interfacial roughness on short length scales. Increasing the setback of the donors from the well decreases Coulomb scattering, increasing mobility until other scattering mechanisms are dominant. It has been shown that threading dislocation densities that exceed 3×10^8 cm^{-2} reduce the electron mobility in modulation-doped strained Si.[19] Additionally, the strained Si layer must be below the critical thickness for misfit dislocation formation at the Si/SiGe interface to avoid scattering.[20] Roughening of the surface of the SiGe virtual substrate, the so-called cross-hatch roughness, is inherent in the strain relaxation process.[18] This roughness appears as interface roughness in the pseudomorphic layer structure that forms the 2DEG,
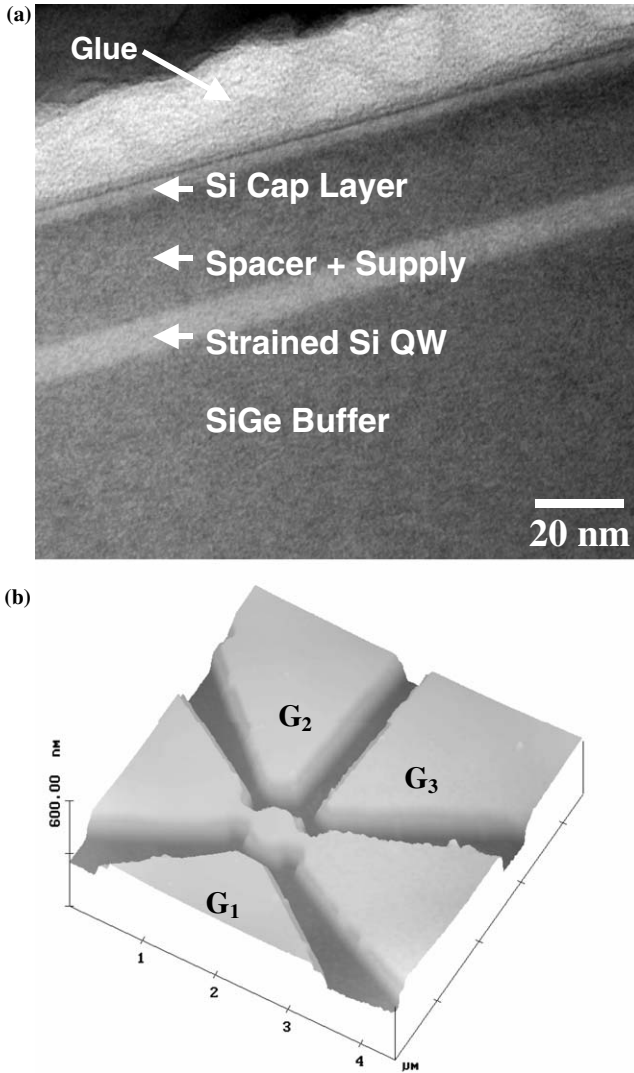
Fig. 1. (a) Cross sectional TEM image of the modulation-doped layer structure. The strained Si quantum well is grown on a uniform composition $Si_{0.7}Ge_{0.3}$ layer, which is grown on top of a step-graded buffer layer (not shown). The spacer and supply layers are also $Si_{0.7}Ge_{0.3}$. (b) AFM image of an etched dot fabricated from the heterostructure shown in (a). Three 2DEG side gates are visible.

specifically the strained Si quantum well. Fortunately, the length scale of this roughness is long enough that it does not reduce the electron mobility.[21] Low temperature electron mobility in the range of $1–6 \times 10^5 \, cm^2/V \, s$ has been achieved in modulation-doped strained Si/SiGe structures grown epitaxially by various growth methods.[22–25]

In addition to low temperature 2DEG and quantum dot formation, these developments are also critical for non-cryogenic applications. The room temperature electron mobility in modulation-doped strained Si structures is typically $2000–2800 \, cm^2/V \, s$, about 3–5 times that in n-type Si metal-oxide semiconductor field-effect transistors (MOSFETs). Thus, faster transistors are anticipated using strained Si structures, provided the device dimensions remain favorable. High-speed modulation-doped field-effect transistors (MODFETs) have been fabricated with Si/SiGe layer structures.[26] Recently MODFETs having 70–79 GHz f_T and record 194 GHz f_{Max} at room temperature were reported.[27]

2.2. Quantum Dots

A critical challenge for single-electron strained Si dots is the fabrication of high quality Schottky contacts on Si/SiGe heterostructures. Although it is relatively easy to fabricate large barrier Schottky contacts on silicon, it is challenging to create ultra-low leakage contacts on Si/SiGe heterostructures, due to the proximity of high P doping (typically $> 10^{19} \, cm^{-3}$) near the interface of the gate electrode.[28] Possible alternative approaches are the use of dielectric films to create metal–insulator–semiconductor (MIS) structures and the relocation of the P-doped supply layer underneath the Si quantum well. Bottom doping has been demonstrated by MBE growth techniques, but for CVD this is extremely difficult to achieve due to memory effects associated with phosphorous doping from PH_3.[28]

A second strategy is to avoid metal top-gates entirely, and instead to use 2DEG side gates, separated from the active region of the device by etch trenches. We have observed Coulomb blockade in such quantum dots with multiple gates to independently control the tunneling to the leads as well as the overall electron occupation of the quantum dot.[29] Quantum dots are fabricated by electron beam lithography and subsequent CF_4 reactive-ion etching. An AFM image of such a device is shown in Fig. 1(b). The electron density in the 2DEG from which the dot was formed is $4 \times 10^{11} \, cm^{-2}$ and the mobility is $40,000 \, cm^2/V \, s$ at 2 K. Ohmic contacts to the 2DEG are formed by a Au/Sb alloy. Figure 2 shows a Coulomb blockade trace at $T = 1.8 \, K$. Control of the dot electron population and the lead resistances is achieved with three separately
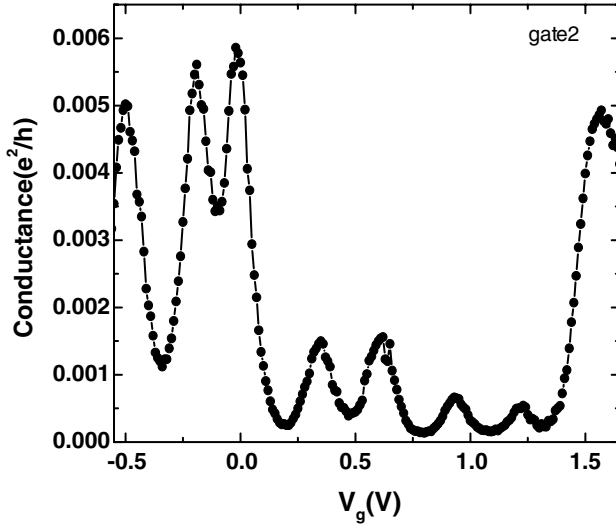
Fig. 2. Coulomb blockade trace for the dot shown in Fig. 1(b). The temperature was 1.8 K, and the gate voltage V_g was applied to gate 2.

tunable gates. Each gate is fabricated from the same 2DEG from which the quantum dot is created. Such in-plane coupling of one 2DEG to another has been used to monitor the electron population in GaAs quantum dots.[12] Here we have inverted this idea and used the 2DEG–2DEG coupling to control the dot.

Etched gates are very effective for individual dots, and can likely be used by themselves to create two coupled quantum dots. However, due to the relatively large size of 2DEG side gates it is likely that truly metallic top-gates will be required to couple many dots together. A second important challenge is the achievement of low charge noise. Switching events in the dot shown in Fig. 1(b) occur on the time scale ~ 1 h (Note added in proof: recent advances have extended this time to more than 10 hours between switching events). Improving this charge noise is an important goal. It is known that the charge noise in some types of silicon quantum dots, for example, oxide confined dots, can be extremely low, allowing repeatable measurement over very long time periods.[30]

2.3. Valley States

As described above, strain in Si/SiGe heterostructures reduces the sixfold silicon valley degeneracy to twofold. This remaining twofold valley degeneracy is a potential complication in two-qubit gates mediated
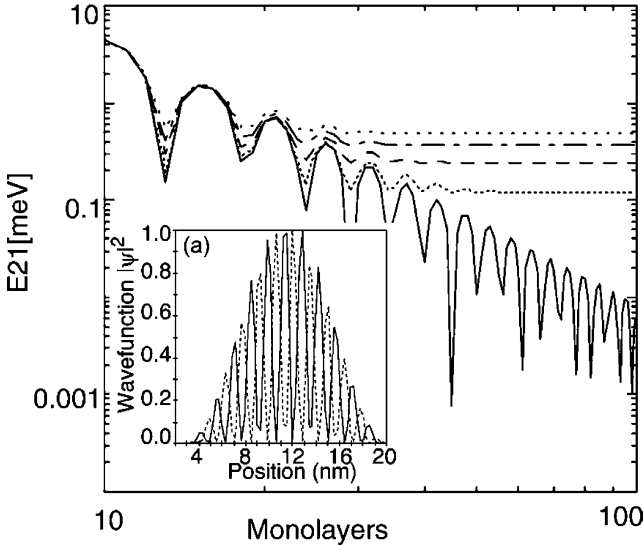
Fig. 3. Computed valley splitting E_{21} versus number of atomic monolayers in the quantum well. Solid line corresponds to zero applied field; oscillations reflect transitions of valley ground state from even to odd symmetry. Dotted and dashed lines correspond to finite applied E fields between 1–4 mV/nm. Inset: even and odd symmetry traces of tight-binding coefficients for a pair of valley split ground states.

by inter-dot exchange coupling.[1] Fortunately, the twofold valley degeneracy in strained silicon quantum wells is split by the quantum well confinement potential. As shown in Fig. 3, recent work has demonstrated that the valley splitting can be engineered both by varying the well width and by applying electric fields, and that the splitting, in some cases, can be quite large.[31] The valley splitting is most easily understood in the infinite square well limit. Because the valley minimum is not at the center of the Brillouin zone ($k = 0$), the electron wavefunctions experience atomic-scale modulations. In a semiconductor with two degenerate valleys, the oscillations of the two lowest energy states have very similar envelopes, but are out of phase by 90°. For an infinite square well, the energy eigenstates are linear combinations of four different k-values, yielding an energy splitting that decays as (width)$^{-3}$; the splitting for a 4 nm well is 1.5 meV. In nonzero electric field the potential is asymmetric, and the energy difference between the two lowest energy states increases with increasing external electric field.[32] Typical modulation doped heterostructures experience internal electric fields of order 10 mV/nm. In calculations involving isolated electrons in a quantum well, we obtain splittings larger than 1 meV— quite a large energy.[31]

A potential concern is whether the exchange coupling between two qubits will oscillate uncontrollably as a function of position, in analogy with donor-bound electrons in silicon.[33] In fact, the situation in strained silicon quantum dots is quite different. Because of strain, the charge density in the plane of the quantum well does not have atomic-scale oscillations. Perpendicular to the quantum well the oscillations self-align because of the presence of the strong confining heterostructure potential. Because the length scale of the quantum well potential is so much shorter than that of variations in the quantum well plane, the Born–Oppenheimer approximation is appropriate and immediately shows that the oscillations in charge density perpendicular to the quantum well plane follow any slow variations in quantum well width and position.[34]

It is important to mention that it is also possible to view valley degeneracy as a resource. It may be possible to use valley states rather than spin states to store quantum information. Such states would be charge qubits with little difference in charge distribution for the two states, possibly leading to weak decoherence. In a different approach, using spin, conceivably one could access all low-lying eigenstates to form a four-dimensional qubit Hilbert space.

2.4. Tolerance to Impurities

For scalable QDQC, it is important that quantum dot exchange couplings be tolerant to the presence of low concentrations of impurities. It is well known that charged impurities such as ionized donors cause scattering effects which limit the 2DEG mobility.[20,35] These charges also have some effect on electrostatic control of qubit gate operations. However, a more important issue from the standpoint of decoherence and scalability is the influence of neutral dopant impurities like P in Si and Si in GaAs. Such impurities can potentially act as renegade qubits, siphoning off quantum information in an uncontrolled way. When the exchange coupling between qubit and impurity becomes large enough, fault-tolerant quantum error correction schemes[36,37] are no longer effective. Such donor-bound spins are abundantly present in the modulation-doped supply layer of semiconductor 2DEGs, and they also occur at low densities throughout the sample.

To investigate this issue, we have computed the qubit-impurity exchange coupling J for two cases:[38] an impurity in the supply layer, and an impurity in or near the quantum well. In the first case, due to the potentially large numbers of neutral donors in the supply layer, the important quantity is the distance between the supply layer and the quantum well. We obtain the following minimum set-back distances between the

quantum well and the supply layer: 18 nm for Si in GaAs and 8 nm for P in Si. These numbers are only weakly dependent on the details of the structure or on the choice of fault-tolerance schemes and error correction coding, because of the exponential dependence of the exchange coupling on qubit-impurity separation. The results do depend on choice of barrier materials and, in particular, on the height of the quantum well barriers. Fortunately, these distances are consistent with typical experimental set-backs of ~ 20 nm for GaAs and ~ 10 nm for Si.

We have also studied the effect of impurities in or very near the quantum well. We find that impurity spins near the quantum well pose a threat to qubits at a distance of ~ 100 nm for Si in GaAs and ~ 60 nm for P in Si. The results are somewhat sensitive to specific details of the qubit confinement potential. A crucial observation, from the perspective of scalability, is that the computed impurity danger zones are approximately equal to the radius of a single electron dot. That is, a single impurity can only kill one, or at most two qubits in a 1D array. Therefore, a modest amount of parallel connectivity would enable scalable computations, provided the impurity density is somewhat smaller than the qubit density. We can estimate this critical impurity density by assuming that only impurities near the quantum well can trap electrons. For Si in GaAs the critical density is about 1.0×10^{15} cm^{-3} (assuming a 25-nm quantum well), while for P in Si the density is 1.6×10^{16} cm^{-3} (assuming a 6-nm quantum well). Both of these impurity density limits are achievable in good materials.

2.5. Decoherence

Silicon-based quantum dots have the compelling attribute that the spin coherence time T_2 can be very long. The reasons for long coherence times are the availability of the spin-zero ^{28}Si isotope, use of which greatly reduces relaxation via nuclear spins (hyperfine coupling), and silicon's small spin–orbit coupling (SOC), which suppresses phonon and SOC-based decoherence mechanisms.

Each electron spin $\mathbf{S}$ interacts with all nuclear spins $\mathbf{I}_i$ with which it overlaps spatially. As pointed out in Refs. 39 and 40, in the QC operational regime the external magnetic field B will exceed 100 gauss, so that electron spin-flips accompanied by one nuclear spin flip are not allowed energetically. This suppresses the single-spin-flip mechanism considered in Refs. 41 and 42, and the dominant ESR relaxation mechanism becomes spectral diffusion.[40] Measurements[43] and theory[40] have made it clear that in the spectral diffusion regime the relaxation rate increases with the density of the nuclear moments.

Natural Si has isotopic fractions 95.33% spin 0 (mostly ^{28}Si and a small fraction ^{30}Si) and 4.67% spin 1/2(^{29}Si). Spins in naturally occurring silicon have T_2 in the range 0.1–1 ms at low temperatures, and the dominant source of decoherence is coupling to the ^{29}Si nuclei.[44] (One must note here that the decay of spin echoes is not purely exponential, and more than one time scale may enter.) Measured T_2 values for low doped isotopically purified ^{28}Si are substantially longer.[45] In 1958 Gordon and Bowers [44] observed a T_2 of around 0.5 ms at 1.4 K for phosphorus-doped isotopically pure ^{28}Si, versus 0.24 ms for similarly doped natural Si:P. Tyryshkin *et al.*[45] recently compared T_2 times with different doping levels in isotopically pure silicon. Below 12 K the relaxation time T_2 in isotopically pure ^{28}Si was as large as 3 ms. Furthermore, by comparing different doping levels and attributing the remaining linewidths to a magnetic dipole–dipole interaction of neighboring phosphorus donors (via instantaneous diffusion),[46,47] they extrapolated from their data $T_2 = 62$ ms (at 7 K) for isolated donors in ^{28}Si. The presence of non-zero nuclear spin isotopes clearly results in shorter electron spin coherence times.

Electron spins in qubits can dephase even while in contact with a bath at zero temperature, because the quantum computer itself is not in equilibrium, and excited states are populated. Because of spin–orbit coupling, there is an effective spin–phonon coupling, and spins can flip by spontaneous emission of phonons. This process contributes to the relaxation rate T_1^{-1}, which is usually a lower bound to the decoherence rate T_2^{-1}. Generally, transition rates are proportional to $(g-2)^2$. This leads to very long T_1 and T_2 values in Si donor states,[48] and these favorable numbers are expected to extend also to dot-confined electrons.[49] Additional spin–orbit mixing due to the Rashba field,[50] typically prevalent in asymmetrically doped semiconductor heterostructures, is also expected to be quite weak in silicon.[51] Thus, spectral diffusion should be the predominant decoherence limiting mechanism in silicon QDQC.

For electrons in a Si/SiGe 2D electron gas, Tyryshkin *et al.*[52] have measured $T_2 = 2.98\,\mu$s in a sample with a phosphorus delta-doping layer above the well that was illuminated and thermally annealed. The relatively short decoherence time is due to the increase in scattering mechanisms in a mobile, 2D electron system, as explained recently in the context of Rashba spin–orbit coupling and the D'yakanov/Perel' (DP) spin-relaxation mechanism.[53] Confinement of the electrons laterally in a quantum dot suppresses the dominant 2DEG relaxation mechanism, greatly increasing the coherence time.[54–60] Since there should be very few phosphorus donors within the well to contribute to magnetic dipole–dipole driven instantaneous diffusion, quantum dots fabricated in

isotopically pure small ^{28}Si quantum wells in principle should have better coherence times.

2.6. Bandwidth Issues

It is important to note that bandwidth in quantum computing is limited on both the high and the low end. At low frequencies, decoherence forms a fundamental, yet device dependent limit. As we have seen, the natural decoherence timescale for a SiGe QDQC should be ~ 10 ms. Threshold theorems for fault-tolerant quantum computing vary according to qubit architectures and coding sophistication.[37] In particular, schemes have been devised for local gates,[61] and can even be extended to 1D arrays with nearest-neighbor coupling.[62] Nonetheless, the exact probability threshold for fault tolerance in a QDQC is not available yet. Somewhat arbitrarily, we estimate it here as 10^{-6}–10^{-4}. Thus, quantum gate operations must be at least as fast as 0.01 to 1 μs in SiGe. Furthermore, fault-tolerance requires that readout and initialization steps must be performed at these same speeds. This does not imply that spins cannot be read out at much slower speeds, only that high speeds are required for scalability.

High-bandwidth constraints include non-adiabatic gating effects,[63,64] and sensitivity limits for readout. Based on shot noise analysis, the upper bound[65,66] on detection sensitivity for charge induced on the island of an optimized rf-SET (the lowest noise detector currently available) is about 4×10^{-6} e/$\sqrt{\text{Hz}}$. Simulations suggest that fast readout and initialization in SiGe can meet the stringent high and low-bandwidth criteria,[8] but experimental confirmation of this result is required.

The technical criteria for scalable QDQC are also challenging. On the low-bandwidth side, computations should be completed at speeds consistent with laboratory or human timescales (probably less than days!). If the necessary structures can be built, this limit is not a problem for solid state QC implementations. However, high-bandwidth technical limits are set by control and measurement electronics. We mention here a single example, discussed in Refs. 67 and 68. In these papers, we investigated the control sensitivity of the exchange coupling J to voltage pulses ΔV for particular SiGe devices. We found that, because of the exponential dependence of J on ΔV in typical architectures, small fluctuations in ΔV produced relatively large errors in J. As consistent with fault tolerant computing, the total exchange pulse (consisting of J integrated over pulse time Δt) should have an error less than 10^{-3}–10^{-2}.[69] However, the accuracy of control electronics is strongly sensitive to bandwidth, in terms of both the height and width of the pulse. As shown in Fig. 4, using specially designed
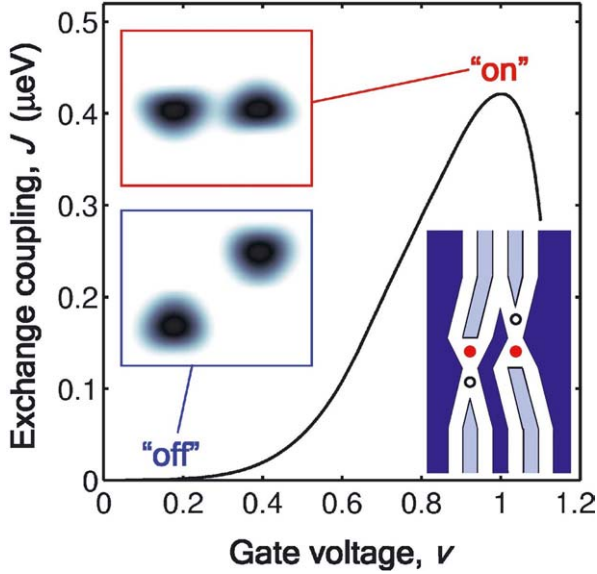
Fig. 4.   Computed exchange coupling as a function of reduced gate voltage. The pseudo-digital technique allows a flat-top working point to replace the usual exponential dependence of $J(v)$. Lower right: pseudo-digital top-gate scheme for coupled double dots, each with a single electron. Upper left: computed electron densities for "off" and "on" configurations.

"pseudo-digital" dot architectures greatly decreases the electronics requirements in these simulations.

3. OUTLOOK FOR QUANTUM DOTS

As described above, recent advances point to a promising future for QDQC. Nonetheless, important challenges remain. A major goal for silicon 2DEG-based quantum dots is the fabrication of highly tunable, coupled dots, and the demonstration of spin measurement. A challenge for quantum dots in all materials is connectivity: is it possible to develop systems that are more highly connected than linear arrays? It is well known that such connectivity is an important aid in algorithm and error correction development, and there is an inverse relation between connectivity and resource requirements and operating timescales. Recent advances show that coupling between dots need not be highly localized.[70] Perhaps the greatest challenge is the development of long-distance couplings between qubits. Although not required, such couplings would be a great benefit

to QDQC. Cross-fertilization from other QC disciplines should play an important role in meeting this challenge.

ACKNOWLEDGMENTS

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