A 1GHz Signal Bandwidth 4-Channel-I/Q Polyphase-FFT Filter Bank

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***Abstract*—This paper presents a prototype analog 4-channel-I/Q polyphase-FFT filter bank (PFFB) using passive switched capacitor circuits to channelize wideband signals. Like FFTs, the proposed PFFB shares computations for low power. The PFFB allows for a longer "effective window length" than is possible in a standard FFT. This characteristic of the PFFB maintains a narrow main-lobe bandwidth combined with low side-lobe amplitudes. The passive switched capacitor structure enables high linearity and low power implementation. The measured performance of the prototype fabricated in TSMC 65nm CMOS shows >40dB side-lobe suppression, +25dBm IIP3, and 208μV_{rms} integrated output noise for all channels at 1GS/s operation. The total power consumption for the PFFB (8-channels total) is 34.6mW (34.6pJ/conv).**

I. Introduction

The continued increase in data requirements for wireless terminals will eventually necessitate the use of wider signal bandwidths. This is already evident with WiFi and LTE where channel banding and carrier aggregation have already been deployed. Additionally, we see that the air channel is a limited resource that has largely been allocated. However, the amount of actual usage is often very low [1]. Hence, it is desirable to detect any unused spectrum and exploit it for wideband signaling.

To handle wideband signals and to detect the available spectrum, it is critical to process wide bandwidths which often contain multiple narrowband signals with different center frequencies and amplitudes. A single ADC could, in theory, be employed but would require both a wide bandwidth and a large dynamic range due to the large peak to average power ratio (PAPR) resulting in larger power consumption [2]. One technique to tackle this problem is to channelize the wideband input signal into separate narrow bands using a mixer bank [3]. However, this channelization structure consumes considerable power and has a limited dynamic range due to mixer spurs.

We propose an alternative efficient and high performance channelization structure using a filter bank that swaps the mixer and filter locations and replaces the mixer with down sampling as shown in Fig. 1. As can be seen in Fig. 1, we now need complex filters instead of simple ones. The VGAs that follow channelization allow for additional gains in channels that have small amplitudes, which results in a smaller relative quantization error for small signals so that a nearly constant SNR per filter bank channel is maintained. In [4], the filter bank was realized using a passive charge domain radix-2 analog-FFT (A-FFT) which was extremely power efficient due to its zero static power consumption and efficient FFT structure [5]. Additionally, the FFT channelization allowed for easy reconstruction using an inverse FFT. However, the simple rectangular window based structure resulted in only

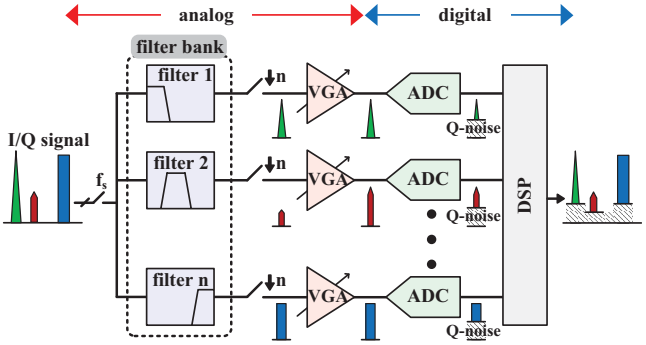


Fig. 1: Filter bank based channelization structure

-13dB adjacent channel isolation. To mitigate this issue, a windowing-FFT can be employed [6]; however, as is well known for windowing functions, it results in a wider main-lobe bandwidth [7].

In this paper, a prototype analog polyphase-FFT filter bank (PFFB) using passive charge domain switched capacitors is presented for the channelization of wideband signals. The polyphase implementation allows for an arbitrary window length, thus breaking the side-lobe suppression vs main-lobe bandwidth tradeoff in traditional FFTs. Additionally, the efficient implementation of the FIR based filter bank derived from well-known windowing functions achieves a high dynamic range, good power efficiency and good linearity. As shown later, stop band attenuation for a simple PFFB structure is comparable to IIR filters (5^{th} order Chebyshev in our design). Also, a linear phase response due to the FIR filter characteristic does not introduce phase distortion at the band edges and also allows for the reconstruction of the original signal in the digital domain after A/D conversion [8].

II. 4-Channel-I/Q Polyphase-FFT Filter Bank

In this section, we describe the inner workings of the polyphase-FFT filter bank. In our 4-channel prototype design, we use a 13-tap window for the FIR low-pass filter that precedes the A-FFT. Fig. 2(a) shows the 13-tap weights, $[W_0, W_1 ... W_{12}]$, that are convolved with the input, $x[n]$, to result in the output, $y_0[n]$. The center frequency of the filter can be shifted by applying a phase rotation in the time domain as shown in *Eq.(1)*. The bottom sub-figure in Fig. 2(a) shows the result of a frequency shift by $f_s/4$ (see $y_1[n]$ and $y_1(f)$).

$$F^{-1}\{X(f-f_0)\} = x(n)\cdot e^{j2\pi\frac{f_0}{f_s}n} \quad (1)$$

The frequency translated window coefficients can be transformed into a polyphase form as shown in Fig. 2(b) [9]. Here, the input signal is successively delayed and down-sampled by 4 to guarantee the same function. An important property of

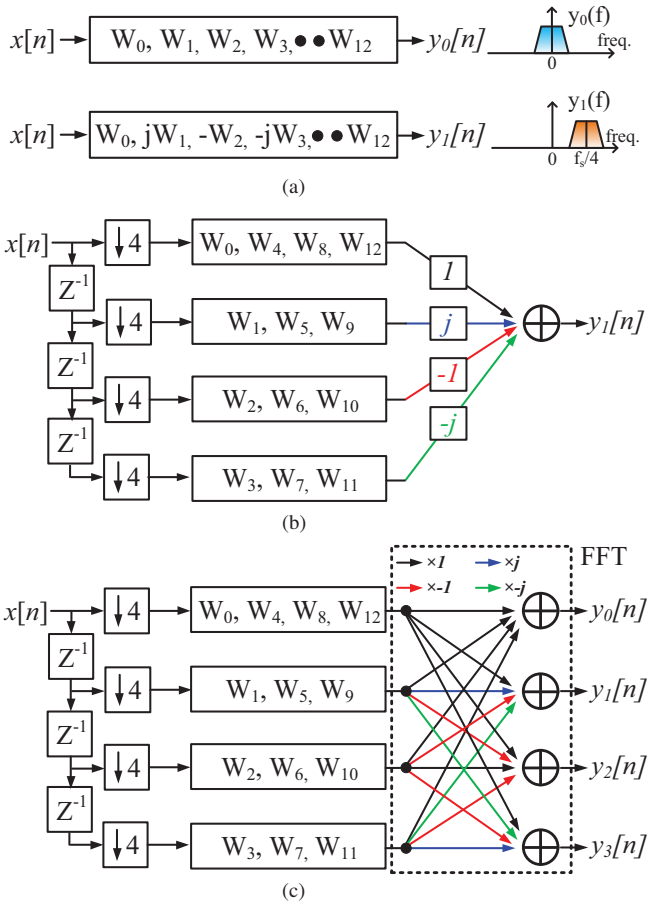


Fig. 2: (a) 13-tap FIR low-pass filter and its frequency shift by $f_s/4$ (b) Polyphase window form of frequency shifted FIR filter (c) Structure of polyphase-FFT filter bank

this polyphase window form is that a common phase value per channel is applied at the end after the window function. Using this property, the center frequency of the arbitrarily long window coefficients can be shifted efficiently. This transformation can be equally applied to other center frequencies at $k \cdot (f_s/N)$ where N is the number of channels and k $\in$ [-N/2+1 : N/2]. For the 4-channel design, we perform these frequency translations at $-\frac{f_s}{4}, 0, \frac{f_s}{4}, \frac{f_s}{2}$. Fig. 2(c) shows the structure that simultaneously generates the filter bank outputs at the 4 separate center frequencies. In this structure, the outputs of the polyphase window are added together with different phase rotation steps for each output. This phase rotation is identical to that of a discrete Fourier transform and can be implemented efficiently as a FFT. This overall structure, which consists of the polyphase widow and the FFT, results in an extremely efficient design due to sharing of the computations, not unlike that in a traditional FFT.

Fig. 3(a) shows the 13 window coefficients used for this 4-channel PFFB. The coefficients were generated by a convolution of a 10-tap, 5-bit resolution Chebyshev filter and a 4-tap rectangular window. Fig. 3(b) shows the resulting four outputs that are equally spaced from $-f_s/2$ to $f_s/2$. We note that there is an overlap in the frequency bands, which is necessary for

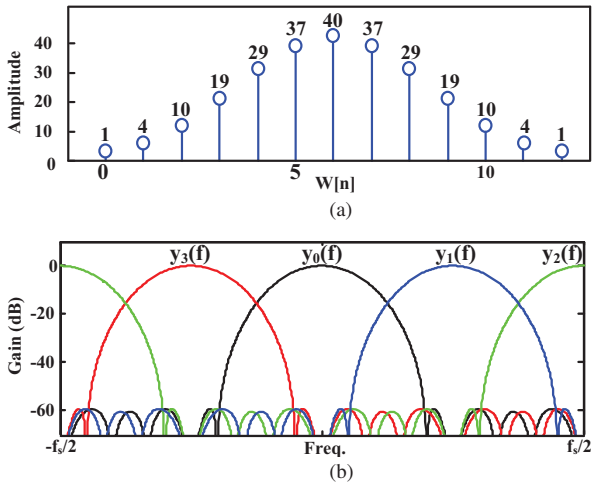


Fig. 3: (a) 13-tap window coefficients (b) Frequency response of PFFB

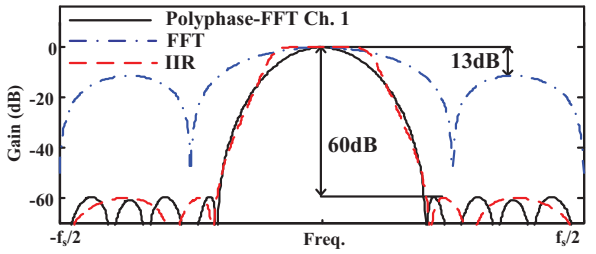
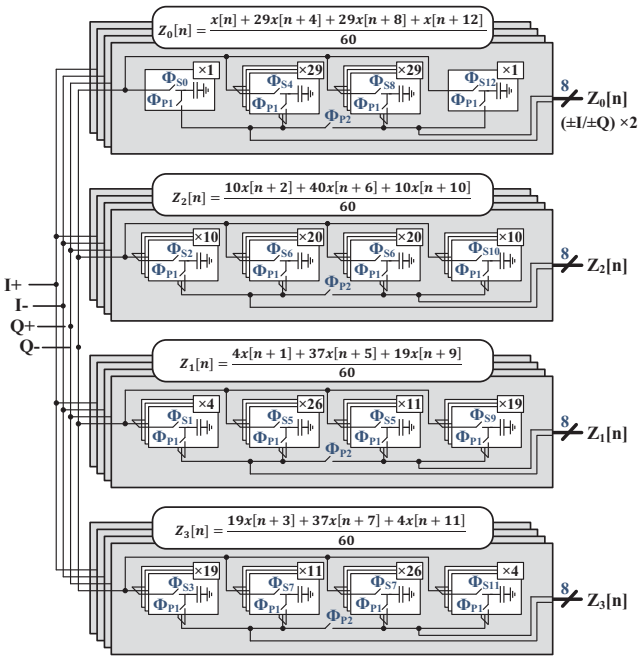


Fig. 4: Comparison of frequency responses of PFFB, FFT and IIR

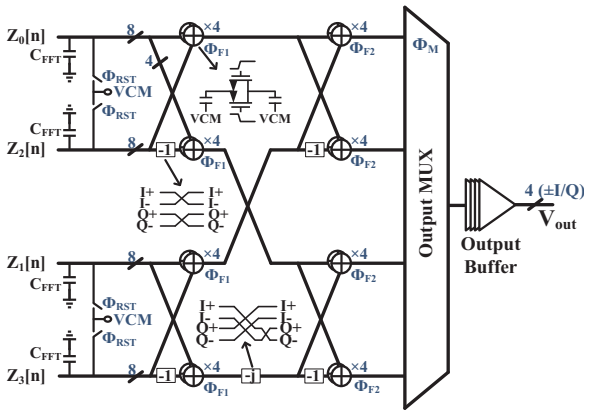
reconstruction. Compared to a standard FFT where the length of the window coefficients is limited to the number of channels [6], the PFFB can have an arbitrary length for the window coefficients, so it can maintain a narrow main-lobe bandwidth and low side-lobe amplitudes as well as retain a linear phase due to its FIR characteristic. Fig. 4 shows a comparison with other filter responses (a standard FFT with a 4-tap rectangular window and a 5th order IIR Chebyshev II filter). As can be seen, the PFFB side-lobes are -60dB, not unlike the IIR filter, while the side-lobes for a standard FFT are -13dB. We also note that the main-lobe is narrower than that for a standard FFT.

III. Circuit Implementation

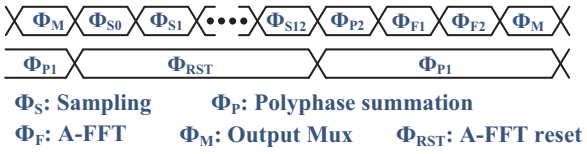
For high speed and low power implementation, a prototype analog 4-channel-I/Q PFFB was designed using passive switched capacitor circuits. Fig. 5(a) shows the schematic diagram of the analog polyphase summation. The related clock sequences are shown in Fig. 5(c). In this block, I/Q input signals are sampled on different numbers of 9fF unit capacitors during 13 sampling clock phases (e.g., 10 unit capacitors at Φ_{S2}). At the same time, the input capacitances of the A-FFT in Fig. 5(b) are reset to VCM to eliminate any history effects. The number of unit capacitors during each sampling phase corresponds to the window coefficient as shown in Fig. 3(a). After the sampling phases, the sampled values are shared for the polyphase window summation during Φ_{P1} and Φ_{P2}. Due



(a) Schematic diagram of polyphase summation



(b) Schematic diagram of 4-channel A-FFT



(c) Clock sequence of analog PFFB

Fig. 5: Schematic diagram of analog PFFB and its clock sequence

to the different number of sampling capacitors, the window coefficients are implemented after the sharing operation. The A-FFT in the next stage requires 2 copies of each input for the butterfly operation so the 60 shared capacitors of each path (e.g., 1, 29, 29, 1 capacitors in the top slice of Fig. 5(a)) are separated into two halves after the falling edge of Φ_{P2}. Each path of the polyphase summation output consists of 8 pairs (2 copies of ±I, ±Q) of capacitors where each capacitor is composed of 30 "unit capacitors" with a total value of 270fF.

The polyphase summation outputs, $Z_m[n]$ where m ∈ [0:3],

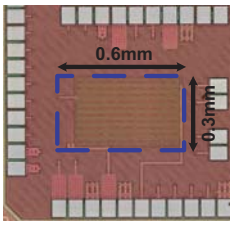


Fig. 6: Die photo

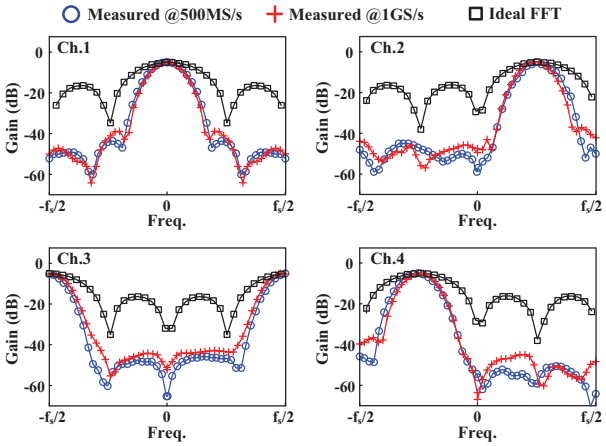


Fig. 7: Frequency response of 4-channel PFFB

are connected to the input of the A-FFT as shown in Fig. 5(b). The A-FFT is implemented in a radix-2 structure and it works during the Φ_{F1} and Φ_{F2} phases with charge sharing for addition and a swapping of signal lines for "negation" and "multiply by -j" operations. The output of the A-FFT is connected to an on-chip output MUX and a source follower buffer that were included for testing purposes only.

In this design, signal information is stored as charge in the capacitors, so it is vulnerable to distortion by coupling from an adjacent clock or other signal lines. Additionally, the coefficient values depend on the total sampling capacitance including any parasitic capacitance due to signal routing. To mitigate these issues, the layout was done symmetrically with ground shielding for all signal lines. For the entire structure, a total of 960 unit capacitors and sampling switches are used for differential I/Q signals and each sampling switch is bootstrapped for high linearity [10].

IV. Measurement Results

The proposed PFFB, implemented in TSMC's 65nm GP process, is shown in Fig. 6. The active area, including the output MUX and buffer for testing, is $0.18mm^2$.

Fig. 7 shows the measured frequency responses and is compared to that of a standard FFT. The source follower's finite gain is calibrated out. As expected, the measured results show a narrower main-lobe width and lower side-lobe amplitudes than for the FFT. To evaluate the effect of the operating frequency, the design was tested at different sampling frequencies. Specifically, the side-lobe amplitudes are -43dB and -40dB at 500MS/s and 1GS/s, respectively. These are 30dB and

TABLE I: Summary of performance

	This work	[11]	[12]	[13]	[14]	[15]
Tech(nm)	65	45	130	65	90	500
No. of tap	13	16	9	4	5	6
No. of channel	4 x I/Q	1	1	1	1	1
Useful signal bandwidth(GHz)	1.0	0.8	0.014*	0.05*	0.25*	0.09
Power/channel(mW)	4.25	48	15.7	12	16.6	160
Sampling speed(GS/s)	1.0	3.2	0.64	2.4	2.0	0.36
Side lobe(dB)	-40	-30	-66	-40	-42	-10
Gain(dB)	-5	0	30	0	29	0
Linearity	25.3dBm IIP3	-50 HD3	-17dBm IIP3	NA	-22dBm IIP3	-42 HD3
IRN (dBm/Hz)	-146	NA	-156	NA	-155	NA

* -3dB bandwidth

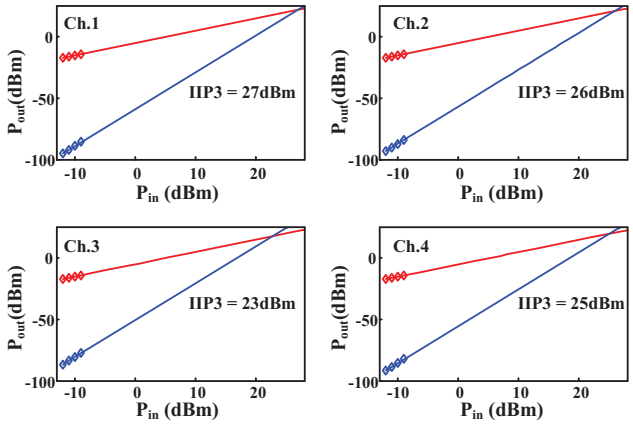


Fig. 8: IIP3 of 4-channel PFFB

27dB better than for a standard FFT (-13dB). The performance degradation from the ideal value, -60dB side-lobe, is caused by the capacitance mismatch resulting in window coefficients variation. At the higher sampling frequency, the performance degrades slightly due to a finite settling error and the effect of the bond wire on the input signal. The measured DC gain is -5dB. This is due to charge stealing by the input capacitance of the A-FFT during the Φ_{P1} phase.

The in-band IIP3 of each channel was measured using two tone signals with 100kHz spacing. Fig. 8 shows the measured results at 1GS/s. The average IIP3 of the 4 channels is 25.3dBm showing the benefits of passive switching [16]. The slightly lower IIP3 value at Ch.3 is caused by the higher frequency of the input signal and increased sampling error.

The measured total integrated output noise up to 1GHz is $208\mu V_{rms}$. This is equivalent to a noise power spectral density of -151 dBm/Hz. The 4-channel-I/Q (8 total) PFFB design consumes 34.6mW of power at 1GS/s output, i.e., it consumes 34.6 pJ/conv. The power consumption for a single channel is 4.33 mW. Table I summarizes the performance and compares it with other state-of-the-art FIR filters. With the proposed PFFB, we achieved high linearity, the lowest oversampling ratio, and the largest signal bandwidth at the lowest power per channel.

V. Conclusions

In this paper, a prototype analog 4-channel-I/Q polyphase-FFT filter bank was proposed. The proposed structure enables an arbitrary FIR filter bank with linear phase and low side-lobes unlike the passive higher order IIR architecture which can only implement real pole filters [16]. Due to its power-efficient algorithm and passive switching, it achieves low power and high linearity. The proposed structure can be employed for low power channelization of wide band signals particularly in software-defined cognitive radios and carrier aggregation.

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