CMOS Energy Efficient Integrated Radios for Emerging Low Power Standards

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Abstract— **This paper describes IEEE 802.15.6 standard compliant 2.36-2.484GHz transmitter and receiver frontends suitable for emerging low power standards. The transmitter digitally multiplexes the appropriate phases from an 800MHz poly-phase filter output to generate π/4 DQPSK signals at 2.4GHz. Modulation at 1/3rd the RF frequency reduces the total power consumption and enables channel selection using a PLL running at 800MHz. The prototype transmitter has an energy efficiency of 2.5nJ/bit at 1.2Mbps while delivering -10dBm RF power. The receiver uses a passive coupling based frequency translated mutual noise cancellation technique which allows for low supply operation thereby saving power. The FOM is 10dB higher than the state-of-the-art and the power consumption is 194μW which is 0.5X lower than the state-of-the-art.**

WBAN; 802.15.6; low power; injection locking; transmitter; receiver; noise cancellation

I. INTRODUCTION

With the proliferation of the Internet of Things the demand for low power radios continues to increase. This paper presents 802.15.6 compliant transmitter and receiver frontends. On the transmit side we propose a robust energy efficient architecture using a passive phase generation technique that utilizes sub-harmonic injection locking (IL). On the receive side we propose a frequency translated passive mutual noise cancellation technique that solves the power and noise figure issues normally found in sub 1V mixers.

II. ARCHITECTURE

A. Transmitter architecture

The block diagram for the proposed transmitter is shown in Fig. 1 [1]. A MUX-based architecture is proposed where modulation occurs at 800MHz (i.e. 1/3rd the RF frequency). A passive polyphase filter centered at 800MHz generates all the 8 phases necessary for π/4 DQPSK modulation at 2.4GHz. These phases are appropriately selected by the phase multiplexer (MUX) based on the digital baseband data. Modulation at 1/3rd the RF frequency reduces the power consumption and also enables us to employ simpler low power circuits which are difficult to operate at the higher RF frequencies. In addition channel tuning can be achieved by a PLL running at 1/3rd the RF frequency which further reduces power. A pulse slimmer enhances the third harmonic content at 2.4 GHz of the phase that is selected by the MUX. The ILO, tuned to 2.4GHz, locks on to this third harmonic and functions as both a high-Q bandpass filter and a frequency multiplier. Fig. 1 also shows the constellation at 800 MHz and 2.4GHz that is mapped by

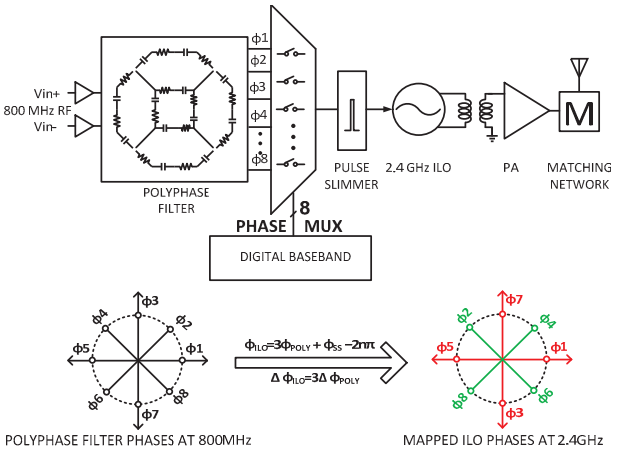

Fig. 1. Block diagram for the proposed transmitter.

this 3X frequency/phase multiplication. This design does not require capacitor bank calibration, can support a large number of channels even at high GHz frequencies and has no nonlinear phase mapping issues unlike existing IL techniques [2].

B. Receiver architecture

As shown in Fig. 2, we propose an active transconductance mixer requiring low LO power to achieve low Vdd operation [3]. The output SNR of a system can be expressed as $SNR_{out}=\epsilon VDD^2/N_{out}$, where $0<\epsilon<1$ and N_{out} is the output noise power. Low Vdd operation decreases the SNR_{out} and hence increases the effective noise figure. Additionally, lower power operation with devices operating in weak or moderate inversion increases the noise figure. Therefore, for low power operation noise cancellation techniques become essential.

In this paper, a frequency translated mutual noise cancelling (FTMNC) mixer is proposed. Unlike traditional techniques [4], we perform symmetrical noise cancellation of a fully differential structure where each path cancels the noise of the other side after downconversion to IF. The RF and LO is combined and applied to the mixer in differential form. A symmetric center tapped differential inductor couples the noise current of one side of the differential topology to the other side thereby making it common mode but retains the signal voltage in differential form. Each side has a transconductance mixer which downconverts the RF to baseband by generating in-phase IF signals which are added at the baseband. On the other hand, noise from each half, is in common-mode and gets downconverted out of phase (by +LO and −LO) and hence gets cancelled due to the addition after frequency translation.

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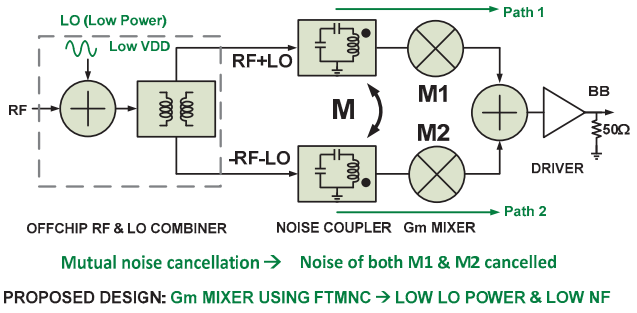

Fig. 2 Block diagram for the receiver frontend.

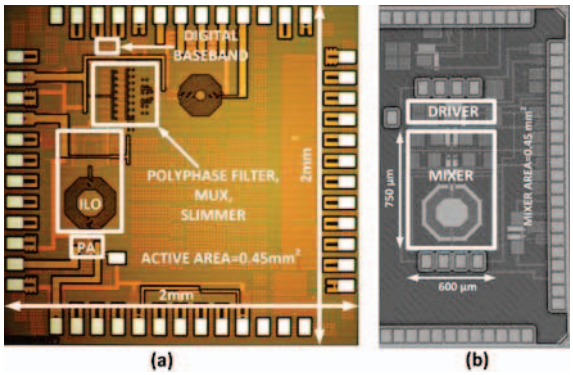

Fig. 3. Die-micrograph of transmitter and receiver frontends.

III. Measurements

The transmitter was implemented in IBM's 130nm CMOS technology. Fig. 3 (a) shows the die micrograph. The measured RMS EVM for π/4 DQPSK modulation is 3.21% as shown in Fig. 4. The complete transmitter including estimated PLL power can be implemented with a power consumption of roughly 3mW resulting in a 2.5nJ/bit efficiency which is 1.5X lower than the state-of-the-art [5]. The receiver frontend was implemented in TSMC's 65nm CMOS technology. Fig. 3 (b) shows the die micrograph. The proposed circuit has a noise figure of 6.55dB while consuming the lowest power of 194µW from a 0.7V Vdd in comparison to state-of-the-art. The proposed design has the highest FOM of 31dB which is 10dB higher than the state-of-the-art [6]. Fig. 5 shows measured and simulated noise figures for the receiver with and without noise cancellation.

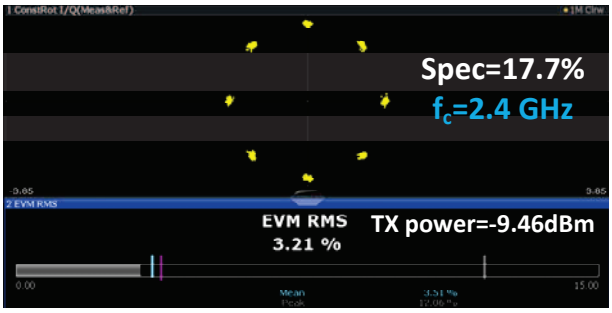

Fig. 4. Measured EVM of transmitter output at 2.4GHz.

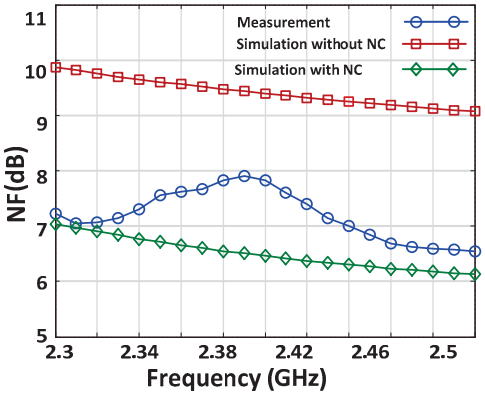

Fig. 5. Measured and simulated NF with and without NC.

IV. Conclusions

Modulation at 800MHz i.e. 1/3rd the RF frequency using a sub-harmonic injection locking technique results in a simple and low power design. Additionally, operating the PLL at 800MHz for frequency synthesis results in improved energy efficiency. The design is flexible and can incorporate other harmonics provided the phase mapping is appropriately thought through. Though the techniques developed here have focused on the 802.15.6 standard they are easily portable to other emerging low power standards with potentially tighter specifications.

On the receive side, the frequency translated mutual noise cancellation technique proposed here improves the noise figure and power consumption of sub 1V mixers. This allows for the development of extremely low power receivers. The proposed noise cancellation technique is mutual where one path cancels the noise of the other and vice-versa. The mixer has the lowest noise figure and power consumption in comparison to the state-of-the-art and its FOM is 10dB higher than the state-of-the-art.

References

[1] M. Rahman, M. Elbadry and R. Harjani, "An IEEE 802.15.6 Standard Compliant 2.5 nJ/Bit Multiband WBAN Transmitter Using Phase Multiplexing and Injection Locking," IEEE JSSC, vol. 50, no. 5, pp. 1126-1136, May 2015.

[2] S. Diao et al., "A 50-Mb/s CMOS QPSK/O-QPSK Transmitter Employing Injection Locking for Direct Modulation," IEEE TMTT, vol. 60, no. 1, pp. 120-130, Jan. 2012.

[3] M. Rahman, R. Harjani, "A Sub-1-V 194-µW 31-dB FOM 2.3–2.5-GHz Mixer-First Receiver Frontend for WBAN With Mutual Noise Cancellation," IEEE TMTT, vol. 64, no. 4, pp.1102-1109, April 2016.

[4] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "Wideband Balun-LNA with Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling," IEEE JSSC, vol. 43, no. 6, pp. 1341–1350, June 2008.

[5] Liu, Y-H, et al., "A 1.9nJ/b 2.4GHz multistandard (Bluetooth low energy/Zigbee/IEEE802.15.6) transceiver for personal/body-area networks," IEEE ISSCC, Feb. 2013.

[6] J. Deguchi, D. Miyashita, and M. Hamada, "A 0.6V 380µW -14dBm LO-Input 2.4GHz Double-Balanced Current-Reusing Single-Gate CMOS Mixer with Cyclic Passive Combiner," in IEEE ISSCC, Feb 2009, pp. 224–225.