A Smart-Offset Analog LDO with 0.3V Minimum Input Voltage and 99.1% Current Efficiency

Saurabh Chaubey and Ramesh Harjani
University of Minnesota, Minneapolis, MN 55455, Email: harjani@umn.edu

***Abstract*—In this paper we present the first fully integrated analog LDO (low dropout regulator) for sub-0.5V supply voltages. The LDO can operate from 0.3V-to-1.0V input voltage, and can sustain a load variation of 10mA-to-100mA at 1.0V input and 5mA-to-25mA at 0.3V input. It achieves a peak 99.1% current efficiency for a 100mA load at 0.9V output voltage. In order to realize the gate drive at sub-0.5V supply voltages, we introduce a negative charge pump based adaptive offset before the pass FET which provides gate-source headroom at input operation voltages normally reserved for digital LDOs. The smart-adaptive-negative offset voltage follows a 0.5-$0.5\times V_{DD}$ scheme to accommodate a wide range of input voltages while providing the necessary extra gate drive for the power FET at low inputs. The 32 phase charge pump runs at a frequency of 3GHz with a ripple of $\sim$ 3mV. The prototype was fabricated in TSMC's 65nm GP CMOS.**

I. Introduction

With the growing need of managing power consumption coupled with continuous technology scaling, the use of near-threshold supply circuits have become popular in VLSI subsystems, including processors, memory, and PLLs. Unfortunately, circuits which operate at near-threshold voltages, are highly sensitive to supply voltage variations, increasing the need of ripple-free power management. Low-dropout (LDO) regulators play an important role in this. Typically they provide ripple suppression and isolation from the switching regulators. In particular, for analog loads, the ripple suppression requirement becomes even more stringent.

Higher power efficiency demands lower drop out voltages, requiring LDOs to utilize PMOS pass transistors. These LDOs find it difficult to maintain the necessary gate-source headroom at lower input voltages below 0.5V. To circumvent the headroom problem, recently, digital LDOs (D-LDOs) have been developed for lower V_{DD}s [1]–[3]. D-LDOs utilize all-digital logic and/or time-to-digital conversion to replace the all-analog controller, and require no additional headroom by fully switching the pass transistor on/off. The fundamental problem with digital LDOs is that they have an inherent ripple even for a constant load due to finite resolution of switch sizes. The pass transistor characteristics roughly follow $I_L \propto \frac{W}{L} \times \Delta V^2$, where I_L, $\frac{W}{L}$ and ΔV are load current, aspect ratio and overdrive voltage receptively. In a conventional analog LDO, we use ΔV and in digital LDOs we use $\frac{W}{L}$ as the lever for load regulation. Being a square term, the ΔV is more powerful lever. So, to inherit the ΔV control lever and the simple design characteristics of analog LDOs, we propose an analog solution in the form of a smart adaptive offset LDO (SO-LDO) for handling the gate-source headroom of the PMOS pass transistor at lower supply voltages.

Fig. 1-left shows a typical LDO schematic (ignoring the voltage source offset V_{OS} for now). It contains a PMOS pass device and the error amplifier (EA), which forms the negative feedback loop. The EA can support an output voltage, $V_E \geq \Delta V_1$ (overdrive voltage of EA's output stage), before its gain rolls off. In a conventional analog LDO without any offset (V_{OS}), the EA voltage, V_E, for proper operation is given by $V_E = V_{DD} - V_{TP} - \Delta V_2$, where ΔV_2 is the pass transistor overdrive voltage and V_{TP} is the PMOS threshold voltage respectively. Thus for typical $V_{TP} \approx 0.3$V, VDD less than 0.7V cannot be supported (assuming $\Delta V_1 = \Delta V_2 \approx 0.2$). Let us consider what happens when we introduce an offset in the LDO. As a first step, let us consider a fixed negative offset between EA and pass transistor (as shown by voltage source V_{OS}). So for a fixed offset, we get, $V_E = V_{DD} - V_{TP} - \Delta V_2 + V_{OS}$ and for V_{OS}=0.4V, the lower limit for VDD becomes 0.45V. But the problem with this scheme is the breakdown voltage, V_{BD}, of the pass transistor, $V_{DD} \leq V_{BD} + \Delta V_1 - V_{os}$. We observe that, the lower limit of VDD does reduce but unfortunately, so does the upper limit due to the breakdown voltage concern. In our design, we resolve the upper limit problem by introducing a variable smart offset, V_{OS}=A-$A\times$VDD (where A is a design variable), such that at lower VDDs we maintain a finite offset but at larger voltages (near 1V in 65nm), the offset approaches zero. Fig. 1-right shows the VDDs that can be supported for the three cases- LDO without offset, LDO with a fixed V_{OS} (similar to D-LDOs) and LDOs with a smart offset (this work). We observe an additional 400mV input voltage dynamic range than conventional LDO and 300mV additional range in comparison to a fixed V_{OS}.

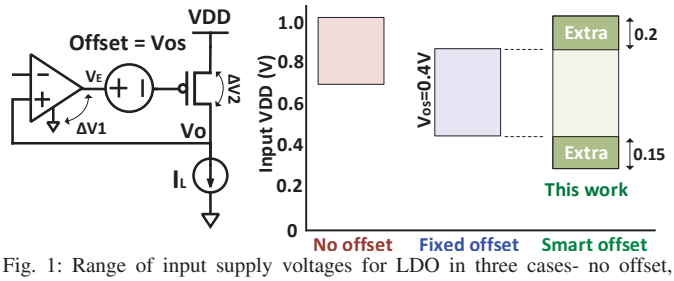

Fig. 1: Range of input supply voltages for LDO in three cases- no offset, fixed offset and smart offset (this work)

II. Design issues with low voltage LDOs

In this section we discuss the comparative present day design issues for low voltage LDO designs.

Analog LDOs: Fig. 2(a) shows the basic block diagram for a capacitor-less LDO. The loop gain of this system depends on the gain of pass transistor and the EA. Even in large output swing error amplifiers the minimum V_E is limited by the overdrive voltage of a NMOS transistor, ΔV_1 (typically $\Delta V_1 \sim$0.2V). As V_E decreases and becomes less than or equal

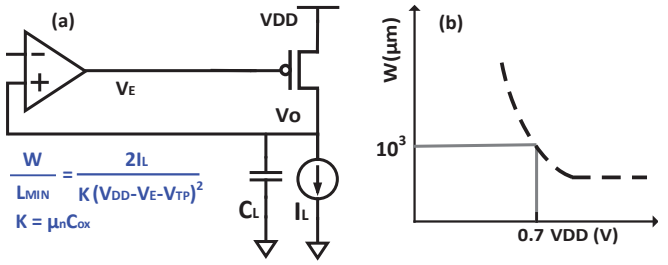

Fig. 2: (LHS) Basic capacitor-less analog LDO, (RHS) Minimum pass transistor size needed as a function of LDO input supply voltage (V_{DD})

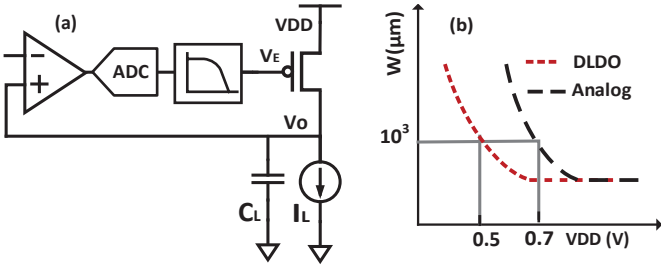

Fig. 3: (LHS) Digital LDO including ADC, comparator and switch array (or DAC). (RHS) Minimum pass transistor size vs input supply voltage for analog LDO and digital LDO. (I_L=100mA)

to ΔV_1, the EA output stage enters into the triode region thus decreasing the overall EA gain. Therefore, adequate regulation is maintained only as long as V_E is greater than equal to ΔV_1.

The maximum output voltage, $V_{O,max}$, is related to the input V_{DD} as, $V_{O,max}$=V_{DD}-ΔV_2. Here ΔV_2 denotes the pass transistor overdrive voltage and increases with increased loads for a fixed FET size. To first order the power efficiency is given by η=1-$\Delta V_2/V_{DD}$. Thus it is natural to design the width of the FET corresponding to a minimum possible dropout voltage for which we maintain the pass FET in saturation and stabilize the loop gain. We choose, ΔV_1≈0.2V, which is a good compromise between the gm/I current efficiency and FET size. Fig. 2(b) shows the LDO pass transistor device width as a function of the input V_{DD}. We note that the device size has to increase to compensate for the lower overdrive voltage that is available at low V_{DD}s. The knee in this figure is at $V_{DD,min} \approx \Delta V_1 + |V_{TP}| + \Delta V_2$ which is around 0.7V for $|V_{TP}| = 0.3V$. After this point, for a fixed current, the transistor width increases exponentially as ΔV_1 throttles the overdrive for the pass FET. The pass transistor carries the entire load current and is normally quite large in size setting both the DC and transient response due to the large parasitics associated with this device.

Digital LDOs: Normally, trying to accommodate V_{DD}s below 0.7V using an analog LDO results in a pass transistor that is unyieldingly large. This was the primary impetus for the design of digital LDOs. Fig. 3 shows the block diagram for a digital LDO which includes a switch array, a comparator, and a digital controller. As the gate drive can be as low as zero, to first order approximation, $V_{DD,min}$=0+V_{TP}+ΔV_2≈0.5V. The analog controlled power transistor is replaced with a switch array and the number of switches that are turned-on is digitally controlled. The output voltage (V_O) is monitored by the comparator instead of the operational amplifier. Thus, the digital LDO (D-LDO) eliminates all analog circuits and can operate at input supply voltages as low as 0.5V.

Comparison between A-LDO and D-LDO Let us compare the pass FET dimensions for an A-LDO (analog-LDO) and a D-LDO operating at 0.7V with a load current of I_L=10mA. For the A-LDO the pass transistor $width$=1000μm is as shown in Fig.(3) (black). We observe that, while keeping the load fixed, as we move to lower input voltages, the width required to support the load increases rapidly. As V_{DD}s approaches ΔV_1+V_{TP} (5̃00mV), the transistor dimensions becomes unrealizable. This is the reason why analog LDOs are not possible for lower input V_{DD}s. However, in the case of D-LDOs, the minimum gate voltage of the pass FET can be zero so for an input V_{DD} of 0.5V at 10mA the FET size is 1000μm and the $width$-V_{DD} curve shifts to the left as shown in red in Fig. 3.

III. Proposed Smart Offset LDO:

From the previous sections, the primary bottleneck for analog LDOs is the finite minimum V_E. We propose to solve this problem via a smart negative voltage offset inserted between the error amplifier and the pass transistor as shown in Fig. 4. The EA shares the input V_{DD} with the LDO. This smart offset allows us to operate at lower voltages and also reduces the pass transistor size as discussed next. The implementation details and loop stability analysis follow after that.

Lowering of the minimum input voltage: The smart adaptive offset is designed to follow a value of A-$A\times V_{DD}$. From Fig. 4, we know V_{OS}=V_E+V_{TP}+ΔV_2-VDD. Having V_E = V_{IN}/2 (for symmetric EA output), we get V_{OS}≈0.5-0.5×VDD. So A, the design parameter, is chosen to be 0.5. As the input voltage drops the smart offset increases so that we maintain a constant ΔV_2 across the pass transistor for different input voltages that range from 0.3V to 1.0V. By providing this offset, we enable the gate of the pass transistor to go to a negative voltage at lower LDO supply voltages (V_{DD}) thus avoiding the exponential bloating of the transistor size. The proposed smart offset LDO (SO-LDO) can sustain a load of 10mA and FET $width$=1000μm at a 0.3V input supply voltage (point A in Fig. 4). This clear reduction in minimum input voltage is due to the extra offset introduced.

Reduction of the pass transistor size: For the same current and a 0.5V V_{DD} we see in Fig. 4 that the FET size reduces from 1000μm to 100μm (a 10X reduction in comparison to D-LDOs) along the vertical grey line at point

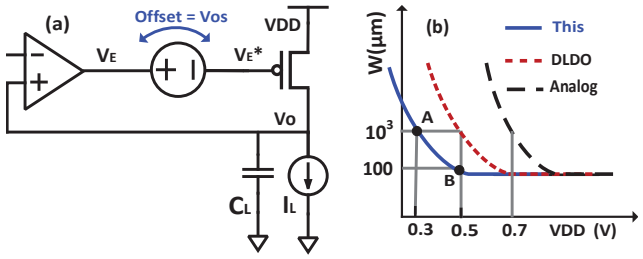

Fig. 4: Variation of the pass transistor width with the input supply voltage of the LDO. Black- analog LDO, red- digital LDO and blue- our proposed smart offset based LDO, all at IL=100mA.

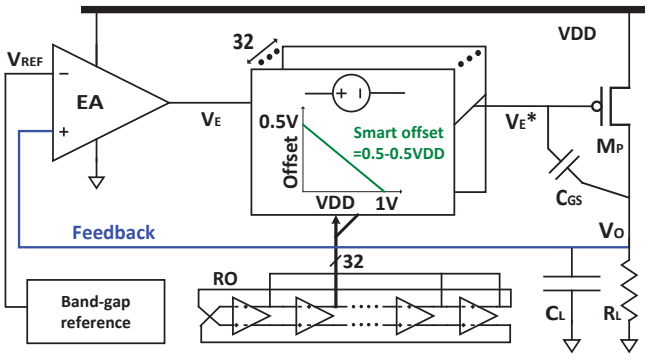

Fig. 5: Overall architectural detail of the proposed negative offset LDO

B. As shown in the Fig. 4, the V_E generated by the error amplifier is converted to V_E^*=V_E-V_{OS} and thus it improves the current driving capability.Taking the case where V_{DD}=0.3V, V_E=VDD/2 and $|V_{TP}|$=0.3V we get V_E^*=V_{DD}/2-V_{OS}=- 0.2V. Thus we see a leftward shift of the V_{DD}-vs-W curve (by 0.2V). The new design improves the drive capability ∼10X.

An adaptive offset helps in lowering the input V_{DD} as compared to a fixed offset. We know $V_E = V_{DD} - \Delta V_2 - V_{TP} + V_{OS}$, so the fixed offset, V_{OS} is bounded by Eqn.(1)

$$\Delta V_1 + |V_{TP}| - V_{DD} \leq V_{OS} \leq |V_{TP}| \quad (1)$$

From Eqn.(1), we see that for a fixed offset, the minimum V_{DD} is $\Delta V_1 + \Delta V_2 + 0.1V$ (design margin) $\approx 0.5V$, while our proposed design allows for V_{DD}s as low as 0.3V.

Architectural details: The smart adaptive offset, V_{OS}= 0.5V-0.5×V_{DD} is realized using a fast switched capacitor charge pump network. Fig. 5 shows the full circuit details. The EA output voltage V_E, feeds into the negative offset based charge pump which converts it to $V_E{}^*$. This $V_E{}^*$ serves as the gate voltage for the pass FET implemented by a LVT device. The switching frequency of the pump is designed to be at least a decade higher than the loop frequency and uses 32 interleaving phases thus maintaining a low output ripple. Non overlapping phases Φ1 and Φ2 are generated by a 32 stage ring oscillator coupled to a non overlap clock generator. The charge pump consists of four capacitors operating during the two non overlapping phases. During phase Φ1 the bucket capacitor A gets charged to V_E, capacitor B gets charged to V_{DD}/2 and capacitors C and D get charged to ≈ 0.5V (created on-chip). In phase Φ2, all the capacitors are connected in series with the capacitors C and D having opposite polarity as shown in Fig. 5. Deep-nwell NMOSs serve as switches in order to handle negative voltages. The resultant voltage $V_E{}^*$ = V_E + 0.5×V_{DD}-0.5. As shown in Fig. 5-right, the 0.5V is created by V_{TN} (≈ 500mV nominal) of a 2.5V I/O NMOS device. Six-σ mismatch is around 15mV while with 100C temperature change, the variation is 80mV. The EA is a self biased folded cascode OTA (which operates in sub-threshold for V_{DD} below 0.7V and in strong inversion for V_{DD} above 0.7V).

Loop stability analysis and ripple: The loop stability can be analyzed by considering the small-signal closed model shown in Fig. 7. The charge pump is represented as an average output resistor, R_{CP}, the error amplifier is represented as a Gm

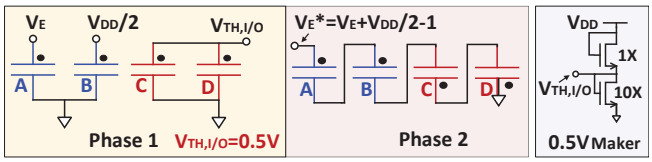

Fig. 6: Circuit details for the negative charge pump offset generator

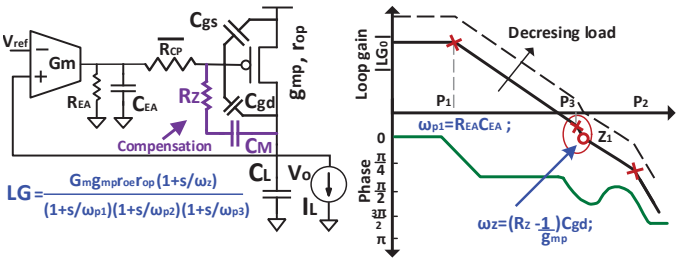

Fig. 7: Small-signal system model and frequency response

cell with a single pole roll off. This system has two poles and a left hand zero, caused by the charge pump resistor and C_{GD}, which helps with self compensation. The pole at the output of error amplifier is dominant while the pole at the LDO output is non-dominant. Thus for the frequency range that is about a decade lower than the switching frequency, the charge pump equivalent resistor helps realize a lag network. In isolation for the open loop, the gate-source capacitance acts as the filter capacitor for the charge pump thereby further reducing the ripple of the charge pump. The closed loop output impedance suppresses the charge pump ripple at the output.

IV. Measurement Results

Fig. 8 shows the measured closed loop impedance. We observe that the 3GHz ripple at a load of 100mA is suppressed significantly. Fig. 9(a) shows the chip microphotograph. The total active area is 0.15×0.4mm^2. Fig. 9(b-c) shows that the undershoot and overshoot recovery for a 10mA-100mA transient is 34.5nS and 43.62nS @0.5V output respectively. Fig. 10 shows the output ripple and charge pump frequency vs input voltage. For V_{DD}s below 0.5V, the switches are not sufficiently turned on, requiring a lower charge pump frequency, which in turn increases the output ripple voltage.

Fig. 11 shows the measured $V_{OUT} - V_{DD}$ characteristics at I_L of 10mA at different output voltages. At V_{IN} equal to 0.4V and V_{OUT} of 0.35V, the measured line regulation is 3.1mV/V. The LDO achieves a successful load regulation of 0.65mV/mA while V_{IN} varies from 0.3V to 1.0V. The measured quiescent current does not depend on I_L, and is 11uA (minimum) at V_{DD}=0.3V, though the quiescent current increases with

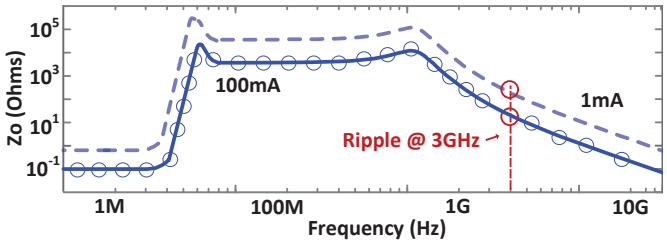

Fig. 8: Normalized closed loop output impedance for the proposed LDO at 100mA and at 10mA at V_{DD}=0.5V

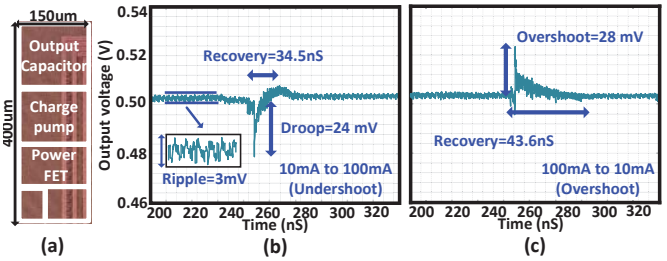

Fig. 9: Chip micrograph and transient at V_O=0.5V for SO-LDO

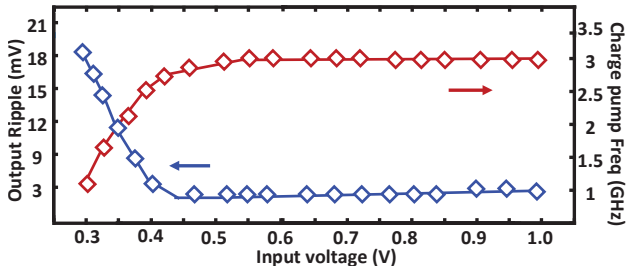

Fig. 10: Output ripple and charge-pump frequency for different input V_{DD}

I_{LOAD} in the other designs compared in TABLE I. This LDO achieves a peak current efficiency of 99.1% at 0.9-V input and 0.7-V output voltage. The input voltage, active area and the quiescent current are the lowest in comparison to any published LDOs as indicated in TABLE I. The EA and other control circuitry share the input voltage with the LDO unlike many other designs that use a higher V_{DD}. Due to the 32 phase interleaving the steady state ripple is always less than 3mV for V_{DD}s greater than 0.4V (and often as low as 1mV) which is an order of magnitude lower than other designs.

V. Conclusions

We present an analog solution for ultra low voltage LDOs using a smart offset. The offset adapts to the input voltage thus facilitating a constant minimum dropout. The charge pump generated smart offset enables an effective size reduction of the pass transistor at higher input voltages and makes the operation possible at the lowest input voltage of 0.3V. The SO-LDO has a 10X device size improvement as compared to D-LDOs. The SO-LDO can support a 0.3V-to-1.0V input with a quiescent current of 11uA. For each such input voltage, the SO-LDO can sustain a load variation of 10-100mA. It achieves a peak current efficiency of 99.1% at 100mA load and a 0.9V output voltage. The charge pump runs at a frequency of 3GHz with 32 phases so that the ripple is less than 3mV for V_{DD}s $\geq$ 0.4V which is an order of magnitude better than state of art D-LDOs. The SO-LDO is simpler to implement than D-LDOs, has lower ripple than D-LDOs and circumvents the minimum V_{DD} limit imposed by analog LDOs. The system was designed and measured in TSMC's 65nm GP.

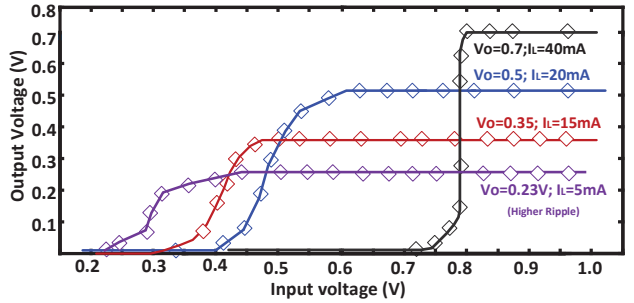

Fig. 11: O/P voltage regulation for Vo= 0.23V, 0.35V, 0.5V, 0.7V

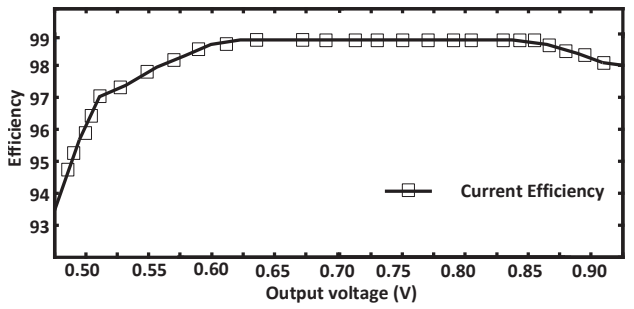

Fig. 12: LDO current efficiency at V_O=0.7V and V_{DD}=0.9V

TABLE I: Summary comparison with other related work

	[4]	[5]	[6]	[7]	This Work
Technology(nm)	65	65	45	40	65
Current Eff %	99.8	99.6	97	98.7	99.1
In Voltage (V)	1	1.2	1-1.2	1.34	0.3-1.0
Out Voltage (V)	0.6	0.7	0.8	0.9	0.23-0.9
Cout (nF)	0.3	0.86	1.67	-	0.1
Ripple (mV)	43	17	18.9	15	1-3[1]
Max I Step (mA)	120	55	13	15	90
Quiescent current (uA)	112	115	203	130	11
Undershoot time (nS)	40	50	30	70	34.5
Pwr Output (mW)	205	354	435	250	103
Area (mm2)	0.08	0.08	0.2	0.06	0.04

[1] For $V_{DD} \geq 0.4V$.

Acknowledgements

This work was supported by SRC/TxACE task ID 2712.008. The authors thank Rakesh Palani for useful discussions.

References

[1] Y. Okuma, K. Ishida, Y. Ryu, X. Zhang, P.-H. Chen, K. Watanabe, M. Takamiya, and T. Sakurai, "0.5-V input digital LDO with 98.7% current efficiency and 2.7-uA quiescent current in 65nm CMOS," in *IEEE Custom Integrated Circuits Conference 2010*, 2010, pp. 1–4.

[2] C. C. Chiu, P. H. Huang, M. Lin, K. H. Chen, Y. H. Lin, T. Y. Tsai, C. C. Huang, and C. C. Lee, "A 0.6V resistance-locked loop embedded digital low dropout regulator in 40nm CMOS with 77% power supply rejection improvement," in *2013 Symposium on VLSI Circuits*, 2013.

[3] C. L. Tai, A. Roth, and E. Soenen, "A digital low drop-out regulator with wide operating range in a 16nm finfet cmos process," in *2015 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2015, pp. 1–4.

[4] F. Yang and P. K. T. Mok, "A 0.6-1V input capacitor-less asynchronous digital LDO with fast transient response achieving 9.5b over 500mA loading range in 65-nm CMOS," in *European Solid-State Circuits Conference (ESSCIRC)*, 2015, pp. 180–183.

[5] ——, "Fast-transient asynchronous digital LDO with load regulation enhancement by soft multi-step switching and adaptive timing techniques in 65-nm CMOS," in *Custom Integrated Circuits Conference (CICC) 2015 IEEE*, 2015, pp. 1–4.

[6] C. S. Wu, K. C. Lin, Y. P. Kuo, P. H. Chen, Y. H. Chu, and W. Hwang, "An all-digital power management unit with 90% power efficiency and ns-order voltage transition time for DVS operation in low power sensing SoC applications," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 1370–1373.

[7] M. Onouchi, K. Otsuga, Y. Igarashi, T. Ikeya, S. Morita, K. Ishibashi, and K. Yanagisawa, "A 1.39-v input fast-transient-response digital ldo composed of low-voltage mos transistors in 40-nm cmos process," in *IEEE Asian Solid-State Circuits Conference 2011*, 2011, pp. 37–40.