Fully Tunable Software Defined DC-DC Converter with 3000X Output Current & 4X Output Voltage Ranges

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***Abstract*—This paper presents a fully integrated, software defined capacitive DC-DC converter. The converter implements K-F-C tuning (K = conversion ratio, F = frequency and C = capacitance) in real time so as to accommodate any output load. It has a 4X tunable output voltage, supports a 3269X output load current range while achieving a peak efficiency of 82.1%. This design introduces an accumulation floating junction MOS capacitor that is used for the 18.3 fF/μm^2 bucket-capacitors with less than 2μA/mm^2 leakage. This leakage is 40X lower than standard MOS capacitors. The converter transforms a 1.0V input to a 0.25-0.95V output for a 0.13mA-425mA load range while maintaining better than 70% efficiency. The power density for better than at 70% efficiency is 1.05W/mm^2 (@ V_{out}=430mV) while peak value is 2.15/mm^2. Load regulation is implemented using capacitive and frequency tuning in digital and analog domains respectively. The design was fabricated in TSMC 65nm.**

***Index Terms*—Software defined DC-DC converter, fully-integrated, high density capacitor, wide output range, KFC tuning**

I. Introduction

Power dissipation is a major concern for integration, particularly in battery-operated devices. Increased device leakage continues to be an issue with device scaling. On-board discrete component based regulators are highly efficient but are not well suited to support more than a few independent domains mandating integrated solutions. On chip power converters on the other hand suffer from area limitations, low passive quality and narrow operating range. Inductive converters provide high efficiency but aren't best suited for integrated implementations due to poor quality passives. Traditionally, capacitive converters have been better suited for limited output power ranges. However, switch capacitor DC-DC converters have become popular as integrated power conversion solutions because they consist of only switches and capacitors, which are both easier to design and are technology portable.

We propose a software defined DC-DC capacitive converter (SDCC) which tunes itself automatically (based on voltage sensing) via three methods - conversion ratio (K), switching frequency (F) and bucket (charge transfer) capacitance (C) level, providing a 4X output voltage range and a 3269X load current range. Fig. 1 show the basic idea of the proposed architecture. Fig. 1 (a) shows the voltage-efficiency profile of a single capacitive converter. We observe that at voltages near the no-load voltage the efficiency loss is dominated by bottom plate parasitics while at lower voltages the dominant loss mechanism is conduction losses. The peak efficiency is obtained close to the no-load voltage. Variable output voltages are best handles via multiple voltage conversion ratios as shown in Fig. 1 (b). Here we show five conversion ratios (K) implementing 'K' tuning. Similarly, Fig. 1 (c) shows the load

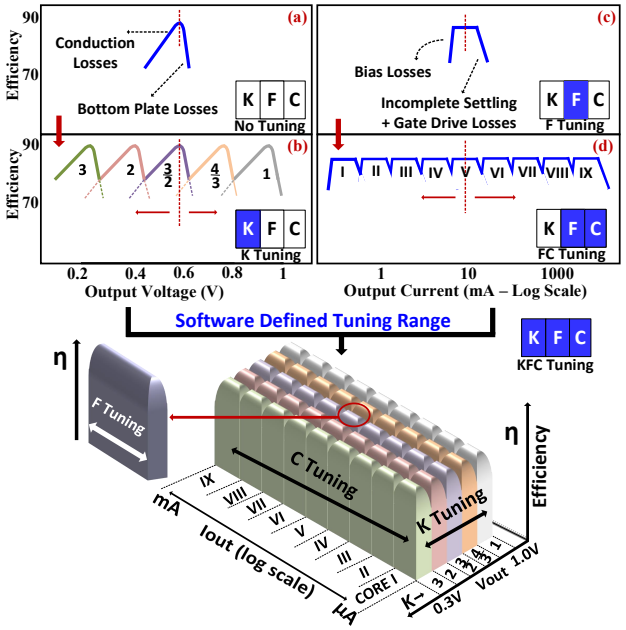

Fig. 1: Efficiency profile of a capacitive converter (a) Vs output voltage (b) Vs output voltage (multiple K values) (c) Vs output current (d) Vs output current (FC tuning). Bottom 3D-plot shows KFC tuning for the proposed SDCC.

current efficiency profile. We observe that by changing the switching frequency (F), we can regulate the output of the converter for a finite range. At higher currents the dominant loss mechanism is incomplete settling and at lighter loads constant losses dominate. If we need to increase the load current range appreciably, we need to increase the size of the bucket capacitors being switched, i.e., capacitive tuning (C-Tuning). As shown in Fig. 1 (d) nine identical capacitor cores are used to increase the load drive capability. Each of the nine cores can have their frequency tuned independently. By using all three forms of tuning, i.e., K, F and C tuning, allows the system to support the largest load range while maintaining high efficiency as shown by the 3-D surface plot in Fig. 1. This scheme forms the core of the proposed SDCC.

The proposed design is a fully tunable capacitive DC-DC converter that can support load voltages between 0.25V to 0.95V with a current range of 0.13mA-425mA (3,269X). It can support a DVS load with power range of 32uW to 203mW (6,344X) and can support a constant current load up to 100mA for all modes. The currents for K=4/3, K=3/2, K=2 and K=3 are higher (see Fig. 3). The design uses a low leakage, high density custom capacitors (AFJ MOS-cap) to implement the

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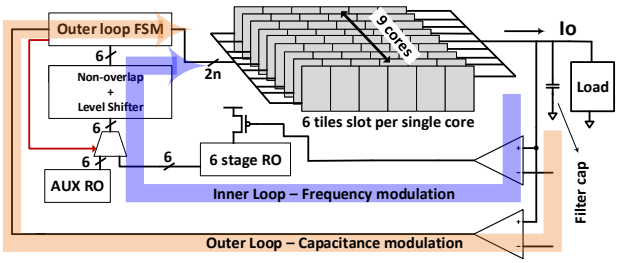

Fig. 2: Overall architecture with dual-loop load regulation

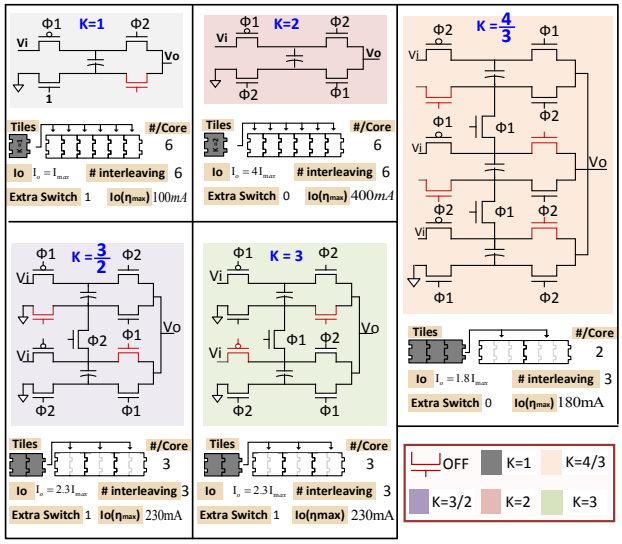

Fig. 3: Details of the IPO-OPG tile based core, and tile silicon reuse. $I_{max} = (V_{max} - V_o)C_{bucket} \cdot f$

capacitive cores with high power density.

II. Proposed Architecture

The proposed fully programmable converter can be digitally tuned to meet the electrical needs of any load (non-DVS and/or DVS) [1]. The proposed design, shown in Fig. 2, enables the converter to support five step down (K:1) voltage ratios (K=1, 1.33, 1.5 2, 3) for a wide range of load currents. This architecture mimics a "digital standard cell" approach and is made to be easily scalable. We propose the use of both capacitive modulation and frequency modulation for load regulation in order to achieve a 3269X current load range. Capacitive modulation (or C-tuning) is realized by an asynchronous digital FSM based (marked in orange in Fig. 2) system while frequency modulation (or F-tuning) is a VCO based analog-PID implementation (marked in purple). C-tuning implements coarse voltage regulation by turning off/on bucket capacitors. The design interpolates between two states of C-tuning using F-tuning as is discussed later in Fig. 6.

Fig. 3 (top row) shows the basic cell tile for the proposed programmable converter. The tile is flexible IPG-OPG (K=1) / IPO-OPG converter (K=2) depending on switch conditions [2]. Six such tiles make up a single conversion core. This single core can serve as any combination of six 1:1 (or six 2:1) or three 3:2 (or three 3:1) or two 4:3 converters. The overall capacitive bank is made up of nine such cores. Since, each

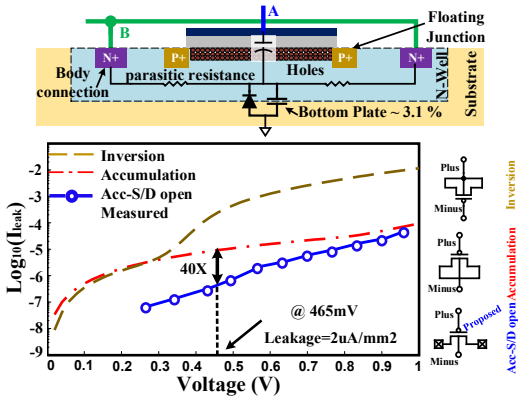

Fig. 4: AFJ MOS capacitor implementation details

tile uses 180pF, the total bucket capacitance size equals to 9.72nF (9x6x0.18nF). As shown in Fig. 3, different conversion ratios are generated by a combination of individual tiles. For example, in Fig. 3 modules of K=3/2 and K=3 can each be formed by stitching two K=2 modules in series. In this table the orange switch is always OFF, switch with a "1" on gate is always ON. Similarly, modules of K=4/3 can be formed by stitching three K=2 modules in series. Modules for K=1 and K=2 are the standard tile itself. We note that only K=1 and K=3/2 uses one additional switch in series in comparison to the minimal design. For this reason we have not scaled the switches for these two modes accepting the lowered fmax instead of lowered efficiency. As all five ratios utilize the same core tile we are able to use all the available capacitance for conversion at all times, i.e., no dark silicon at peak currents.

III. AFJ MOS-Cap based composite capacitor

We propose a custom designed low leakage, high density composite bucket capacitor for this converter. Accumulation Floating Junction (AFJ) MOS-cap is the primary constituent of the proposed composite capacitor. The AFJ MOS-cap is an accumulation mode PMOS transistor (Fig. 4-top) with the source and drain junctions left open (floating). This AFJ MOS-cap has the density of a conventional inversion mode MOSCAP but has 40X reduced leakage ($<$2uA/mm^2) due to reduced gate tunneling (Fig. 4), achieving 18.3fF/um^2 at 0.45-volt output voltage in 65nm GP. As the substrate-well diode remains in reverse bias (terminal B remains higher than substrate) the diode leakage is negligible (1/10X) as compared to the gate leakage. The source and drain terminals are floating (Fig. 4-top) allowing a 3X reduction in source/drain area and commensurate leakage reduction. The rest of the leakage reduction (13.3X) is due to reduced electric fields at the channel edges because of the floating source/drain. Fig. 4-bottom shows the leakage for an inversion mode, source/drain connected accumulation mode and measurement results for source/drain floating AFJ MOS-cap. The composite capacitor is a parallel combination of MIM, MOM (Met1-Met6) and AFJ MOS-cap contributing 20%, 20% and 60% of the total capacitance respectively. The composite capacitor has a 3.1% bottom plate and negligible top plate parasitic.

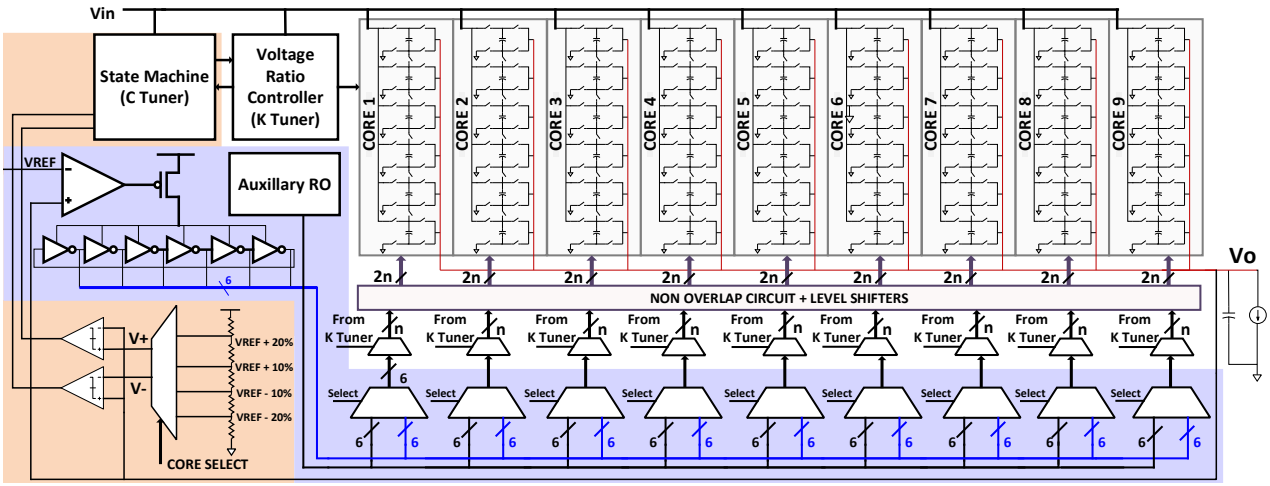

Fig. 5: Overall circuit diagram for the SDCC showing open loop core, time interleaving and silicon reuse

IV. Operation and Circuit Details

The overall circuit diagram is provided in Fig. 5. The converter utilizes dual feedback loops, i.e., one digital FSM based outer (in orange) and one analog based inner control loop (purple). These implement capacitive and frequency modulation respectively. The inner F-tuning loop is shown in purple and the outer C-tuning loop is shown in orange. Fig. 5 also shows the circuit details of the inner analog based control loop. We compare the output voltage with a reference level and the error is amplified to control the frequency of the 6-stage ring oscillator (RO). This RO based VCO also provides the time interleaved phases required for the different voltage ratios. The operation of the two loops are best illustrated via the orange staircase (C-tuning) and the purple interpolation ramp (F-tuning) in Fig. 6. Once the number of cores is selected by the FSM the 6 phase RO starts at an fmin=55MHz and can increase to an fmax=520MHz depending on the bias control voltage. We observe that when an additional core is switched-on, there is a current step and within a given core the internal loop ramps-up the current capability with a fixed slope of $4[(f_{max} - f_o)/V_{ripple}]C_o\Delta V$. As an example, when we are traversing (F-tuning) core #6, all the cores #1 - #5 are operating at fmax to maximize their current drives and RO only changes the frequency of core #6.

Fig. 7 shows the control flow for KFC-tuning. The algorithm starts with selecting the K value (manually implemented in this prototype). Once the K is set the control moves to the interplay between the inner and outer control loops (F-C tuning). V+ and V- are the upper and lower thresholds for outer control loop, which are programmable on outer loop (C-tuning) state via a string DAC. Note that for 1:1 and 2:1, we have 54 IPO-OPG modules, and then, 6 interleaving stages. For 3:2 and 3:1, 3 modules/phases while for 4:3, we have 2 modules/phases. The large interleaving allows for a minimal output filter capacitor size of 450pF.

Fig. 8 shows the simulated transient behavior for the outer loop. This digital FSM based outer loop provides capacitive modulation by switching on/off one core at a time. As described earlier, it locks all other working cores to fmax,

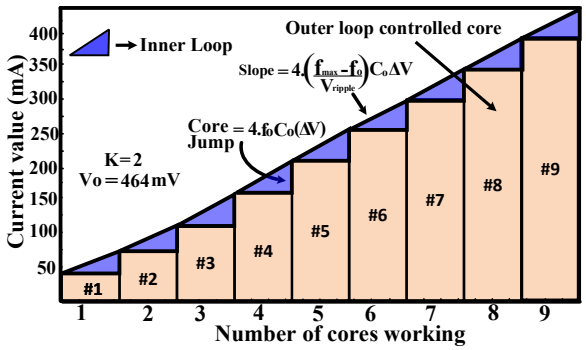

Fig. 6: The current profile using C-tuning (orange) and F-tuning (purple) for K=2, Vo=0.464V

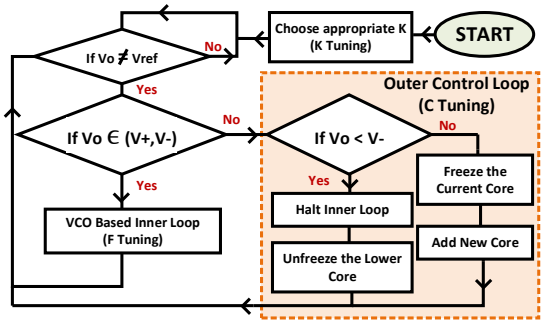

Fig. 7: Control flowchart for the proposed SDCC

generated by an auxiliary RO for maximum power density. The undershoot droop is 84mV and recovery time is 23.4nS which is possible due to the asymmetric state transitions (shown in Fig. 8-bottom, the blue arrows show the 10mA to 110mA trajectory ($1 \rightarrow 4 \rightarrow 7 \rightarrow 6 \rightarrow 5 \rightarrow 4 \rightarrow 3$ while the black arrows show the 150mA to 40mA trajectory ($4 \rightarrow 3 \rightarrow 2 \rightarrow 1$)). In Fig. 8 undershoot recovery starts by moving to state 4 then to 7. Finally, trickling down from state 7 to state 3 (one-by-one), completes the recovery. This under compensated behavior is similar to what is done in PLLs for the fastest transient response. The slight offset in the final

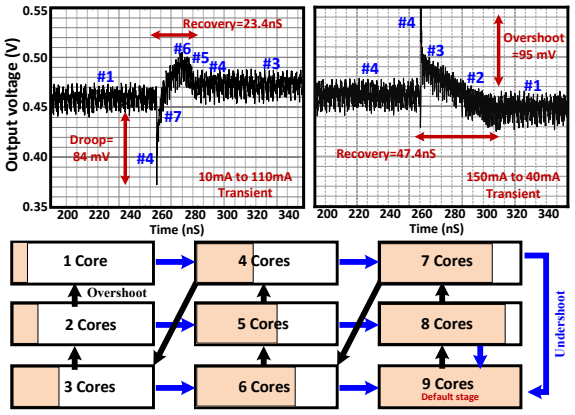

Fig. 8: Simulated capacitive control transient response

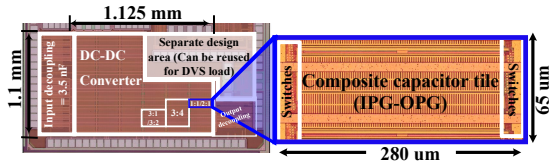

Fig. 9: Overall chip micrograph & standard cell layout details

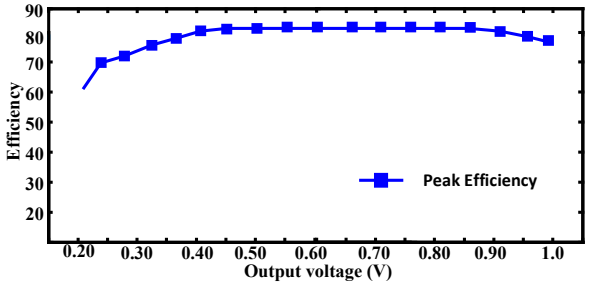

Fig. 10: Measured peak power efficiency vs output voltage

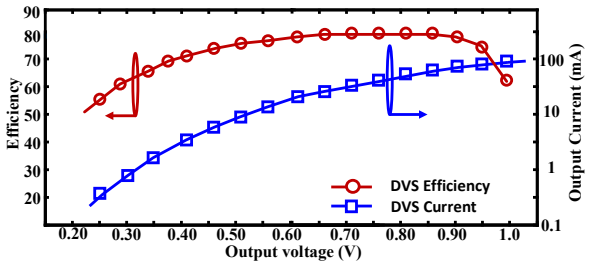

Fig. 11: Measured efficiency vs. output voltage and load current vs. output voltage for a DVS load

value is due to finite loop gain.

V. Measurement Results

Fig. 9 shows the micrograph of the chip and a zoom-in of the standard-cell IPG-OPG/IPO-OPG tile that is the basis for all converter topologies. For steady-state efficiency measurements, we stress the converter with on-chip MOS-based resistive banks. The converter achieves its peak efficiency of 82.1% for K=2 (Vo=0.43V). Fig. 10 shows the peak efficiency verses output voltage for different loads. For output voltages below $0.4V$, (i.e., lower currents) the peak efficiency drops due to control and biasing losses. For higher voltages the peak efficiency starts to drop slightly due to switching losses and partial charging [2]. During the voltage change from 0.25V to 0.95V the current can change from 0.13mA-425mA (3,269X). As an addition representative example, we test a DVS based load using a nine stage ring oscillator. Fig. 11 shows the DVS load efficiency and DVS current-voltage relationship for the test load. For the DVS load the power ranges from 32uW to 203mW (6,344X). The best recovery time for the system is 23.4nS for 10-110mA load variation at 460mV in K=2 mode facilitated by both the loops.

VI. Conclusions

We have implemented a fully programmable capacitive DC-DC converter which supports a wide range of output loads for every given output voltage between 0.25V to 0.95V. In order to achieve high power density we used a novel high density composite capacitor. This new PMOS-based capacitor has the lowest measured leakage (40X) of any structure available in standard CMOS. Further, simulations suggest that the AFJ MOS-cap inherits it low leakage properties for 45nm and smaller processes. The methodology can be applied to NMOS devices in twin-well processes as well, showing its versatility. A dual control loop achieves zero dark silicon for all five-voltage modes. Fully programmable time-interleaving was used to boost power density and reduce the ripple. The design uses a maximum of 6-phase time-interleaving and reduced output filter capacitor. The power density for better than 70% efficiency is 1.05 W/mm^2 while peak power density is 2.15 W/mm^2. Table I shows that this SDCC design has the largest power range (32uW-203mW, i.e., 6344X), the highest power density in a standard 65nm GP process without exotic high density capacitors as in [1], [3]. The design provides complete flexibility (K-F-C-tuning) while maintaining good efficiency. Only [1] has higher efficiency but uses 28nm SOI with deep trench capacitors.

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TABLE I: Summary and comparison with prior work

	[1]	[3]	[4]	This Work
Technology (nm)	28	32	130	65
Input Voltage (V)	1	2	1-1.2	1.0
Output Voltage (V)	0.45	0.88	0.6	0.25-0.95
Ripple (mV)	20	61	8.9	30
Passive Size	1nF	5nF	1nF	9.7nF
Capacitor Type	DT	DT	MOS	AFJ-MOS
Max Power Efficiency %	87	79.76	82	82
Max Power Density (W/mm^2)	0.35	0.86	0.67	2.15
Power Range (mW)	8-173	23-450	34-567	0.032-203