# Integrated DC-DC Converter Design

***Ramesh Harjani***
Department of Electrical & Computer Engineering
harjani@umn.edu

# Talk Outline

- **Introduction to DC-DC converters**
  - Motivation, uses
- **Types of DC-DC**
- **Linear converters**
  - Series/shunt
  - Classification, design
- **Inductive converters**
  - Passives + integration
  - Control, design methodology
  - Examples, SIMO
- **Capacitive converters**
  - Framework
  - Design methodology
  - Control, circuits
- **Special capacitive converters**
- **Design example - capacitive**


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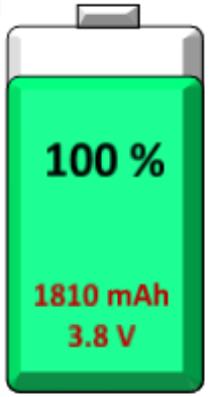
# MOTIVATION

# Power Is Precious

Wi-fi > 10 h (691 mW)

LTE > 10 h (691 mW)

3G > 14 h (490 mW)



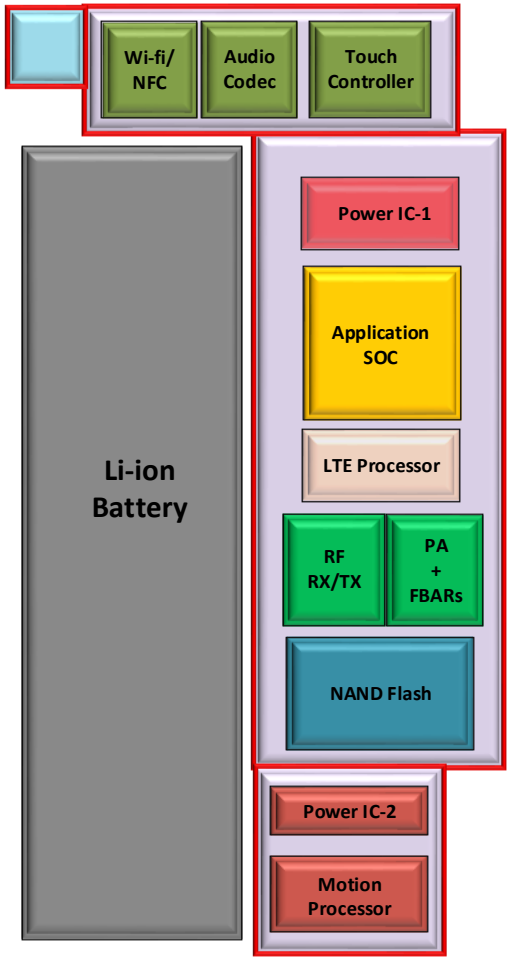

Gaming > 2 h (3.25 W)

Standby > 250 h (27 mW)

Video > 10 h (691 mW)

Audio > 40 h (175 mW)

1 battery → Multiple features




Smartphone teardown

Volume energy density = 400J/cm$^3$

Weight energy density = 900J/cm3

25KJ = 1day iphone = 28g = 62.5 cm$^3$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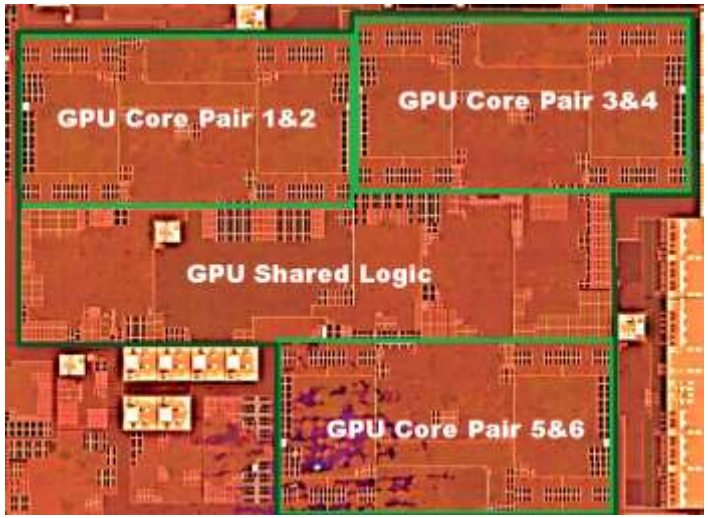
# Motivation: Mobile Devices

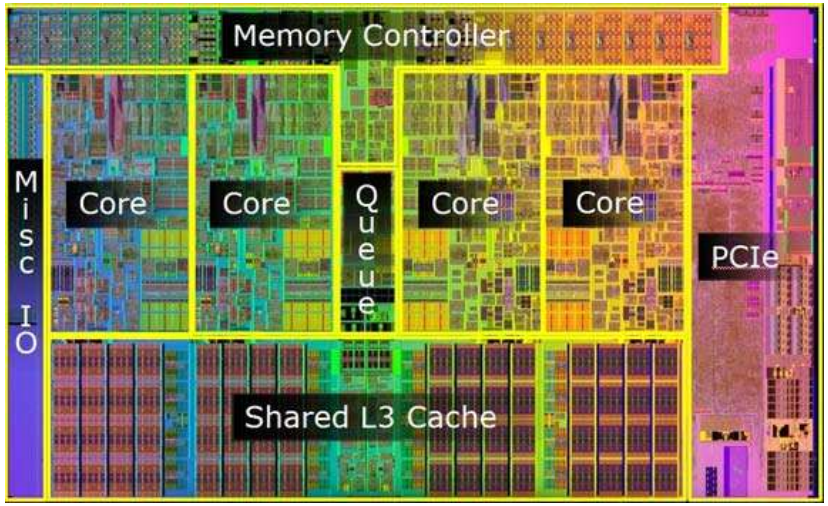
- Rapid advancement in VLSI technology
  - Multi-core processors in battery powered devices
  - Si technology moved from 350nm in 1995 → 22nm NOW
- Battery capacity does not follow Moore's law
  - Li-ion battery energy density only 2X since 90s !!!! *

## Apple A9 GPU core




http://www.anandtech.com/show/9686/the-apple-iphone-6s-and-iphone-6s-plus-review/5

## Intel core i7 mobile




http://hothardware.com/printarticle.aspx?articleid=1384

*(http://thisweekinbatteries.blogspot.com/2010/02/moores-law-for-batteries-maybe-not.html)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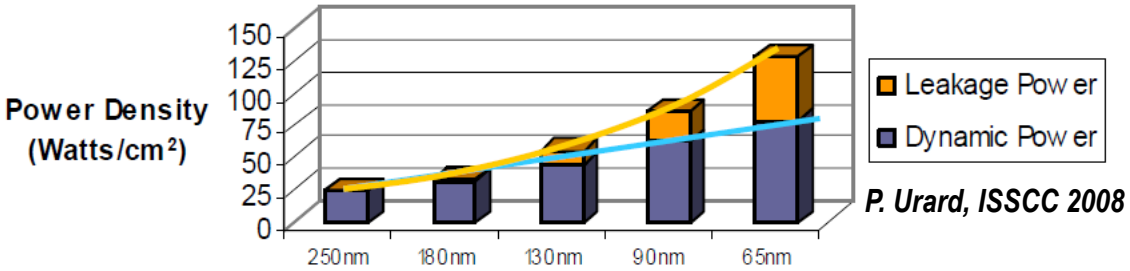
# Leakage Power & Multiple Domains

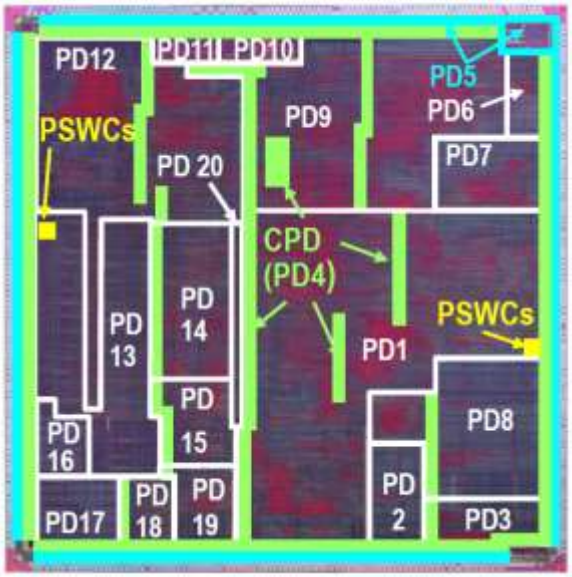
- Leakage power is an increasing contributor

ASICs [source: STMicroelectronics].




*P. Urard, ISSCC 2008*

- Increase in the number of power domains




One-chip 3G Cellular Phone processor with 20 power domains, 90nm 8M, dual VT CMOS, Y. Kanno, et al, ISSCC 2006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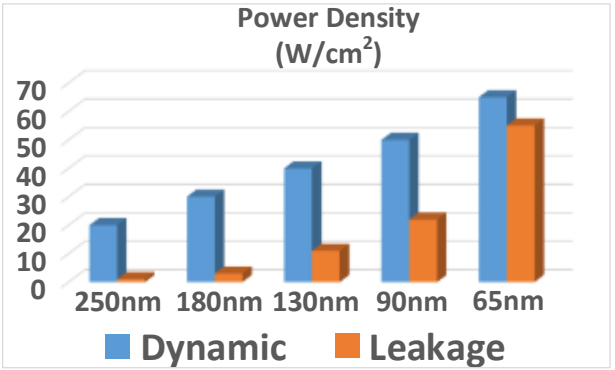
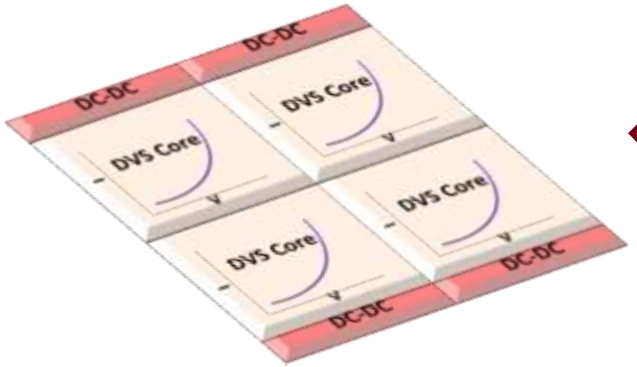
# Why Integration?




Higher Performance

Small Form Factor

More Features

Less Cost

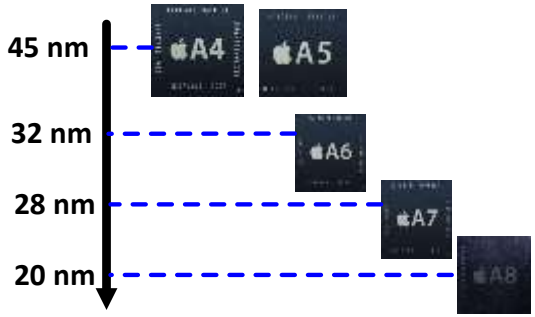
Scaling

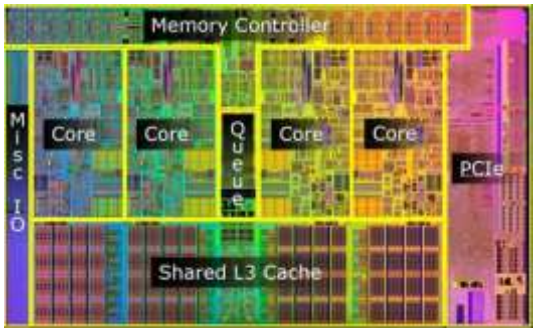
Leakage

Multiple Cores

DVFS per core

Integrated Solution





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# TYPES OF DC-DC CONVERTORS

# DC-DC Converters Are Everywhere

- Linear converters
  - Low noise → no switching parts
  - Efficiency depends on conversion ratio
  - Primarily for down conversion (buck converter)

- Capacitor converters
  - Buck, boost and voltage inversion possible
  - Most popular switching converter
  - Needs only capacitors & switches → easily integrated

- Inductive convertors
  - Buck, boost and voltage inversion possible
  - Theoretical high efficiency for any conversion ratio
  - Need large, high-Q inductors → not easily integrated

**Ideally**

$P_{in} > P_{out}$

$P_{in} > P_{out}$

$P_{in} = P_{out}$


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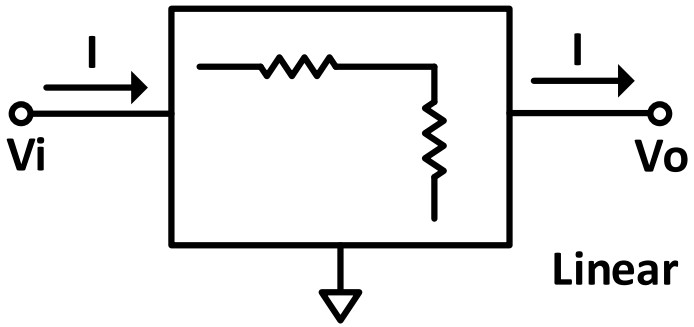
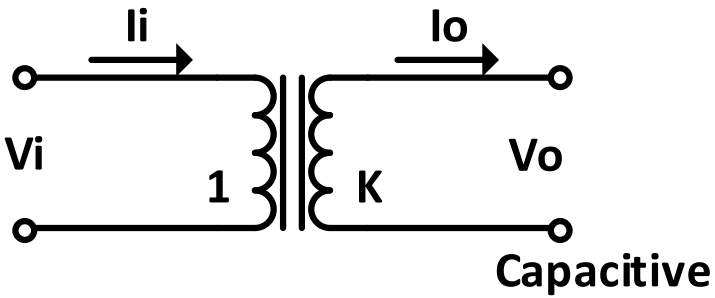
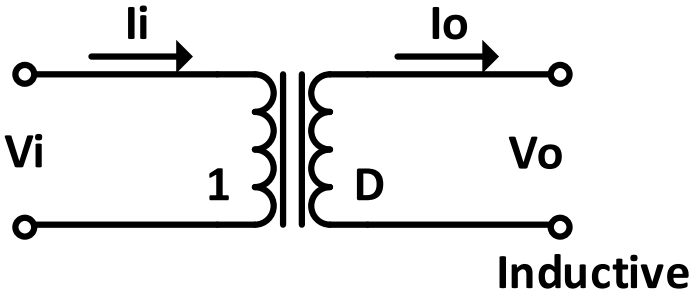
# DC-DC Converter Modelling (Ideal)




| Transformer Model | Efficiency Voltage Relationship |
|---|---|
| $1:1$ | $\eta = \frac{Vo}{Vi}\ ;\ Vo < Vi$ |
| $1:k$ | $\eta = \frac{Vo}{kVi}\ ;\ Vo < kVi$ |
| $1:D$ | $\eta = \frac{Vo}{DVi}\ ;\ Vo = DVi$ |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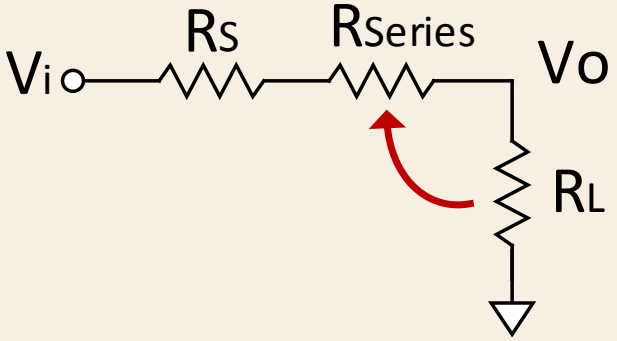
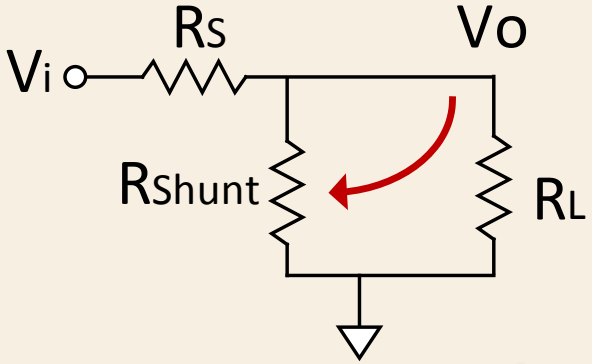
# LINEAR CONVERTERS

# Linear Regulators




$$\frac{V_o}{V_{in}} = \frac{R_L}{R_L + R_{Series} + R_s}$$

Series regulator




$$\frac{V_o}{V_{in}} = \frac{1}{1 + \left( \frac{R_s}{R_{shunt} \,||\, R_L} \right)}$$

Shunt regulator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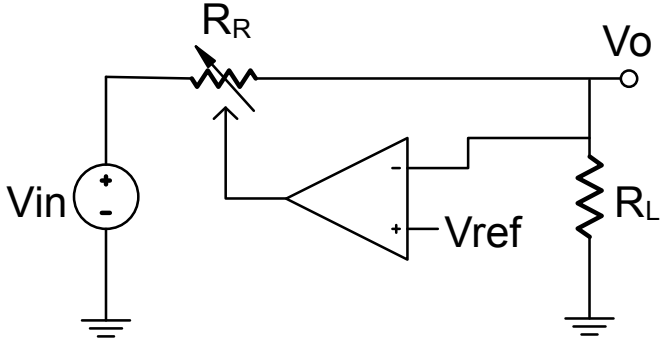
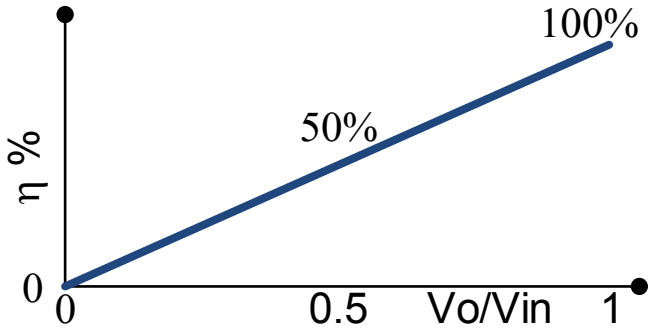
# Series Regulator

- The output voltage Vo is kept constant by varying $R_R$
- Efficiency = power in load /power from source
- If same current is flowing in $R_R$ and $R_L$ then $\eta = Vo / Vin$




**Linear Converter Block Diagram**




**Conversion Efficiency vs Vo/Vin**

$$\eta = \frac{Vo^2}{R_L}\frac{R_R + R_L}{Vin^2} = \left(\frac{Vo}{Vin}\right)^2 \frac{R_R + R_L}{R_L}$$

$$= \left(\frac{R_L}{R_R + R_L}\right)^2 \frac{R_R + R_L}{R_L} = \frac{Vo}{Vin}$$

$$\eta = \frac{I_L \cdot Vo}{I_L \cdot Vin} = \frac{Vo}{Vin}$$

**Voltage divider → efficiency is ratio of voltages**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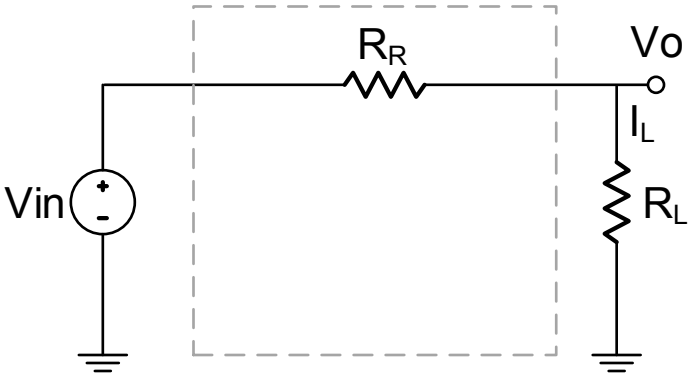
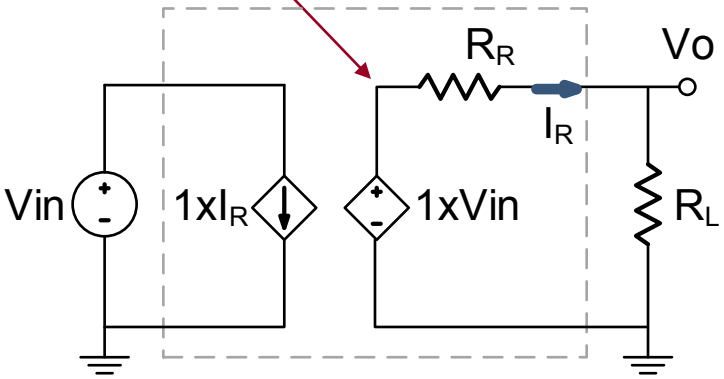
# Model For Linear Converter

- Linear regulator = linear converter = aka LDO
- Linear regulator model ⟷ transformer model
- Transformer has a turns ratio of 1
- Conversion efficiencies

$$\eta = \frac{Vo}{1 \times Vin} = \frac{Vo}{Vin}$$




Linear Converter Model




Linear Converter Transformer Model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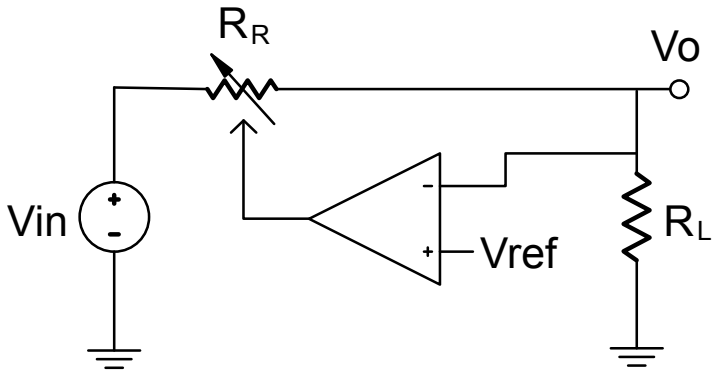
# Characteristics

- DC characteristics
  - Line regulation

$$\frac{\Delta V_o}{\Delta V_{in}} = \frac{1}{1+\beta A}$$

  - Load regulation

$$\frac{\Delta V_o}{\Delta I_o} = \frac{R_{o,open}}{1+\beta A}$$

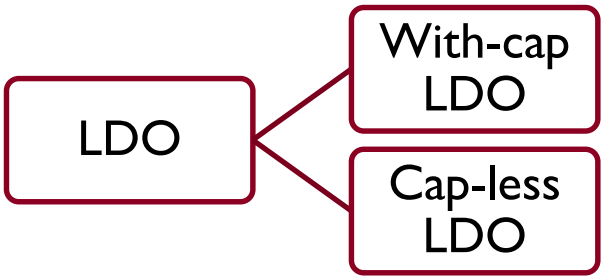



$$\beta = \frac{R_L}{R_L + R_R}$$

- AC characteristics
  - Input ripple rejection (PSR) → AC equivalent of line regulation
  - Output ripple rejection → AC equivalent of load regulation

# Low Drop Out Regulator

- Low Drop Out (LDO) regulator
  - (Vi-Vo) is desired as low as possible
  - Most popular/researched topology




- With Cap LDOs
  - Off-chip output capacitor, higher power levers, discrete
- Cap-Less LDOs
  - Integrated, fast/higher bandwidth, large load transient droop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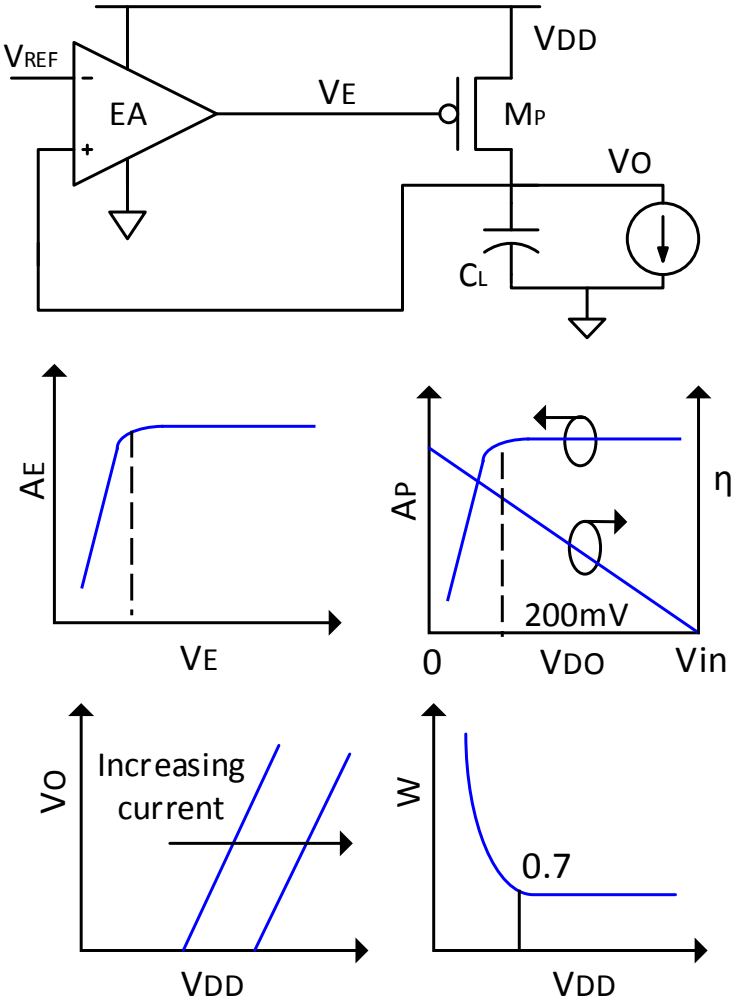
# With-Cap LDOs

- With Cap LDOs
  - Output capacitor, CL, is the dominant pole capacitor
  - Small bandwidth, less droop
  - Easy compensation
- Design constraints
  - $V_E$ cannot be lower than a $\Delta V$
  - Vo,max = VDD – $\Delta V$
  - AE, AP must be constant during the operation of regulation
  - Width of the pass transistor goes up rapidly for lower VDD





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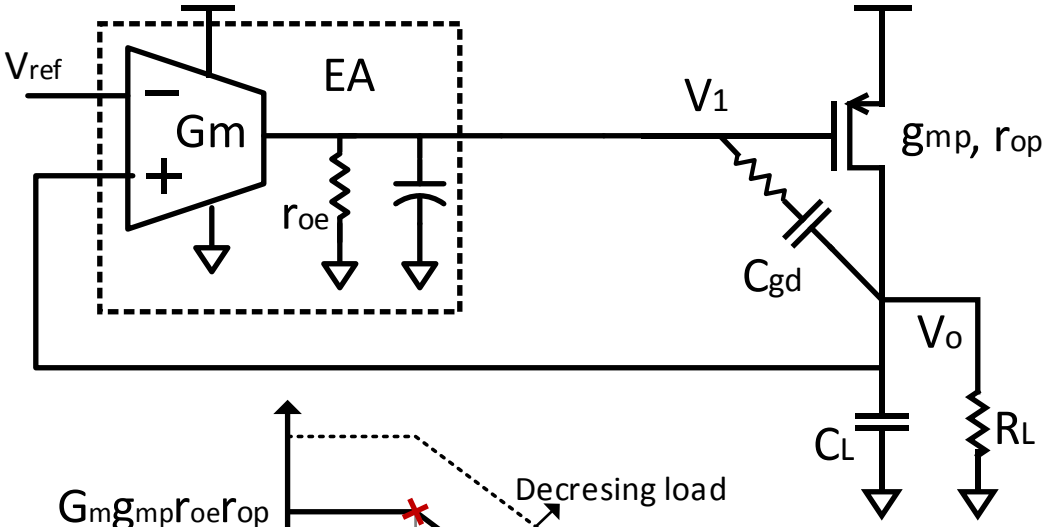
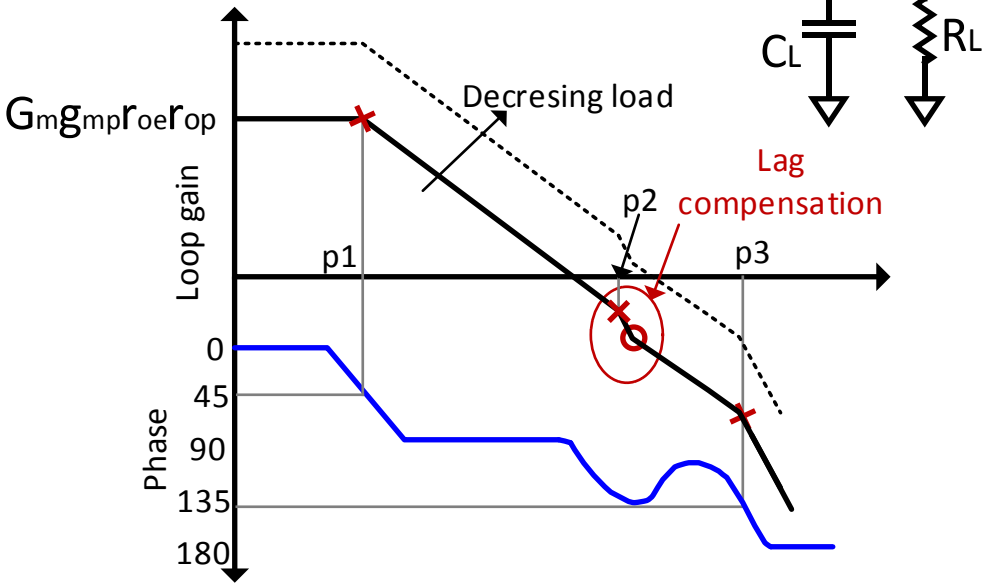
# Compensation

- Dominant pole
  - Output capacitor, CL, is dominant pole capacitor
  - Small bandwidth, Easy compensation
- Non dominant poles
  - EA internal poles
  - Gate of the pass transistor
- Impact of load
  - More instability at lighter load





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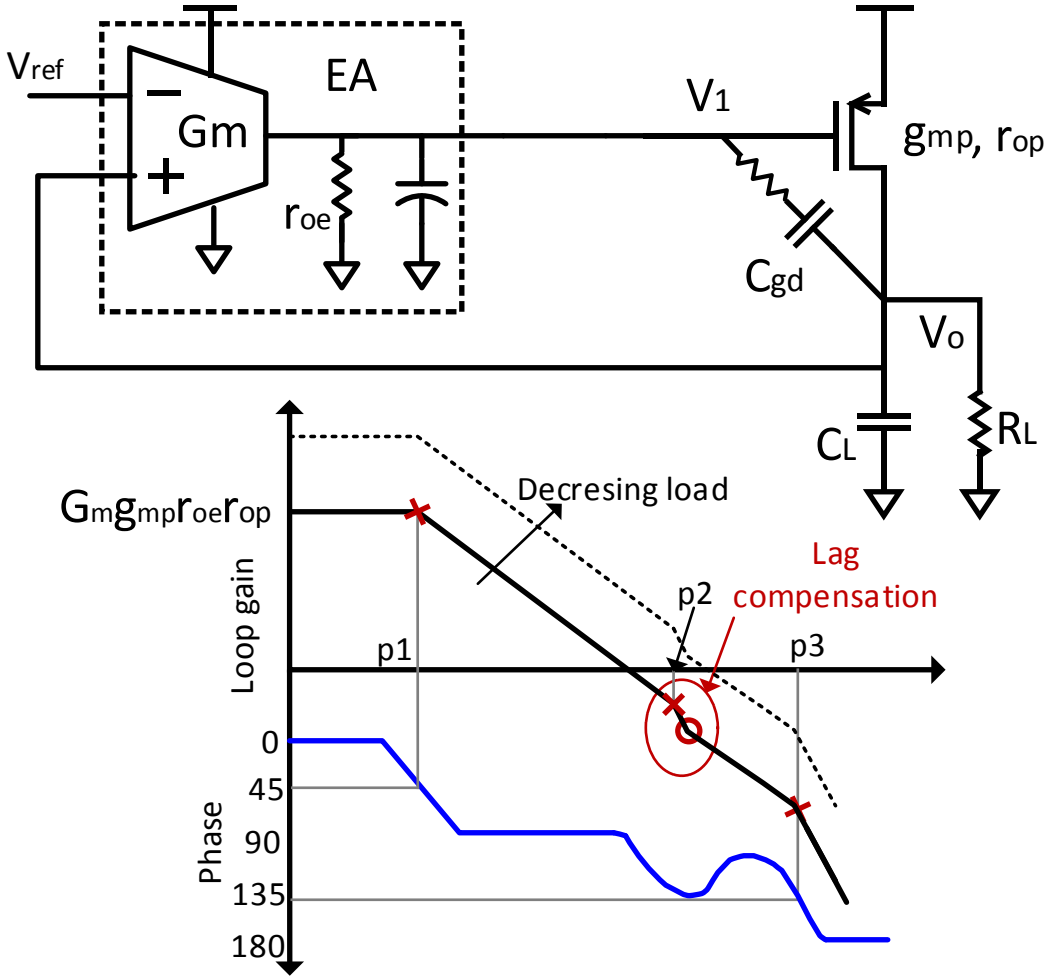
# CAP-Less LDOs

- Dominant pole
  - Dominant pole of the EA
  - Large bandwidth, difficult compensation
- Non dominant poles
  - Gate of pass transistor
  - EA internal poles
- Impact of load
  - More instability at lighter loads as gain increases





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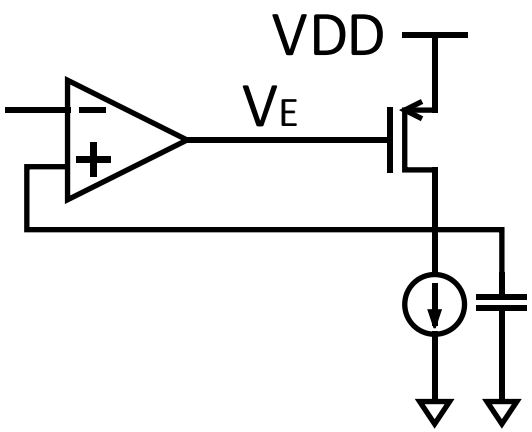
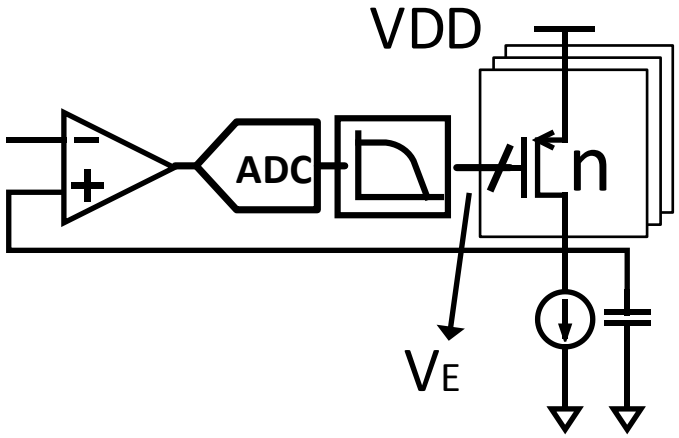
# Classification




- Analog amplitude
  - No steady state output ripple
  - Analog compensation
- Digital amplitude
  - Steady state ripple
  - Digital compensation

**Conventional LDOs**

**Digital LDOs**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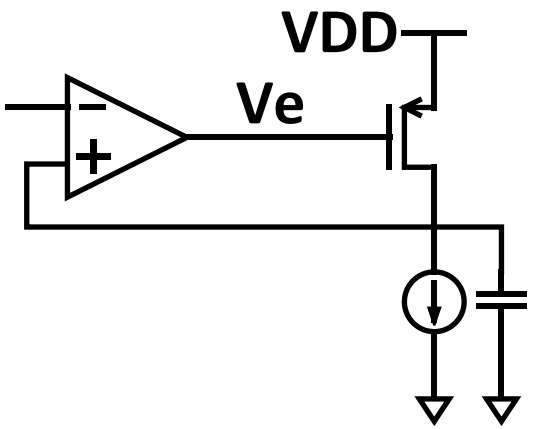
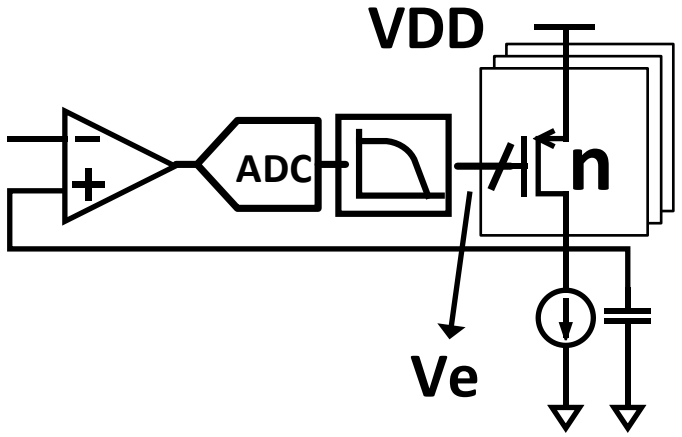
# Digital LDOs

- Motivation - analog vs digital
  - As VDD lowers, Ve is bottleneck
  - Make Ve zero
- DLDOs
  - Pass transistor either OFF/ON
  - Mimic LDO operation
  - Complex design
  - Easy compensation
  - Intrinsic ripple due to quantization





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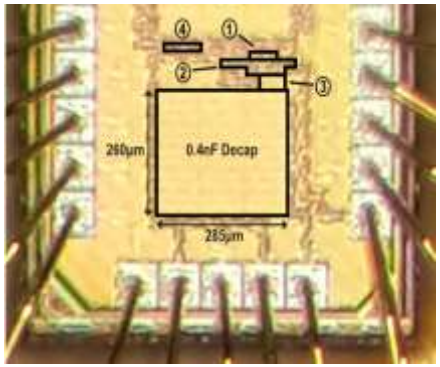
# A 100nA-to-2mA SAR DLDO With PD Compensation And Sub-LSB Duty Control




**Process: IBM 130nm CMOS**

**Loai G Salem, Patrick Mercier**

**ISSCC 2017**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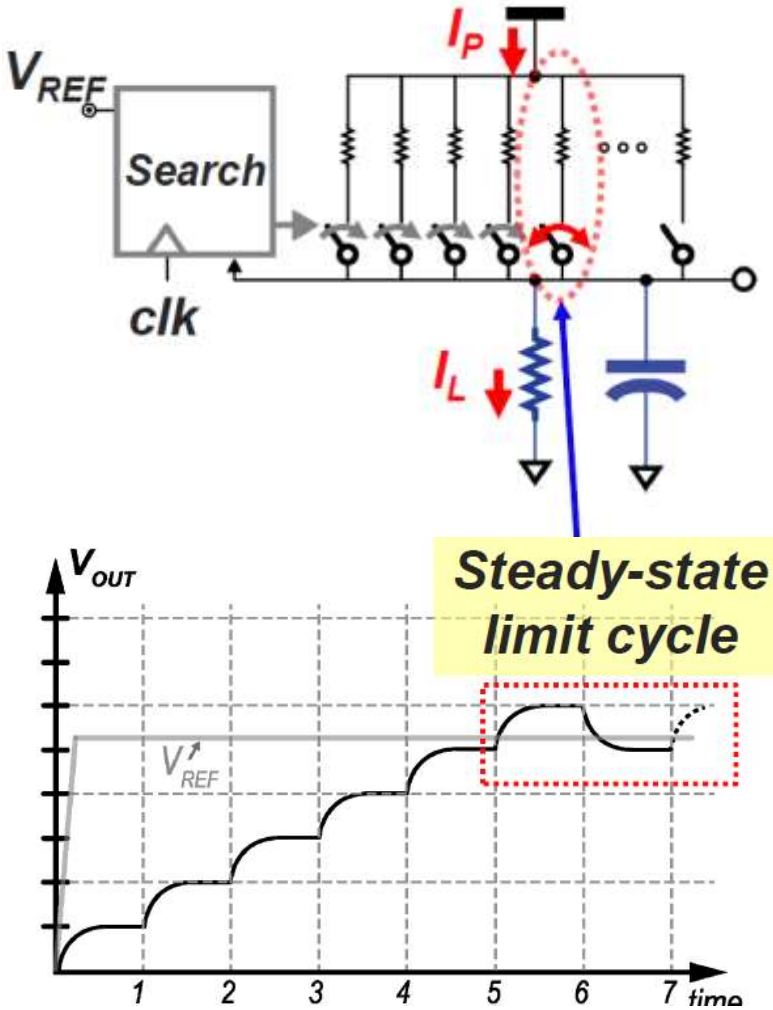
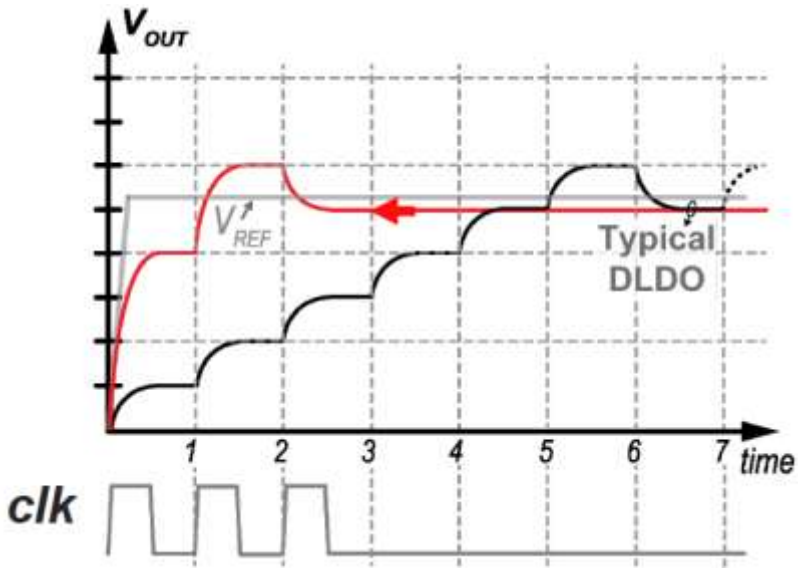
# Example - SAR DLDO





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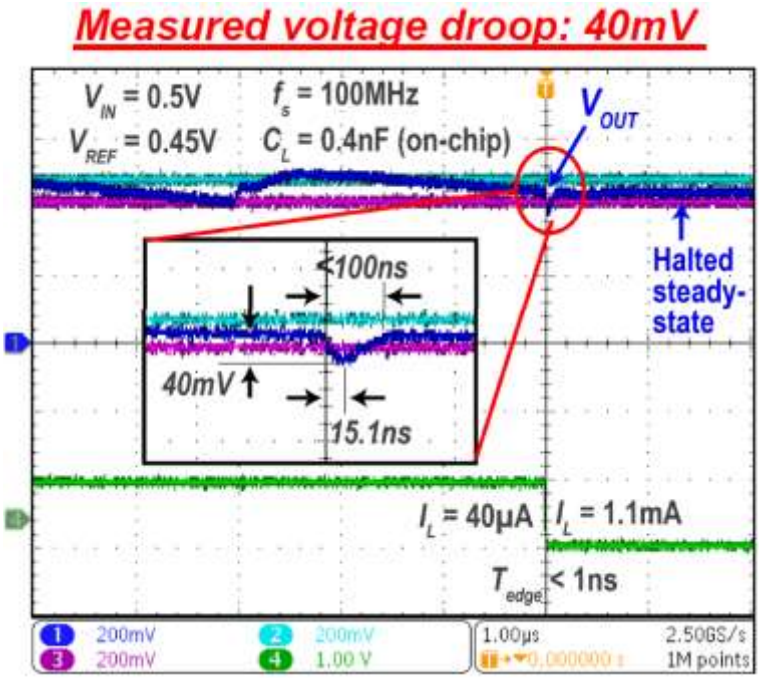
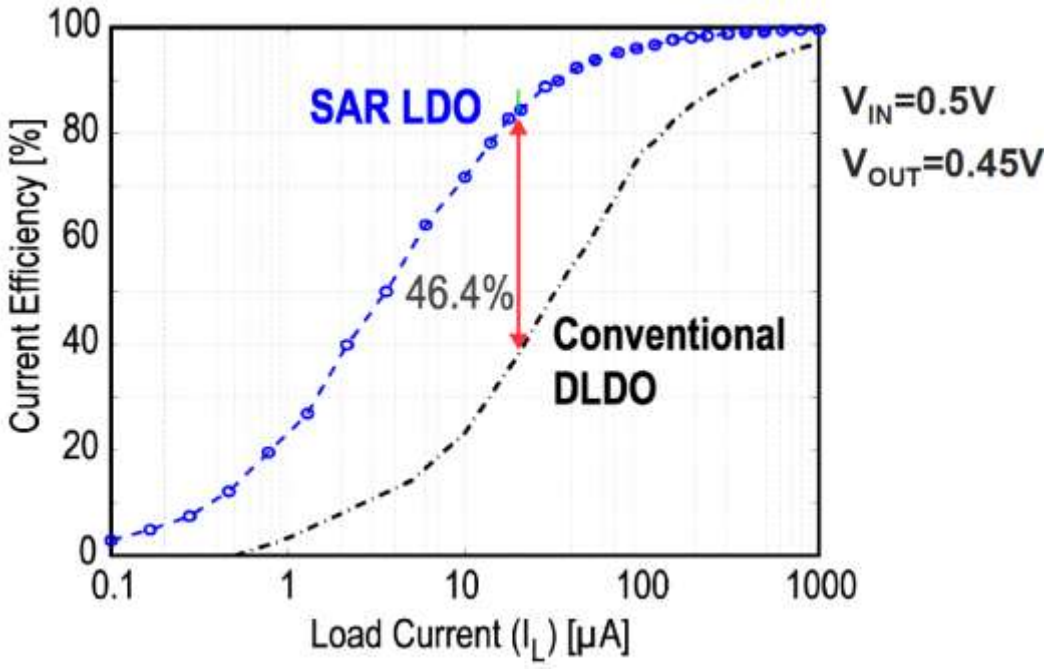
# Measurement Results




| | Proposed LDO | Prior LDO |
|---|---|---|
| Response time ($T_R$) | 15.1ns | 377.5ns |
| Settling time | <100ns | 1.37µs |
| FOM | 199.4ps ⟷ | 638ns |

$>2^{2N}/N$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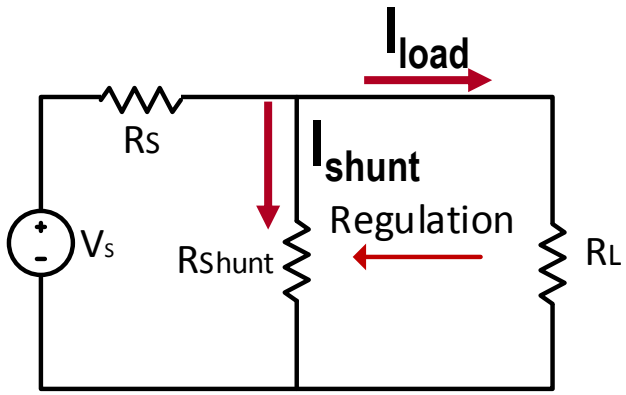
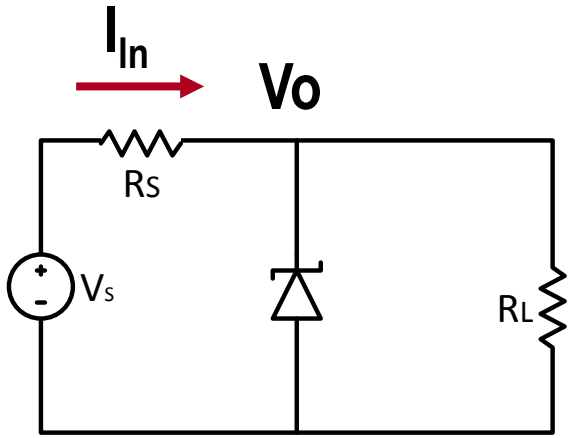
# Shunt Regulator

- Motivation
  - Lowest operating point (Minimum Vin-Vo)
  - If power supply is high (|Vin| is high)
  - Good for making
    - Negative reference
    - Floating reference
    - Voltage limiting reference




- Unequal input and output currents
- Shunt resistor regulates
- Less popular (bulky)




**Current divider → efficiency is ratio of currents**

$$\eta = \frac{I_{Load}}{I_{in}} = \frac{1}{1 + \frac{I_{Shunt}}{I_{Load}}}$$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# INDUCTIVE CONVERTER

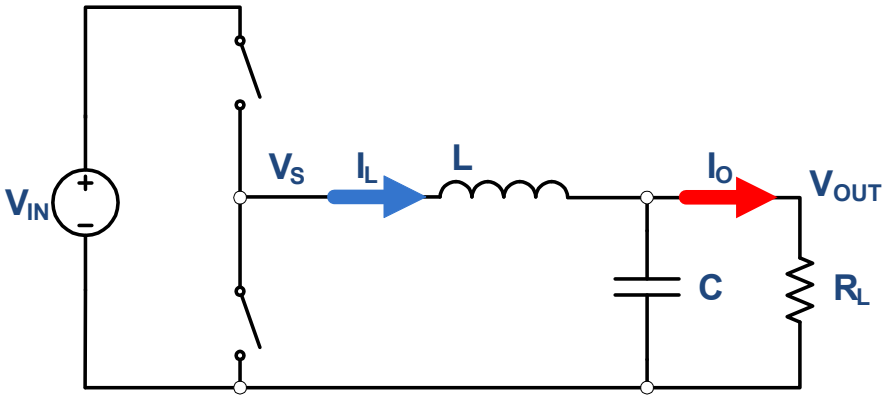
# Inductive Power Converter

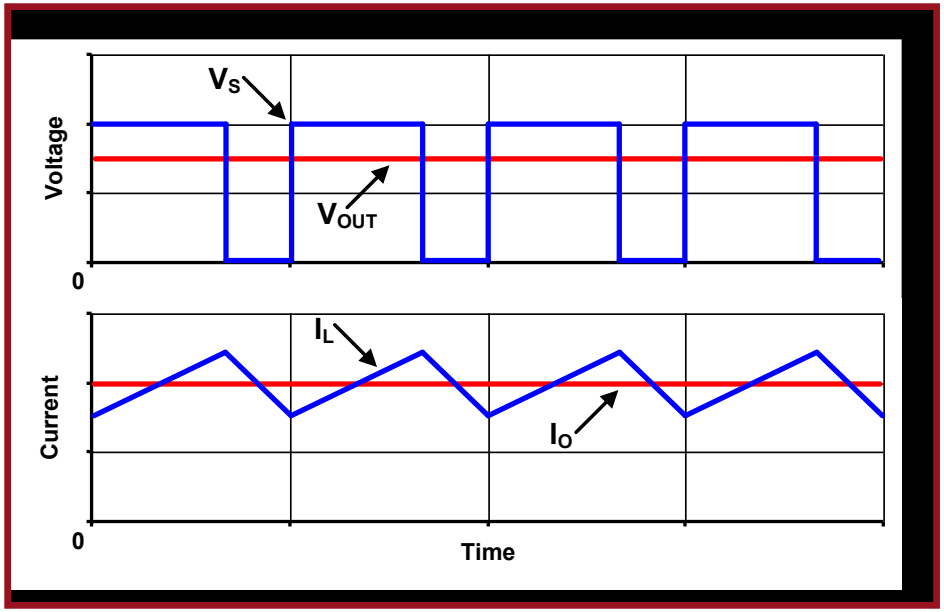
- Switch
  - Chops up the input voltage
  - Can be implemented using a Diode-FET, NMOS-PMOS, or NMOS-NMOS combinations

$$Vout = D \cdot Vin$$

- Filter
  - Ripple current is proportional to switching frequency and inductance
  - Ripple voltage is proportional to ripple current and output capacitance

$$Iripple = \frac{1}{L} Vin \cdot D(1-D) \frac{1}{f}$$





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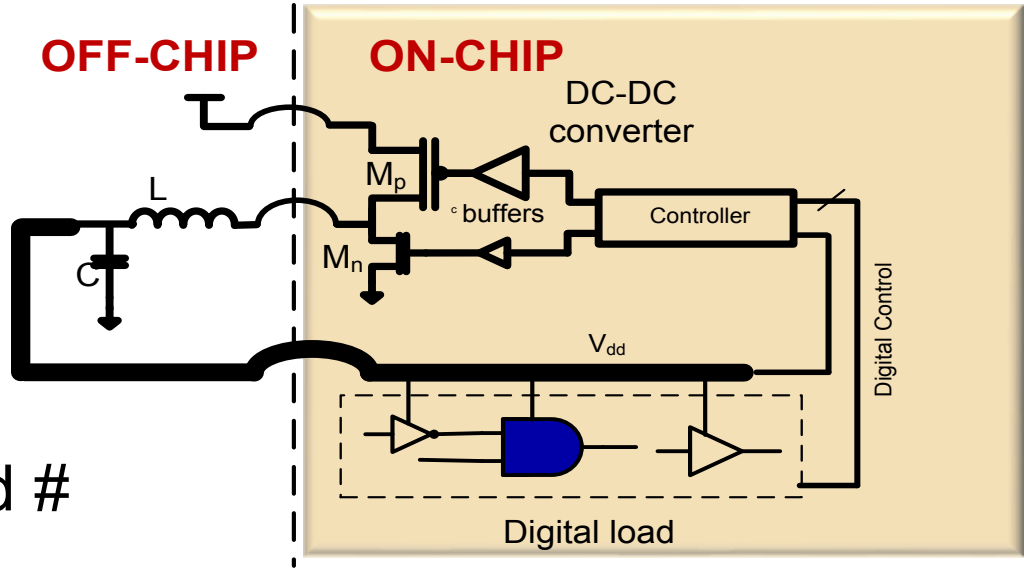
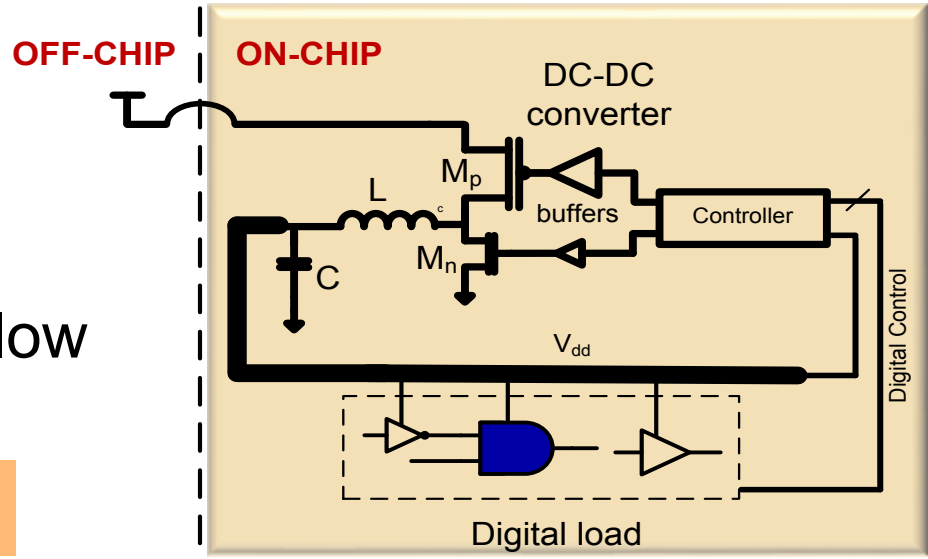
# Why Fully Integrated Converters ?

- Passives off-chip
  - ✓Large L and C possible
  - ✓Good quality of L and C
  - x Higher BOM
  - x Large pin-count
  - x Power domains → limited #
- Fully integrated converter
  - ✓Small pin count
  - ✓Lowest BoM
  - ✓Power domains → large #
  - x Small L and C , Quality of L low
  - x Consumes silicon area
- Goal: reduce on-chip overhead





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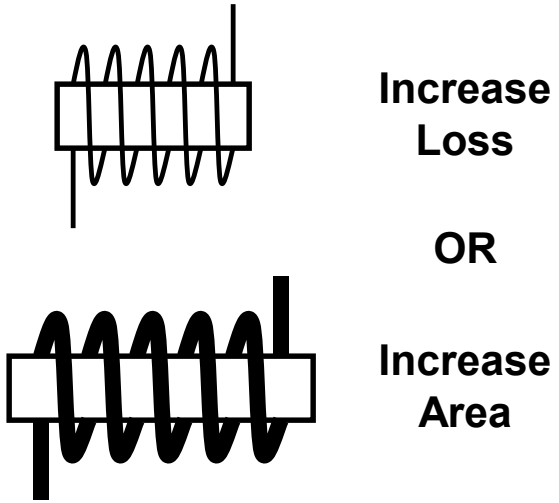
# Integration - Inductors

- **Output filters require high inductance (1μH to 100μH)**
- **High inductance results in**
  - Large area
  - High series resistance resulting in low efficiency
- **1-3nH integrated inductors have reasonable series resistances**
- **Low inductance generates large current ripple resulting in**
  - Large output voltage ripple
  - Low efficiency

- **Strategy for integration**
  - Interleaving: makes output independent of inductor current ripple
  - Magnetic coupling: reduces current ripple magnitude at inductor
    - On-chips are close and so have coupling

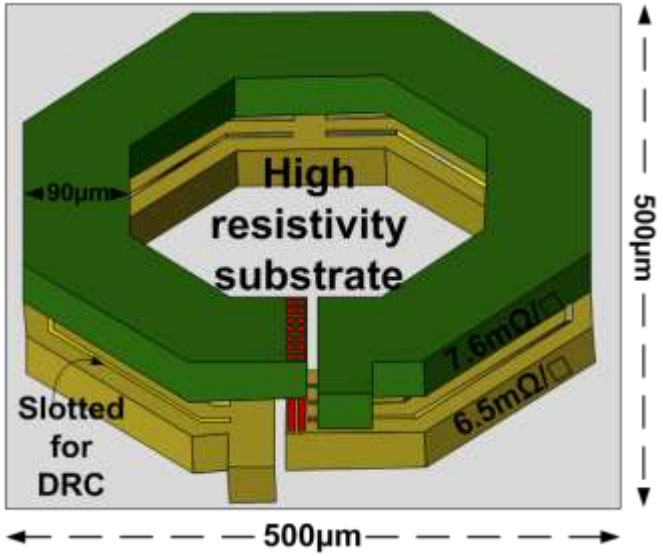


© Ramesh Harjani

# Inductors

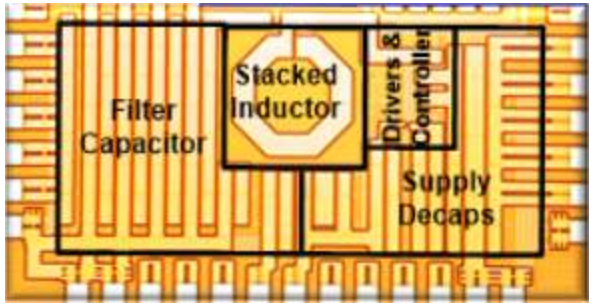
- Inductors
  - Area bulky (**1nH/0.2mm2**)
  - High quality factor – a problem (typically **1nH/150mOhm**)

- Examples




- Diameter: 600 µm
- Metal Width: 75 µm
- Turns: 1.75
- Spacing: 4.5 µm

# Fully Integrated On-Chip DC-DC Converter with a 450x Output Range




**Process: IBM 130nm CMOS**
**Sudhir Kudva**
**CICC 2010, JSSC 2011**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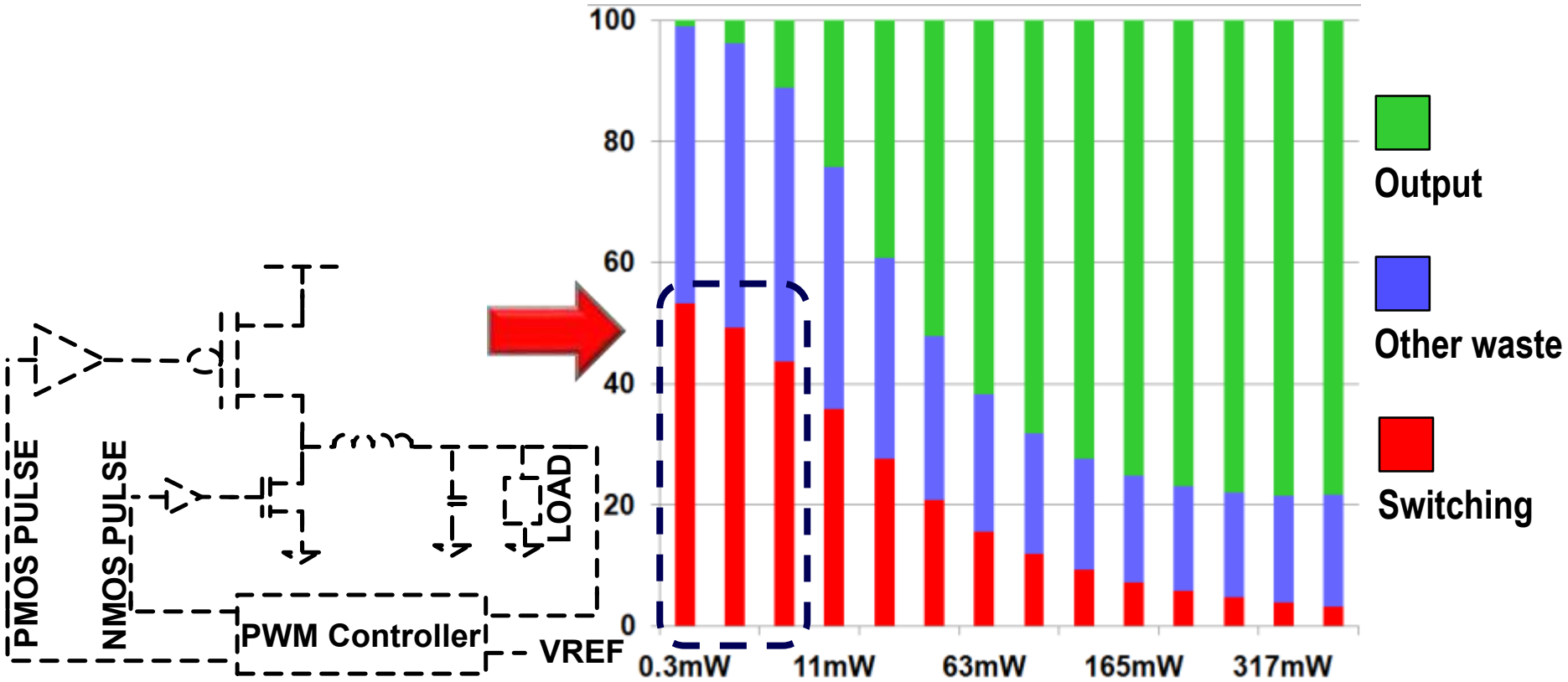
# Typical Buck Converter

- Switching power significant % of wasted power @ lower currents





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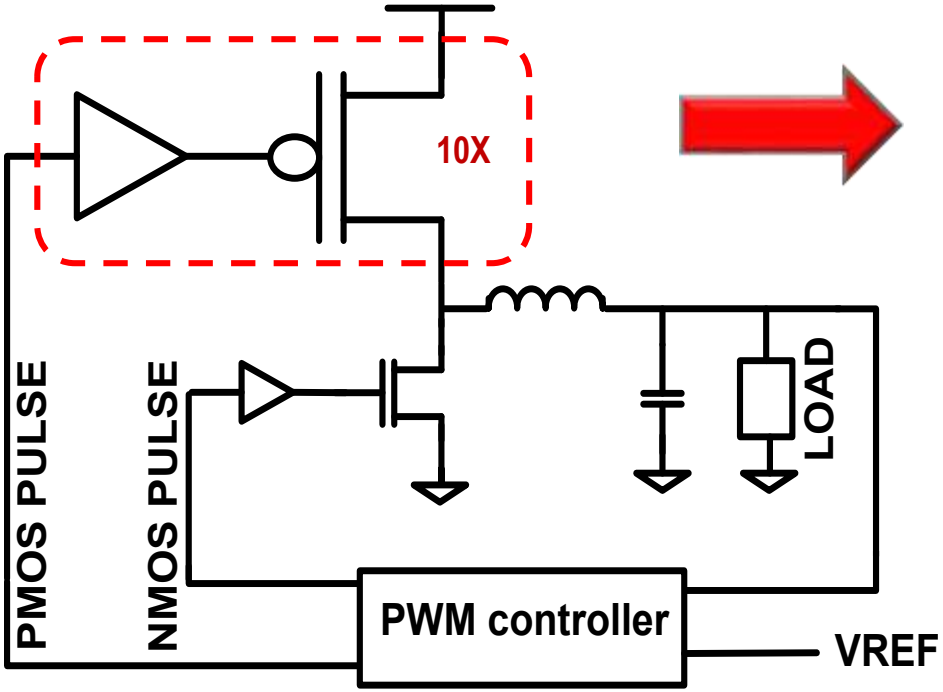
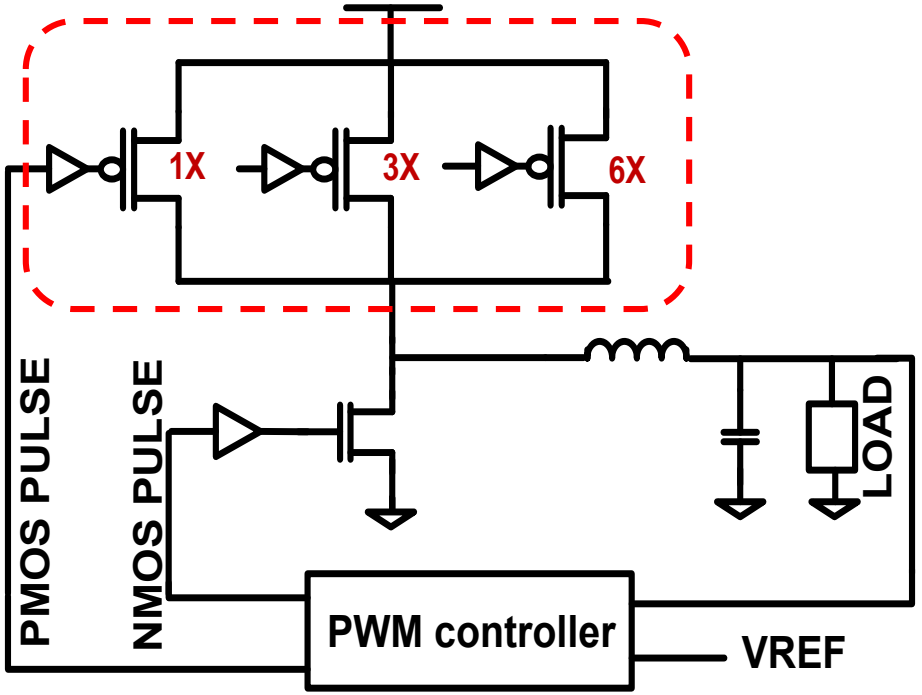
# Modified Circuit

- Split PMOS switch and the drivers
- Size of the nail decides the hammer
- Only PMOS variable ➔ larger PMOS to handle larger current





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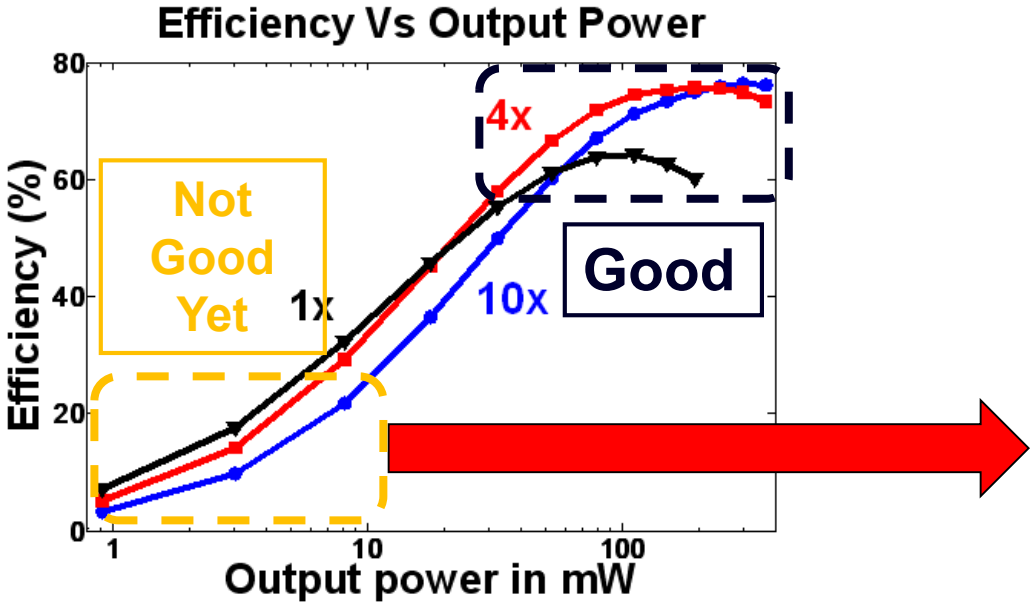
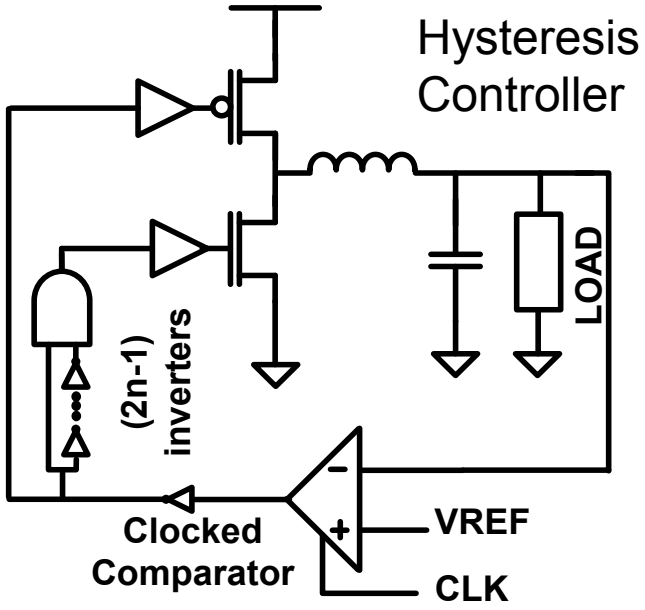
# Hysteresis Controller

- Improved efficiency at high output loads
- However, still low efficiency at low loads
- Switch pulse frequency depend on the load current
- Effectively variable switching frequency
- PMOS and NMOS both OFF for some time





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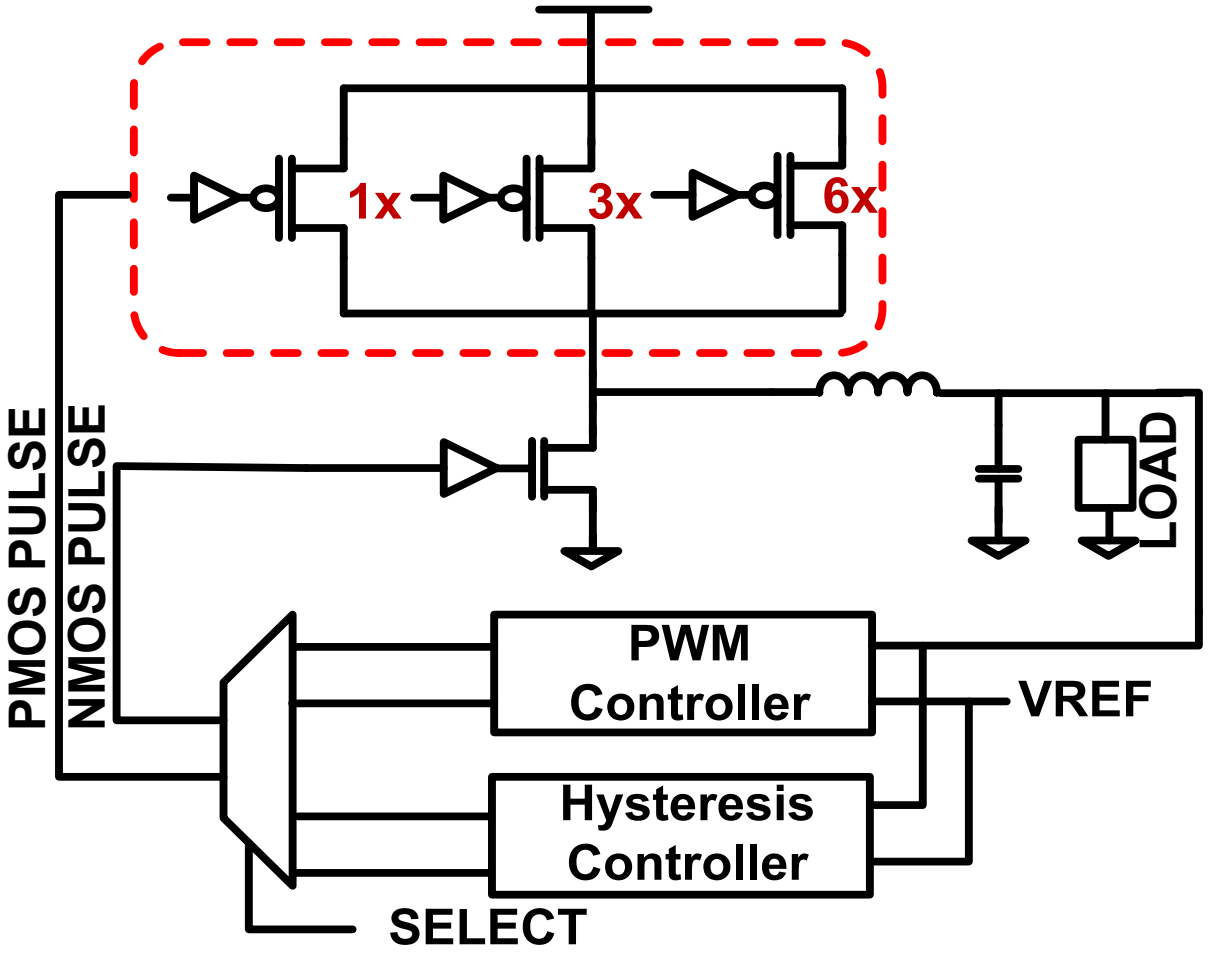
# Integrated Converter

- Variable PMOS switches → 10x,4x,1x
- High load ➔ PWM, Low load ➔ Hysteresis





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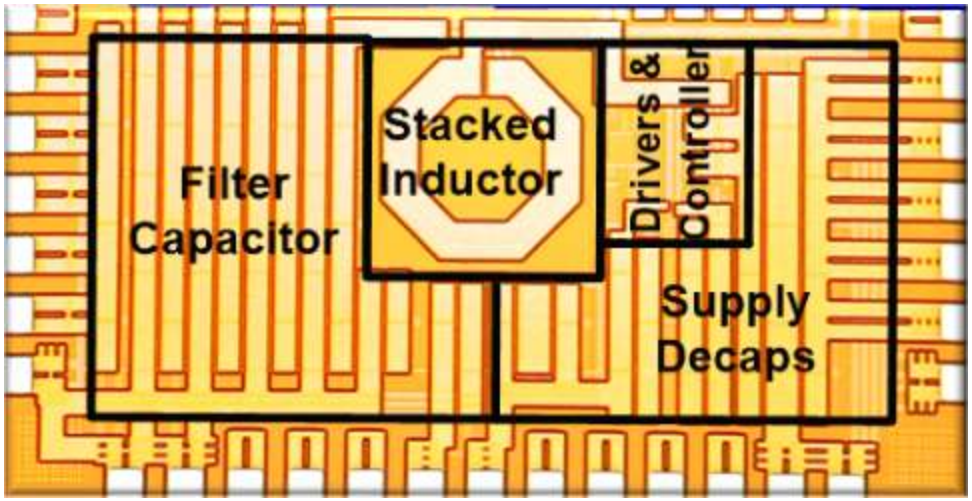
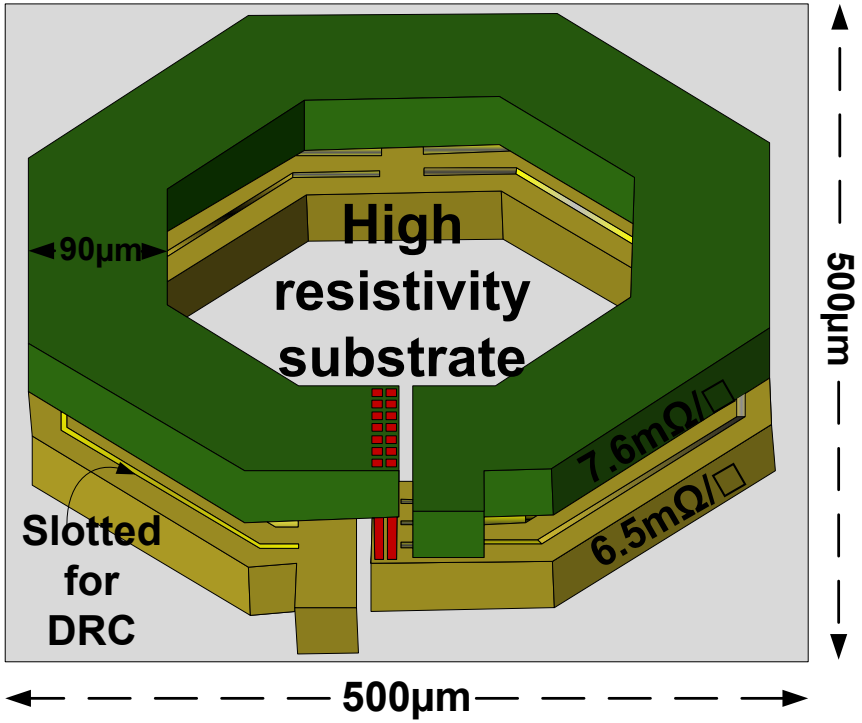
# Chip Photograph

- IBM 130nm CMOS process
- Converter core area – 1.13mm$^2$
- Total area with supply decaps – 1.592mm$^2$
- Capacitance – 5nF  Inductance - 2nH





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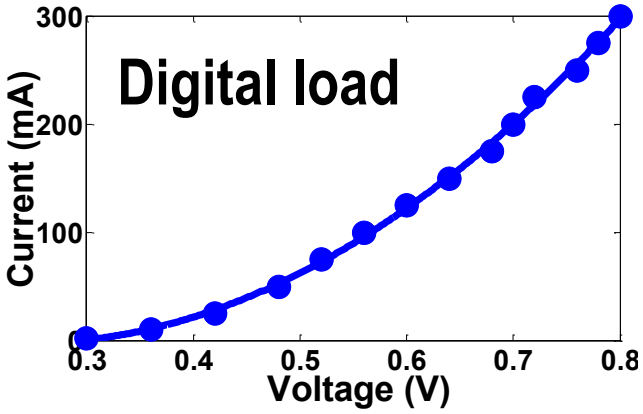
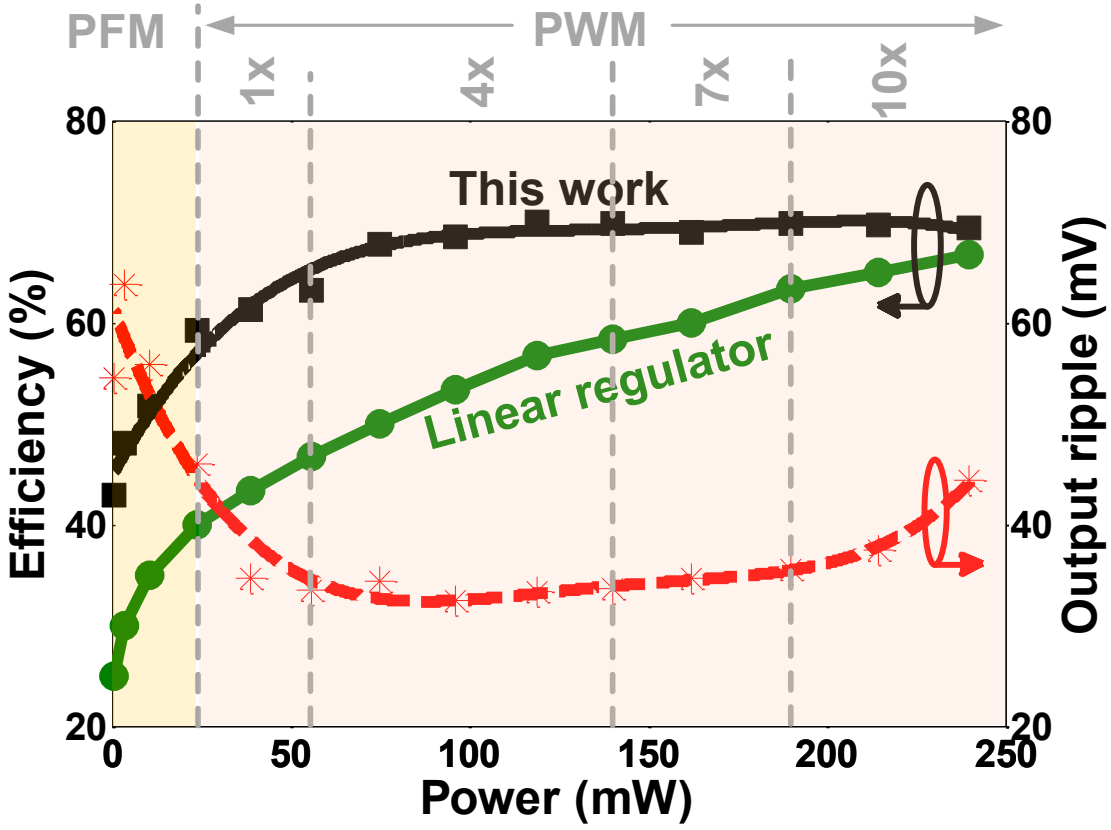
# Measurement Results: Efficiency

- Current increases quadratically with voltage
- Quadratic fit shown




- Efficiency is maximized at all loads by changing operating modes





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# Inductive: Comparison

| | O/P Power (mW) | O/P Power range | Efficiency (%) | Inductor/ Capacitor | Passive Components |
|---|---|---|---|---|---|
| **Musunuri PESC 2005** | 50 – 200 | ~4X | 40 - 60 | 0.1μH/30nF | MEMS inductor |
| **Xiao JSSC 2004** | 0.15-600 | ~4000X | 70 - 92 | 10μH/47μF | Off-chip inductor and capacitor |
| **Wibben JSSC 2008** | 3 – 315 | ~100X | 10 - 78 | 2x2nH/5nF | On-chip inductor and capacitor |
| **Abedinpour T PE 2007** | 95 – 400 | ~4X | 35 - 64 | 2x11nH/6nF | On-chip inductor and capacitor |
| **This work** | 0.6–266 | ~450X | 42.8 - 74.5 | 2nH/5nF | On-chip Inductor and capacitor |

**This work provides best on-chip performance**


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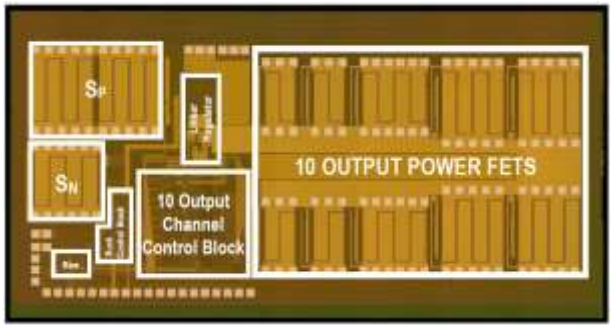
# An Error Based Controlled Single Inductor 10 Output DC-DC Buck Converter with High Efficiency at Light Load




**Process: 0.35um Process**
**Min-yong Jung**
**ISSCC 2015**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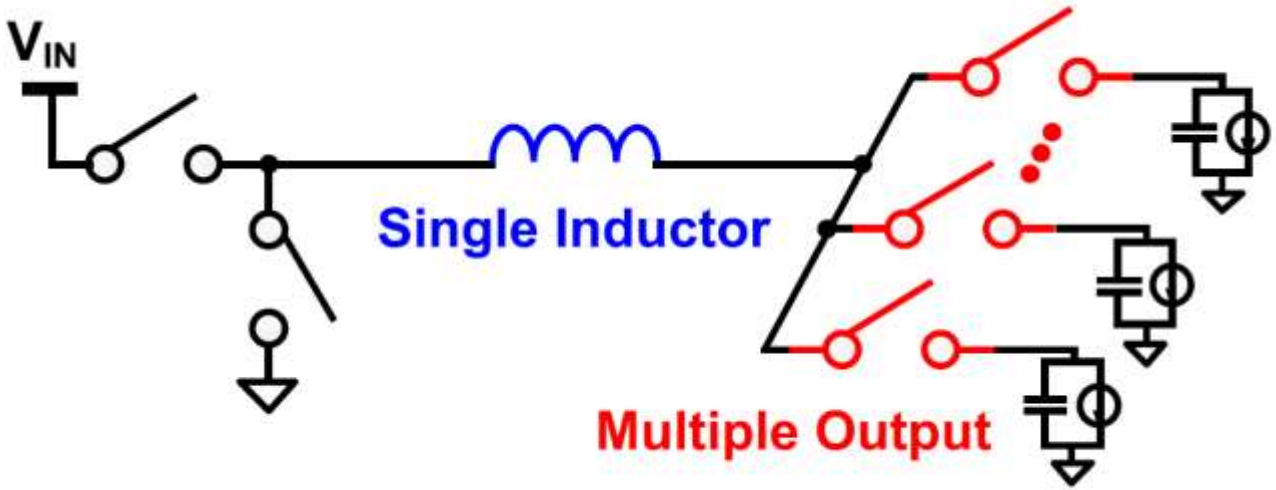
# Advanced Inductive Converter

- Single Inductor Multiple Output **(SIMO)** inductive converter




- **Problems**
  - ✓ Cross Regulation
  - ✓ Large Ripple
  - ✓ Poor Efficiency at Light Load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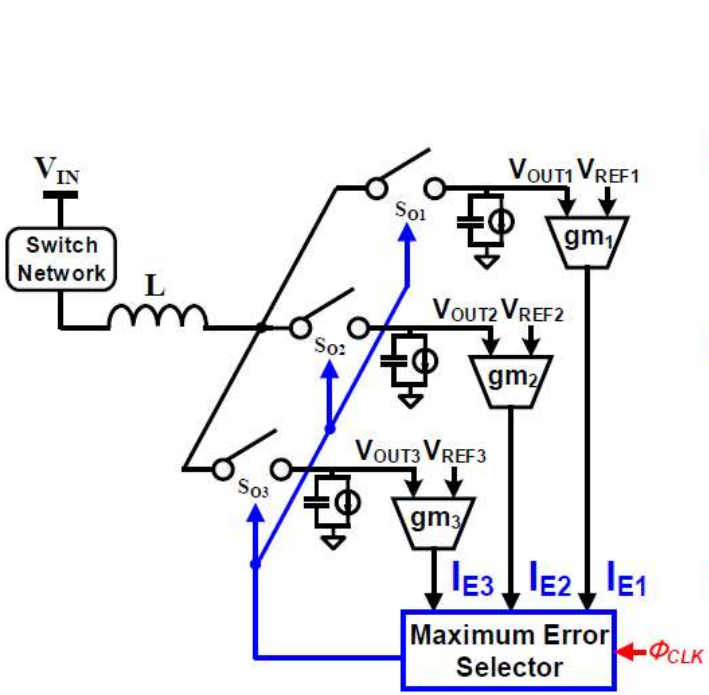
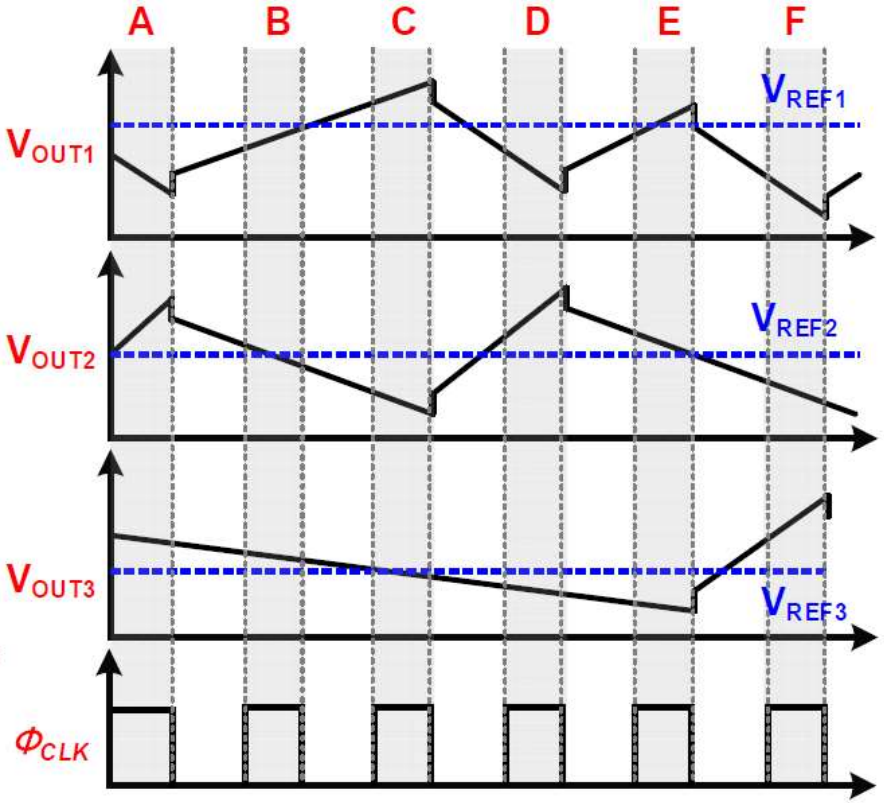
# Error Based Control

- Turning on the switch which has the largest error




**$\Phi_{CLK}$ → Error Compare → Turn on the Switch (Max Error)**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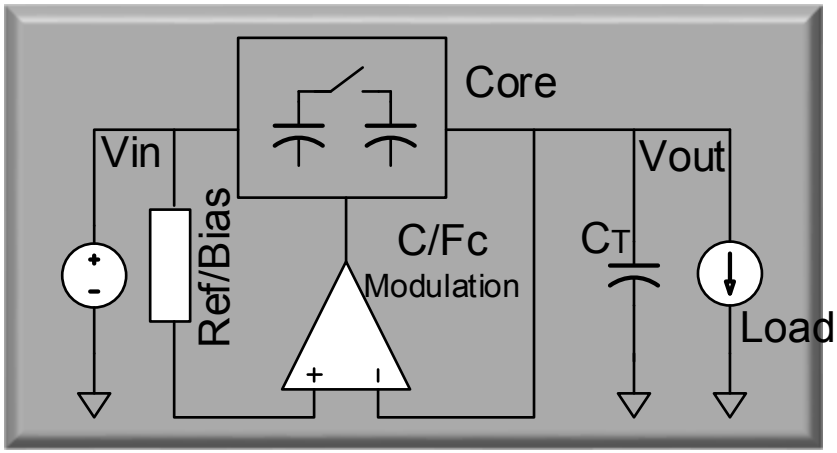
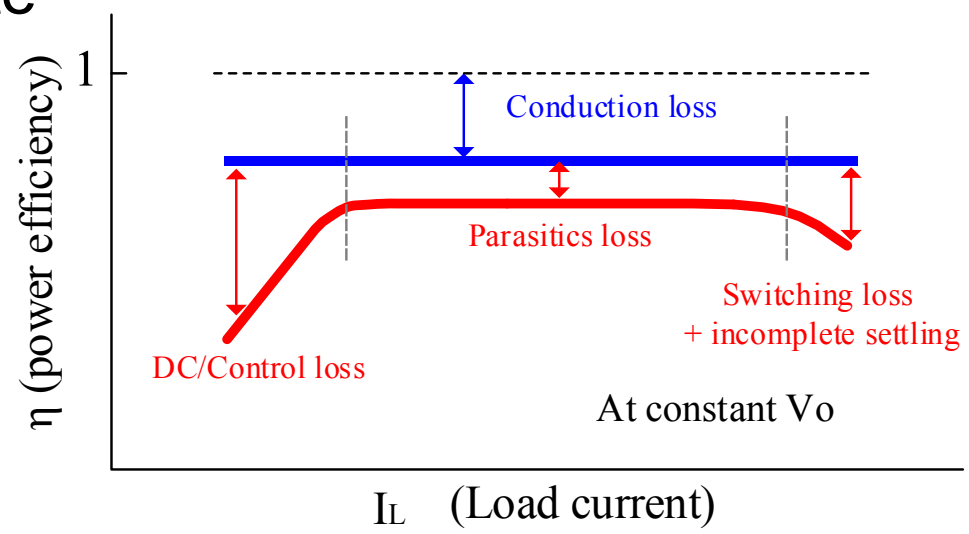
# CAPACITIVE CONVERTER

# Capacitive Conversion Efficiency Trends

- Conduction loss : Fundamental – sets upper limit
- Parasitic loss: sets peak value
- DC control losses: almost constant with load – dominate at lighter loads
- Partial charging loss: dominates at higher loads




Capacitive DC-DC converter





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# Present Day Integrated Capacitors

- Power density → capacitive density
- Desired qualities of integrated capacitor
  - Low bottom plate capacitance
  - High density, low leakage, low ESR
- MIM (Metal Insulated Metal)
  - Low density, low bottom plate parasitic, expensive
- MOM (Metal Oxide Metal)
  - High parasitic, low density, cheap
- MOS (Inversion)
  - High density,  high leakage, medium bottom plate
- Floating Junction High Density Capacitor
  - Low Leakage, higher density


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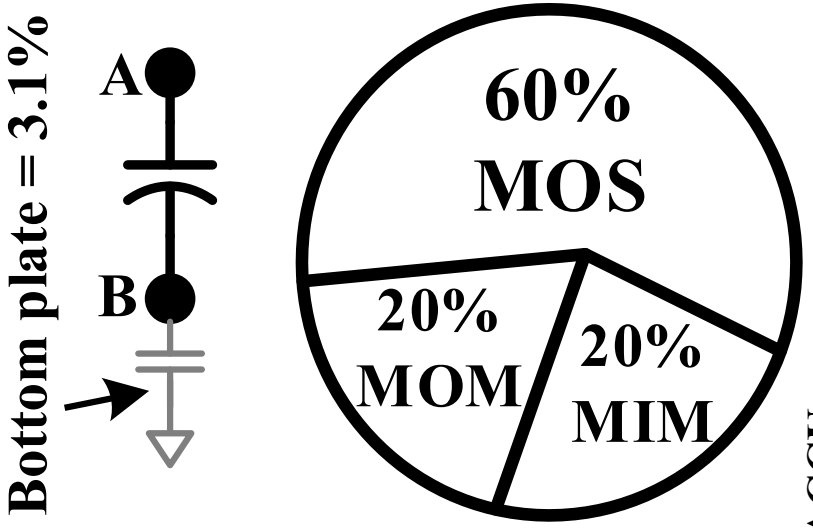
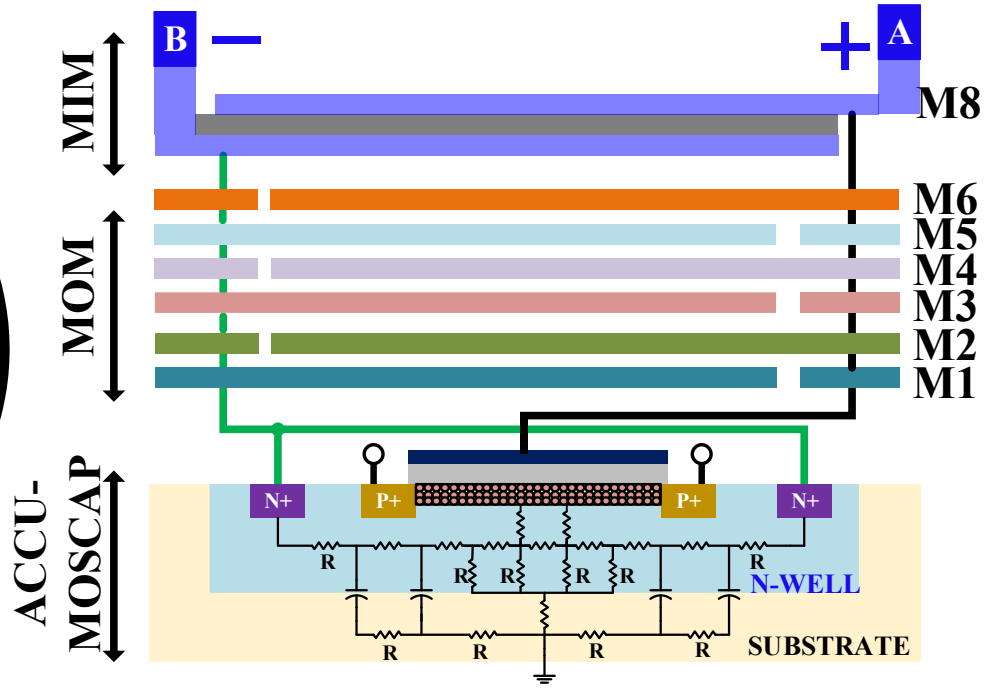
# Passives I: Floating Junction HD Cap

- Wide output power range
  - Desired constant efficiency over output
  - Modular open loop helps





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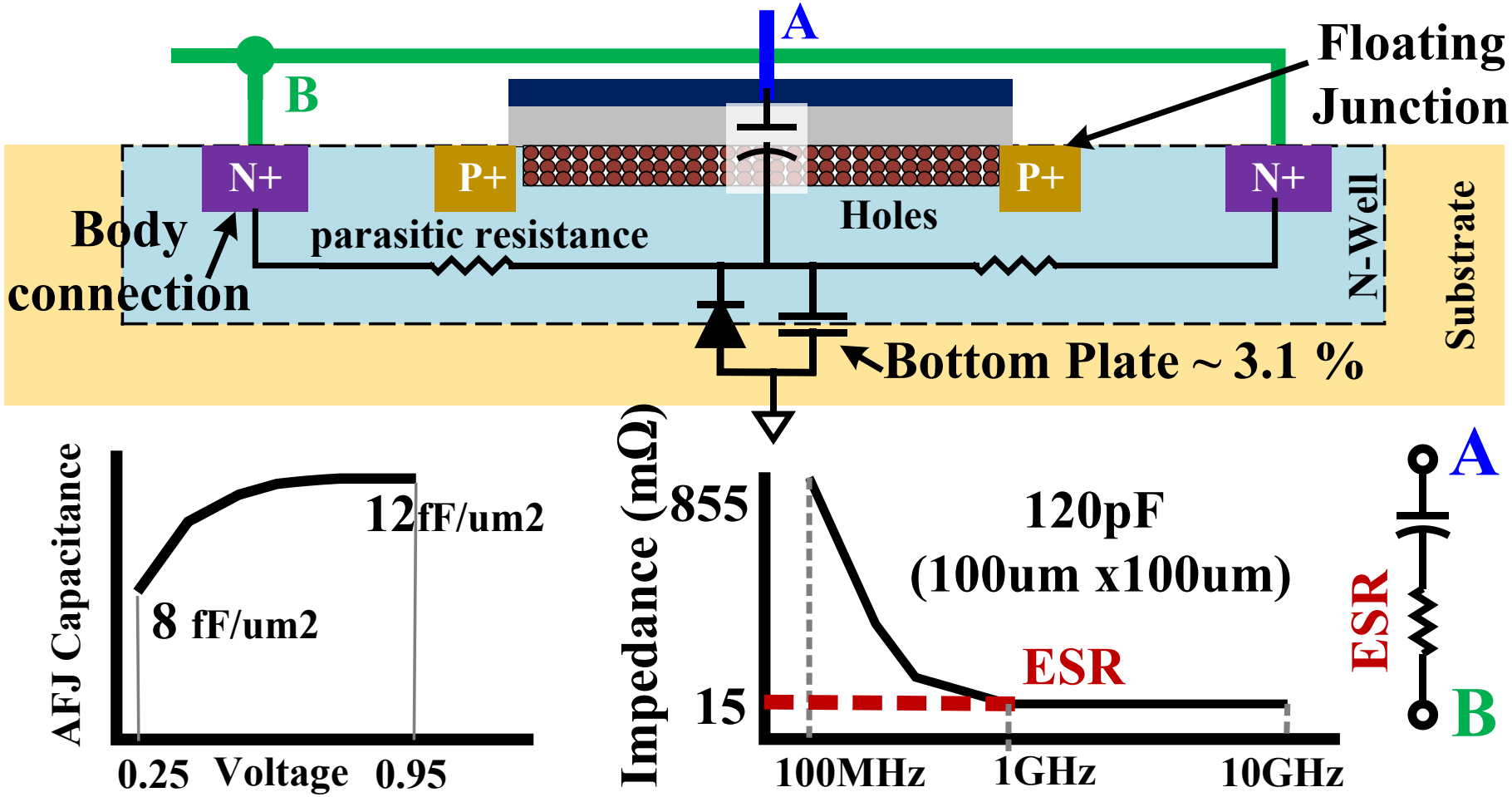
# Passives II

- Cross section - Accumulation Floating Junction (AFJ)





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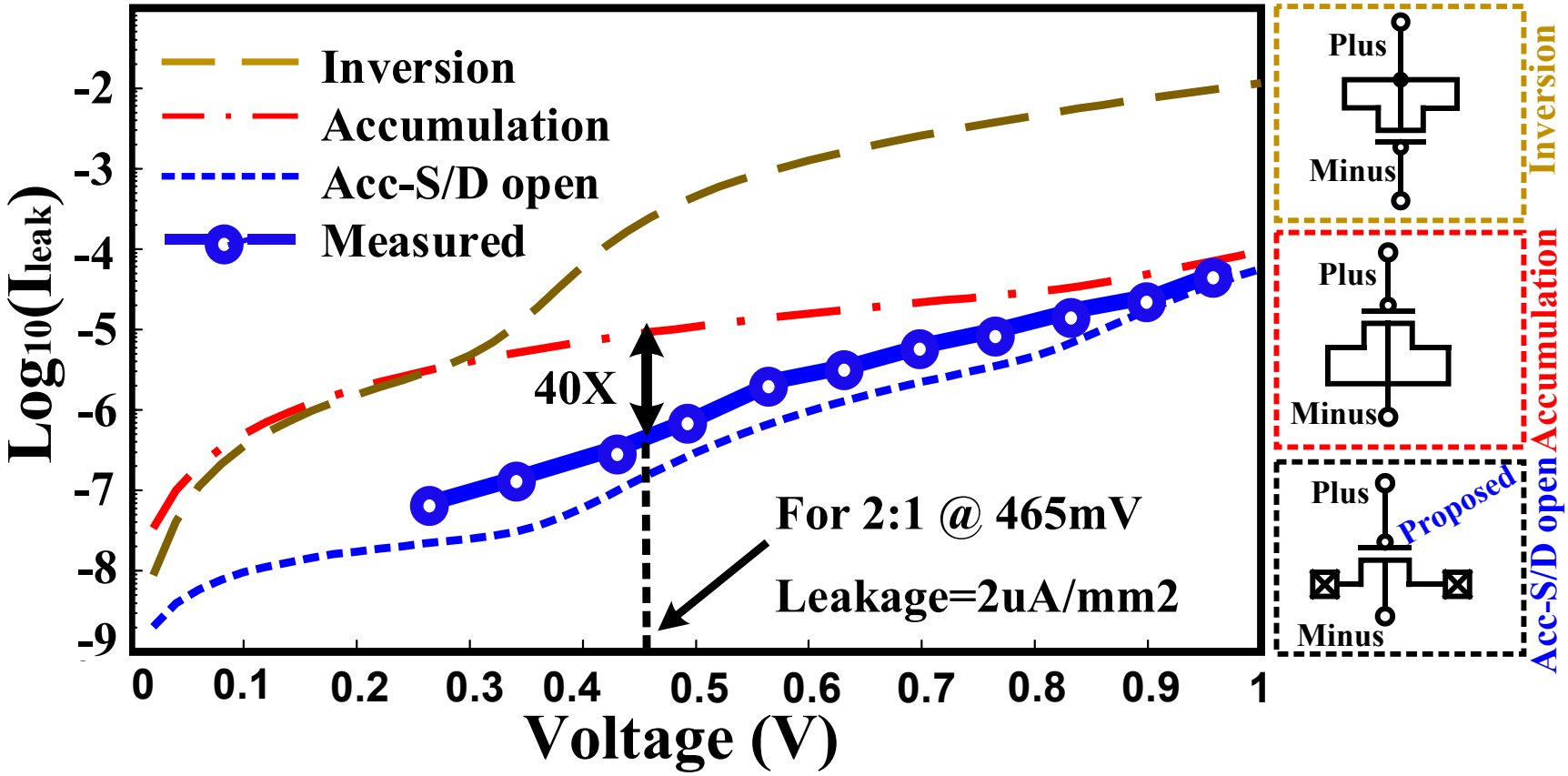
# Passives III (Leakage Measurement)

- 40X improvement
- Floating source/drain





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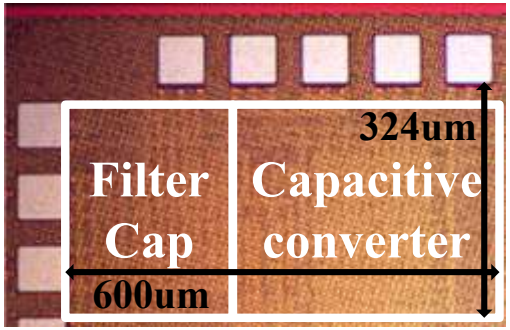
# Unified Series Parallel Capacitive DC-DC Converter Framework




Ramesh Harjani, Saurabh Chaubey,
CICC 2014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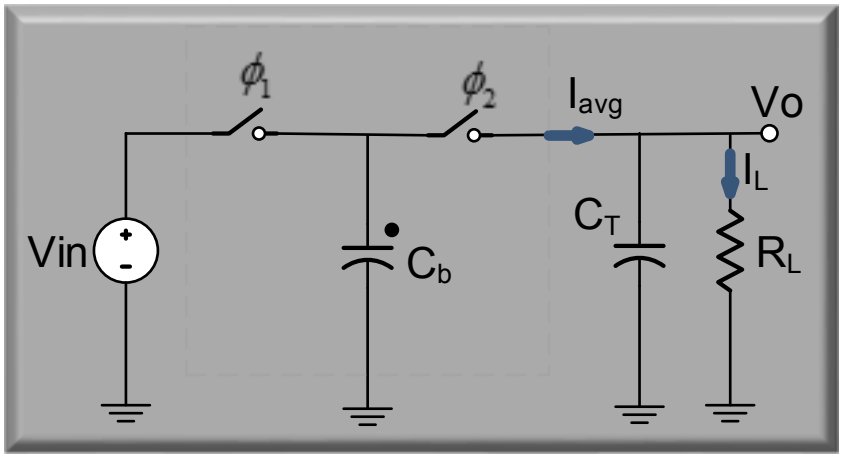
# 1:1 Converter (IPG-OPG)

- Figure shows a 1: 1 capacitor converter
  - I.e., the maximum voltage at the output is Vin, $(Vo \le Vin)$
- Bucket capacitor, $C_b$, charged to Vin during input $\Phi_1$
- $C_b$ discharge to Vo during $\Phi_2$
- The tank capacitor is much larger $C_T >> C_b$
  - I.e., Vo can be assumed to be fairly constant




**IPG-OPG Capacitive Converter**

$$\Delta Q = (Vin - Vo)Cb \text{ per cycle}$$

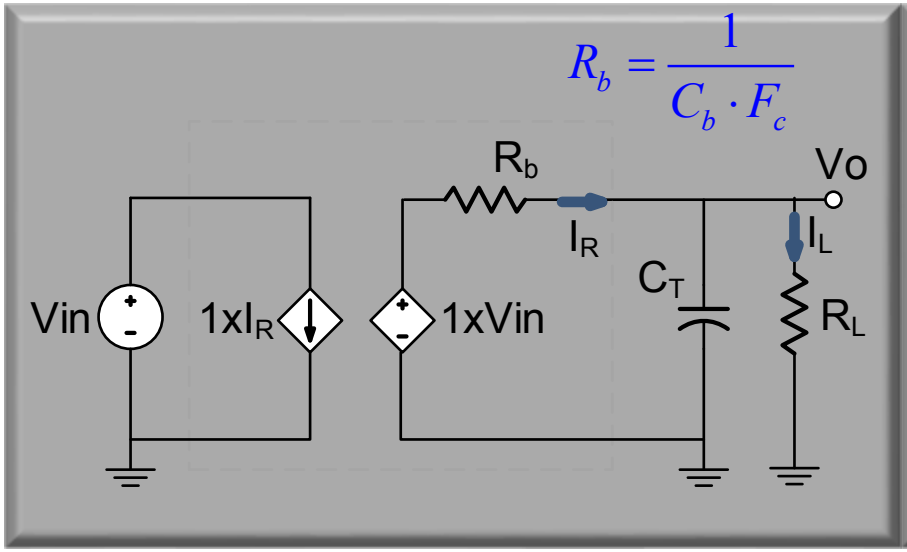
$$I_{avg} = \Delta Q \cdot F_c = (Vin - Vo)Cb \cdot F_c = I_L$$

$$R_{avg} = \frac{\Delta V}{I_{avg}} = \frac{(Vin - Vo)}{(Vin - Vo)Cb \cdot F_c} = \frac{1}{Cb \cdot F_c}$$

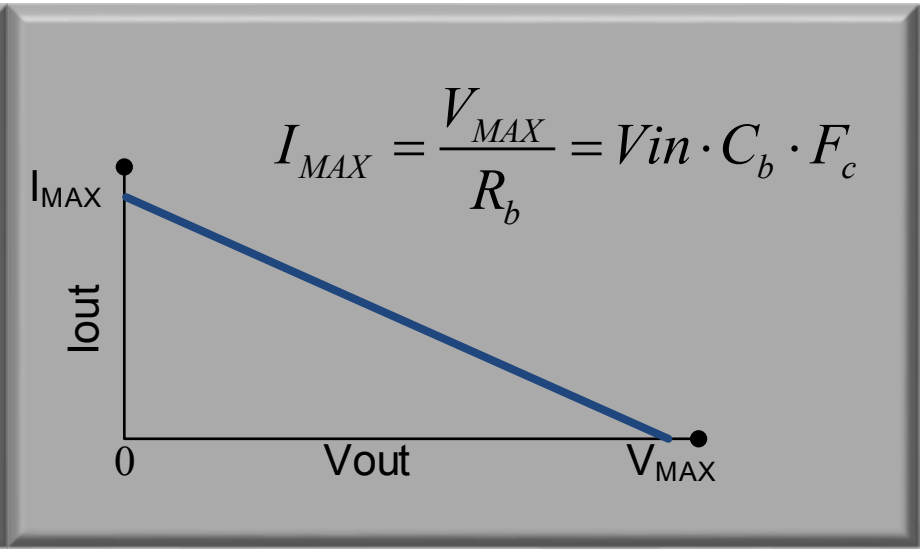

© Ramesh Harjani

# Transformer Model for IPG-OPG

- Transformer model for 1:1 capacitive converter
- Load line for IPG-OPG converter
- Maximum current when Vo approaches zero
- When Vo=Vin → no charge transferred to output




IPG-OPG Converter Transformer Model




IPG-OPG Load Line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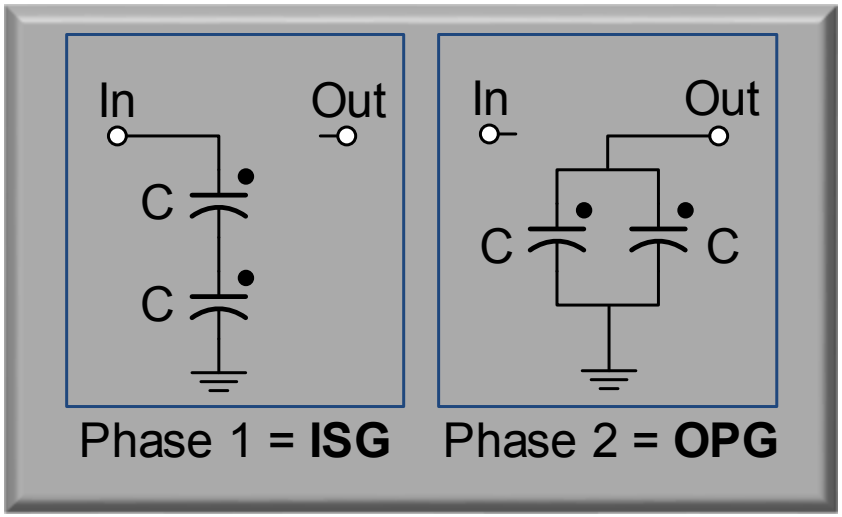
# Buck Converter #1 (ISG-OPG)(1 : ½)

- $\Phi_1$ each capacitor charged to Vi/2
- $\Phi_2$ both capacitors discharged to Vo




$$\Delta Q_1 = 0$$

$$\Delta Q_2 = 2\left(\frac{Vi}{2} - Vo\right)C$$

$$Io = \left(2\left(\frac{Vi}{2} - Vo\right)C + 0\right)F_c$$

$$Ro = \left(\frac{Vmax - \mathrm{Vo}}{Io}\right) = \frac{1}{2 \cdot C \cdot Fc}$$

$$Vmax = \frac{Vi}{2}$$

$$Ro = \frac{1}{N \cdot C \cdot Fc}$$

$$Area = N \cdot Area_c$$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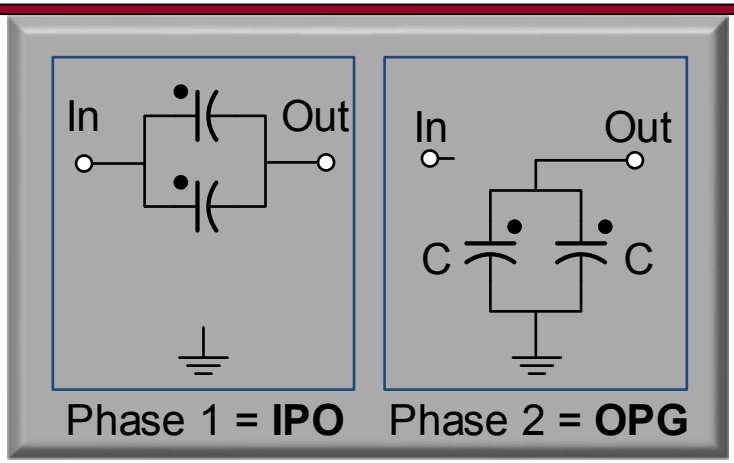
# Buck Converter #2 (IPO-OPG) )(1 : ½)

- $\Phi_2$ caps parallel to Vout
  - Charged to Vout
- $\Phi_1$ caps in parallel between input and output
  - Caps charged to Vin-Vo
- Charge transferred to output during each phase
- Calculating Vmax




$$\Delta Q_1 = \left[\left(Vi - Vo\right) - Vo\right] 2C$$

$$\Delta Q_2 = \left[\left(Vi - Vo\right) - Vo\right] 2C$$

$$Io = \left(\Delta Q_1 + \Delta Q_2\right) Fc$$

$$= 2\left(\frac{Vi}{2} - Vo\right) 4C \cdot Fc$$

$$\left(Vin - Vo\right) = Vo \rightarrow V_{\max} = \frac{Vin}{2}$$

$$Area = N \cdot Area_c$$

$$Ro = \frac{1}{4N \cdot C \cdot Fc}$$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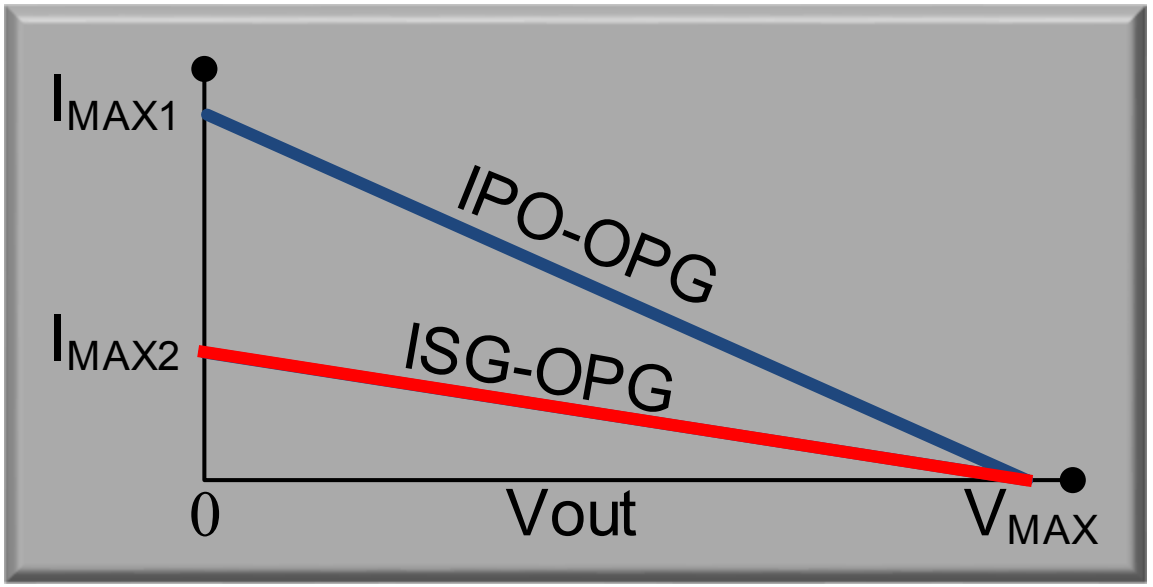
# Quick Summary: Topology Selection

- Same total capacitance used to compare designs
  - N=2, C=1
- Some topologies are just better than others
  - Lower Ro ➔ can provide larger current
  - **IPO-OPG:** charges during Φ1 and Φ2 ➔ lower ripple

$$Ro = \frac{1}{4N \cdot C \cdot Fc}$$

$$Ro = \frac{1}{N \cdot C \cdot Fc}$$





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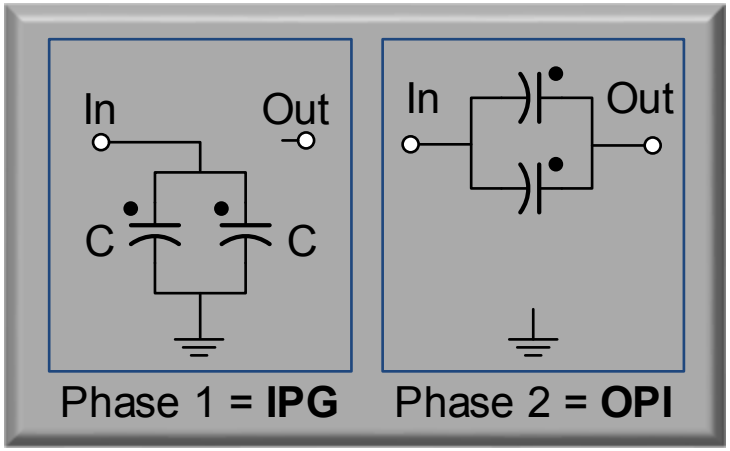
# Boost Converter: (IPG-OPI) )(1 : 2)

- $\Phi_1$ parallel capacitors connected to Vi
- $\Phi_2$ parallel capacitors between Vo and Vi
  - Note phase of capacitors
- Calculating Vmax




$$Vi = -(Vo - Vi)$$

$$Vmax = 2Vi$$

$$\Delta Q_1 = 0$$

$$\Delta Q_2 = [(Vi - Vo) + Vi]2C$$

$$Io = [0 + (2Vi - Vo)2C]Fc$$

$$Ro = \frac{1}{N \cdot C \cdot Fc}$$

$$Area = N \cdot Area_c$$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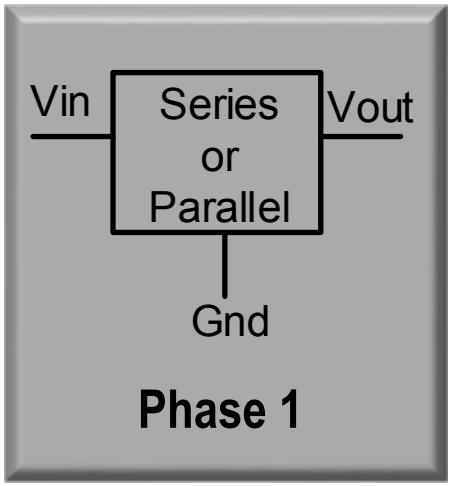
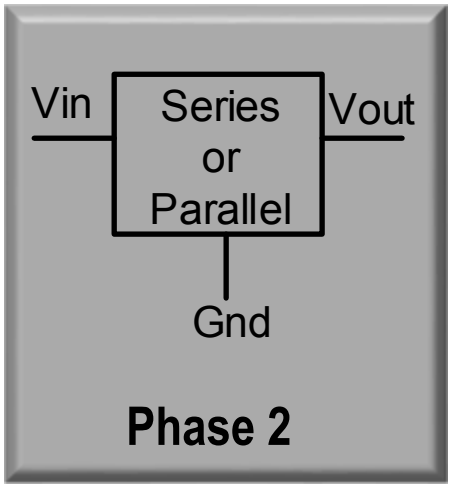
# Design Rules

- Motivation
  - Currently, ad hoc single point solutions
  - No generalized set of topologies & equations
- Heuristic rules
  - Ripple voltage is small
  - Only three terminal designs
  - All bucket caps same size
  - All bucket caps move as one group
  - The bucket caps are in series or parallel
  - A cycle is composed of two phases
  - All three terminals used during each cycle





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*Ref: Ron Balczewski and Ramesh Harjani, IEEE International Symposium on Circuits and Systems, 2001*

# Nomenclature

- Phase notation we will use

| Position | Code | Description |
|---|---|---|
| 1st | I, G, O | 1st connection (Input, Output, Gnd) |
| 2nd | P, S | Series or Parallel |
| 3rd | I, G, O | 2nd connection (Input, Output, Gnd) |

3x2x2 = 12 phases

| | | | | | |
|---|---|---|---|---|---|
| IPG | IPO | GPI | GPO | OPI | OPG |
| ISG | ISO | GSI | GSO | OSI | OSG |


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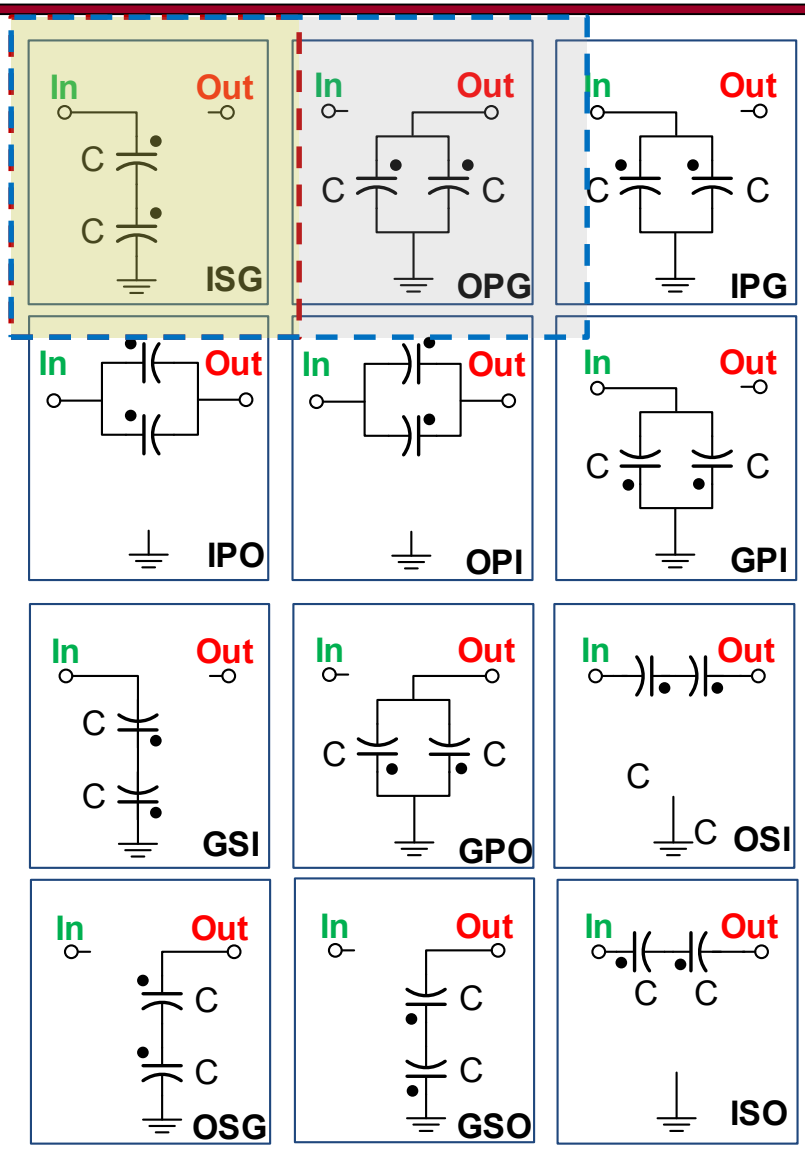
# 12 Distinct Configurations

**Configuration Topology**





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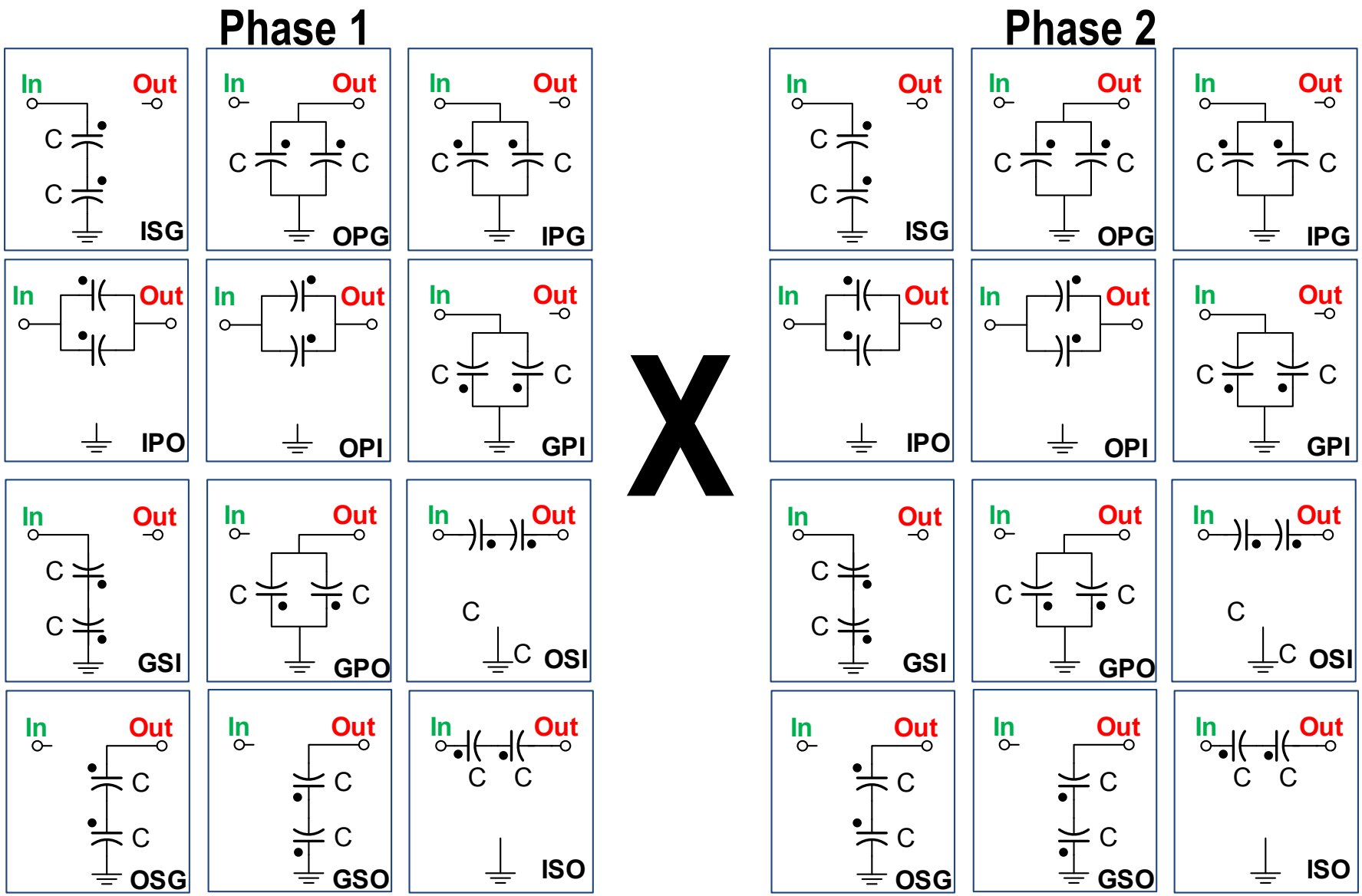
# Configuration to Topology





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# Enumeration

- 12 configurations for 1st phase
- For two phases (12 x 11=132) combinations
- Apply the heuristic rules: reduces to 96
- More heuristic rules
  - Same 2 phases but different order: ISG-IPO ; IPO-ISG
  - Series or parallel in both phases: ISG-ISO = IPG-IPO
  - Flipping 1st and 3rd letter (IPG-IPO=GPI-OPI)

**18 structurally unique topologies**

| | | | | | |
|---|---|---|---|---|---|
| IPG-IPO | IPG-GPO | IPG-OPI | IPG-OPG | IPG-ISO | IPG-GSO |
| IPO-GPO | IPO-OPG | IPO-ISG | IPO-GSI | IPO-GSO | GPO-ISG |
| GPO-OSI | IPG-OSI | IPO-OSG | IPG-OSG | GPO-ISO | GPO-GSI |


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# Derivation of Performance

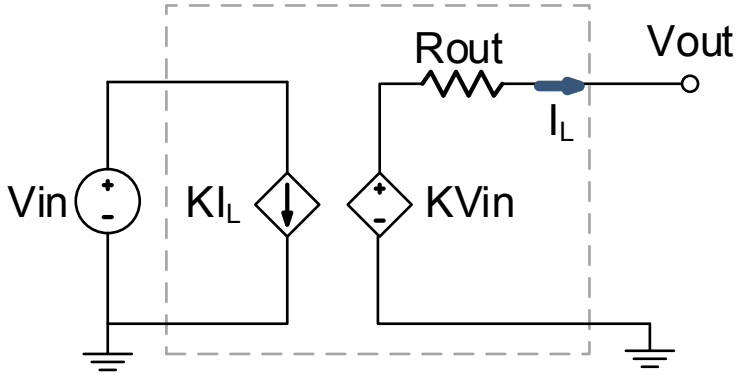
- Generic performance equations

$$Vmax = K \times Vin$$ → No load voltage

$$Iout = \left(F_{sw} \cdot C\right) \times f(Vin, Vout, N)$$ → Output current

$$Iratio = \frac{Iout}{Iin} = K$$ → Conversion ratio

$$Peff = \frac{Pout}{Pin} = \frac{Vout}{Vmax}$$ → Power efficiency





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# Performance Equations: Final Set

| MODE | K | Rout | Nmin |
|---|---|---|---|
| IPG-OSI | N+I | $\frac{N}{fC}$ | 2 |
| IPG-OPI | 2 | $\frac{1}{fCN}$ | I |
| ISG-OPI | $\frac{N+1}{N}$ | $\frac{1}{fCN}$ | 2 |

Boost performance equations

| MODE | K | Rout | Nmin |
|---|---|---|---|
| ISG-GPO | $-\frac{1}{N}$ | $\frac{1}{fCN}$ | 2 |
| IPG-GPO | $-1$ | $\frac{N}{fCN}$ | I |
| IPG-GSO | -N | $\frac{N}{fC}$ | 2 |

Negative performance equations

| MODE | K | Rout | Nmin |
|---|---|---|---|
| IPG-OPG | I | $\frac{1}{fCN}$ | 2 |
| IPO-OSG | $\frac{N}{N+1}$ | $\frac{N}{fC(N+1)^2}$ | I |
| IPO-OPG | $\frac{1}{2}$ | $\frac{1}{4fCN}$ | 2 |
| ISO-OPG | $\frac{1}{N+1}$ | $\frac{N}{fC(N+1)^2}$ | 2 |

Buck performance equations

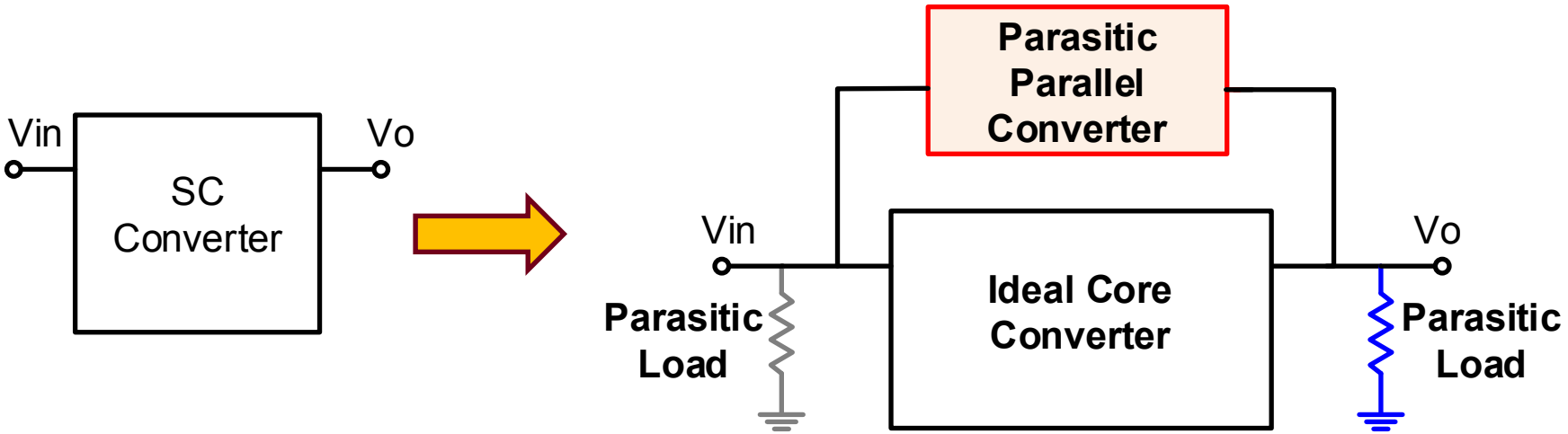
| | | | |
|---|---|---|---|
| IPG-OSG | OPI-OSG | IPO-ISG | ISG-OPG |
| ISO-GPO | IPG-ISO | IPG-IPO | OPG-OPI |

Non-optimum cases

**Only 10 Optimum Topologies**

# Modeling Capacitor Parasitics

- Top / bottom parasitics modeled as conduction loss
- Capacitor parasitics
  - Parasitic input load
  - Parasitic output load
  - Parasitic parallel converter





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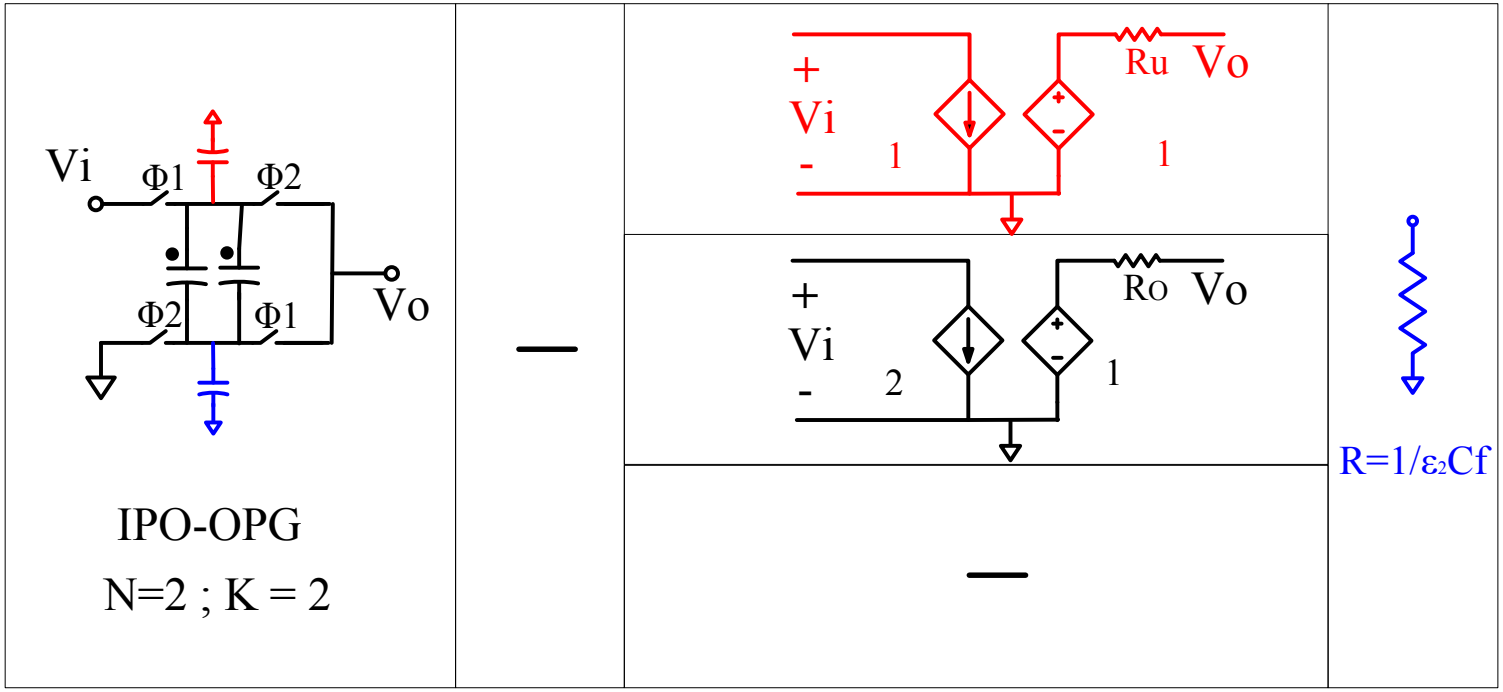
# Effect Of Parasitics

- Example: IPO-OPG
  - **Top plate acts as 1:1 parallel converter**
    - **Takes charge from Vin in $\Phi_1$ dumps on load in $\Phi_2$**
  - **Bottom plate acts as a passive load**
    - **Takes charge from Vout in $\Phi_1$ and dumps to ground $\Phi_2$**





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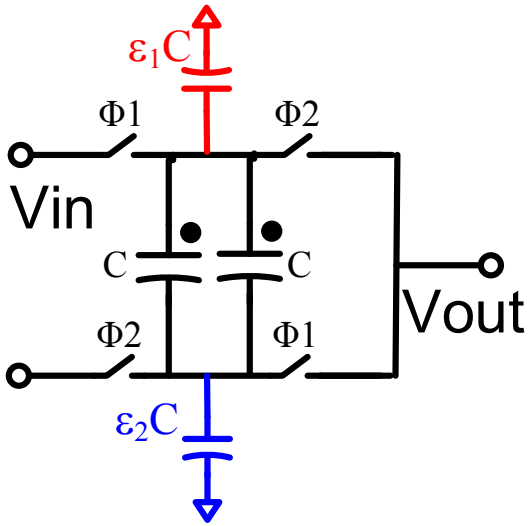
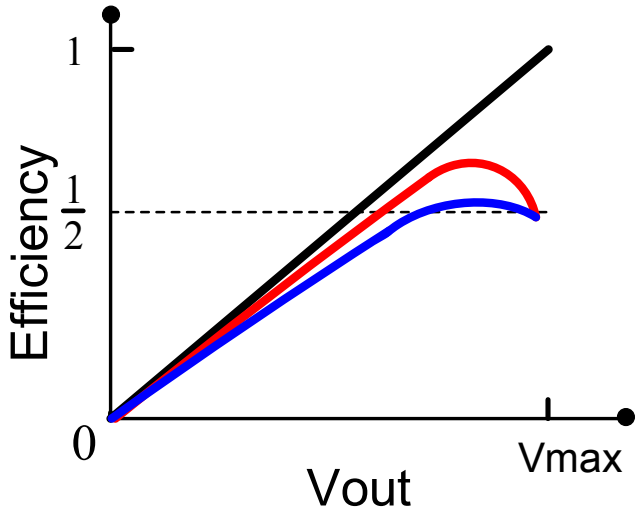
# Parasitic Modeling

- Bottom plate further reduces efficiency

$$\eta = \frac{\left[4\left(\frac{Vi}{2}-Vo\right)C_b f + \varepsilon_1\left(Vi-Vo\right)C_b f - \varepsilon_2 Vo C_b f\right]}{\left[2\left(\frac{Vi}{2}-Vo\right)C_b f + \varepsilon_1\left(Vi-Vo\right)C_b f\right]}\left(\frac{Vo}{Vi}\right)$$





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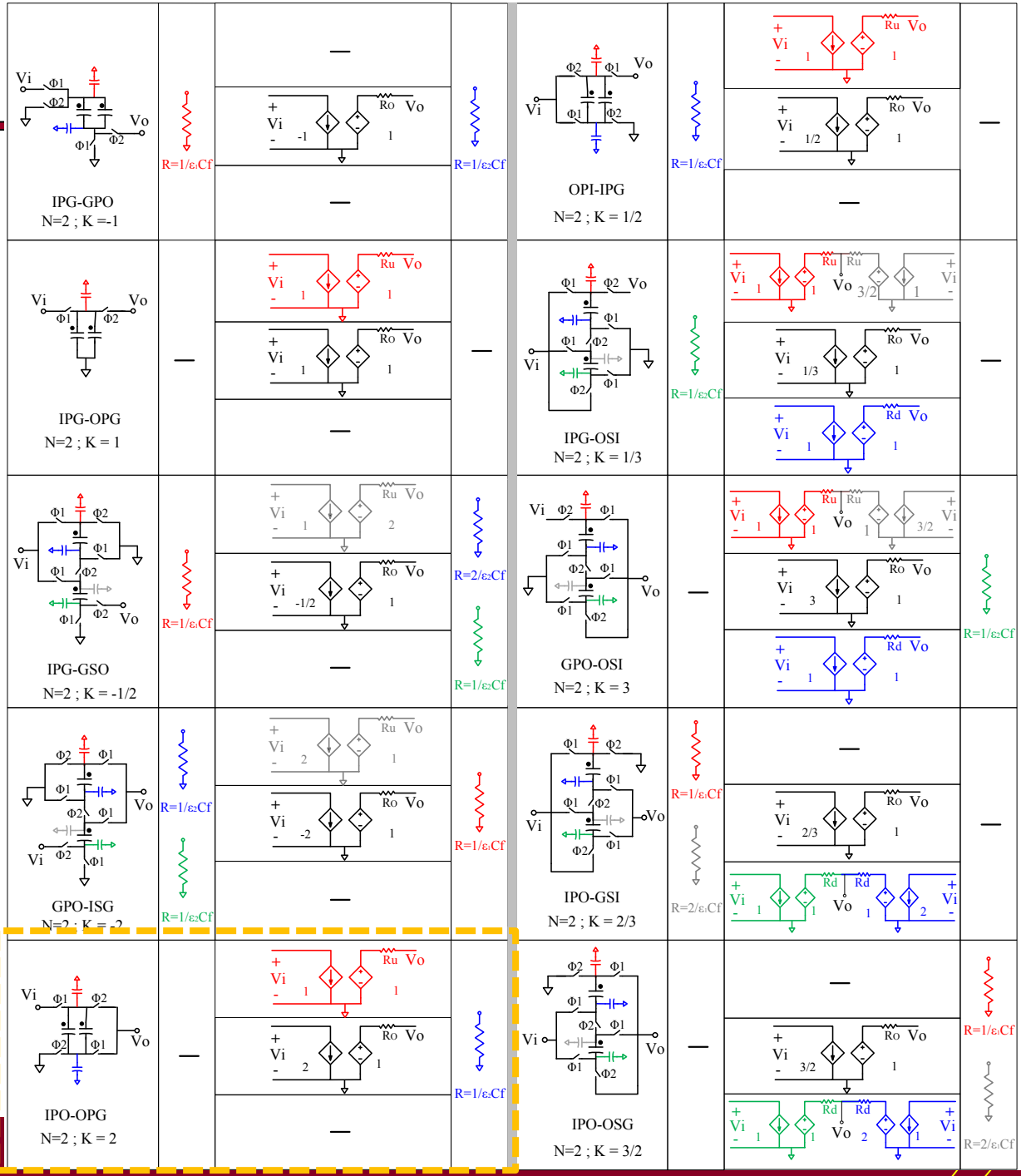
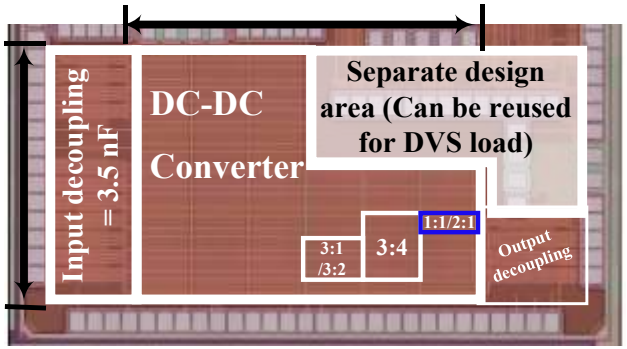
# Parasitics

- All 10 topologies
- For each topology
  - Primary converter
  - Parasitic input load
  - Parasitic output load
  - Parasitic converter



# Software Defined 3000X Output Current Range SC DC-DC Converter




**Process: TSMC 65 GP**

**Saurabh Chaubey**

**CICC 2017**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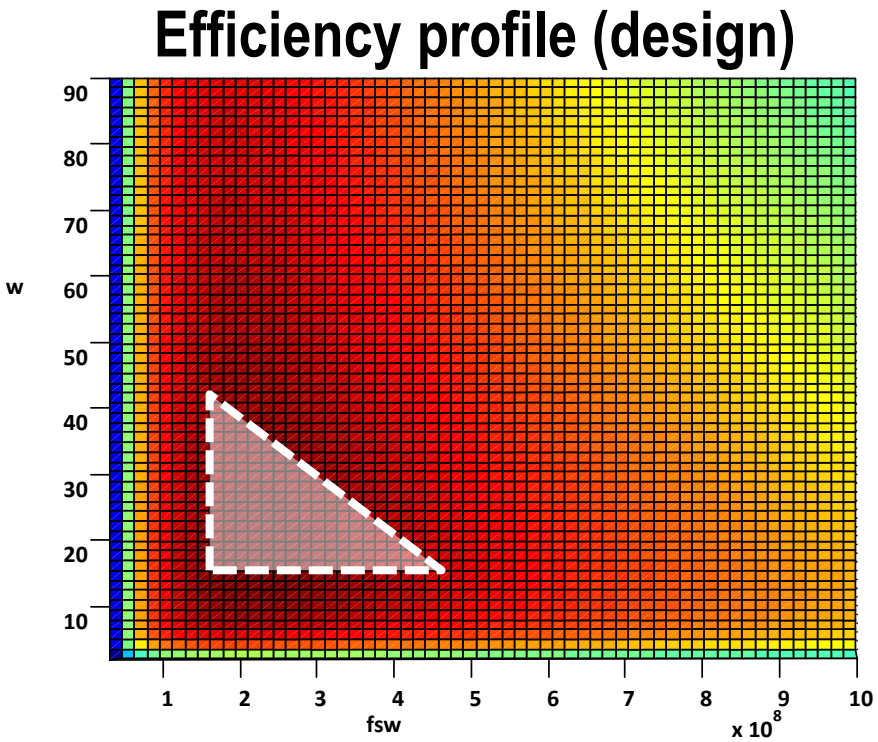
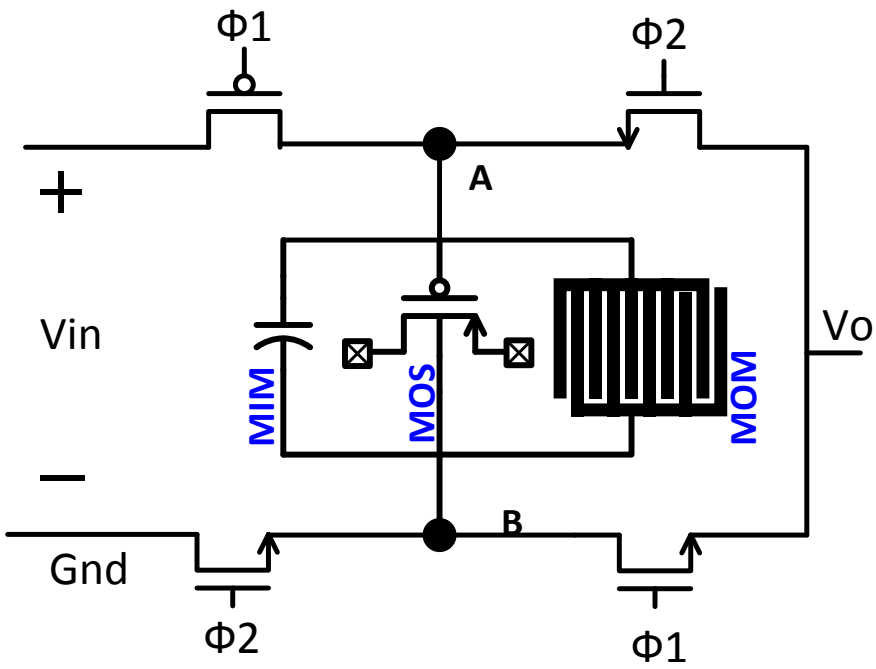
# Single DC-DC Conversion Module

- Converter consists of standard cells
  - Each cell → 2:1 converter (IPO-OPG)
  - 2:1 → 1 IPO-OPG , 3:1 → 2 IPO-OPG and so on
  - Passives → custom high density cap → **180 pF**





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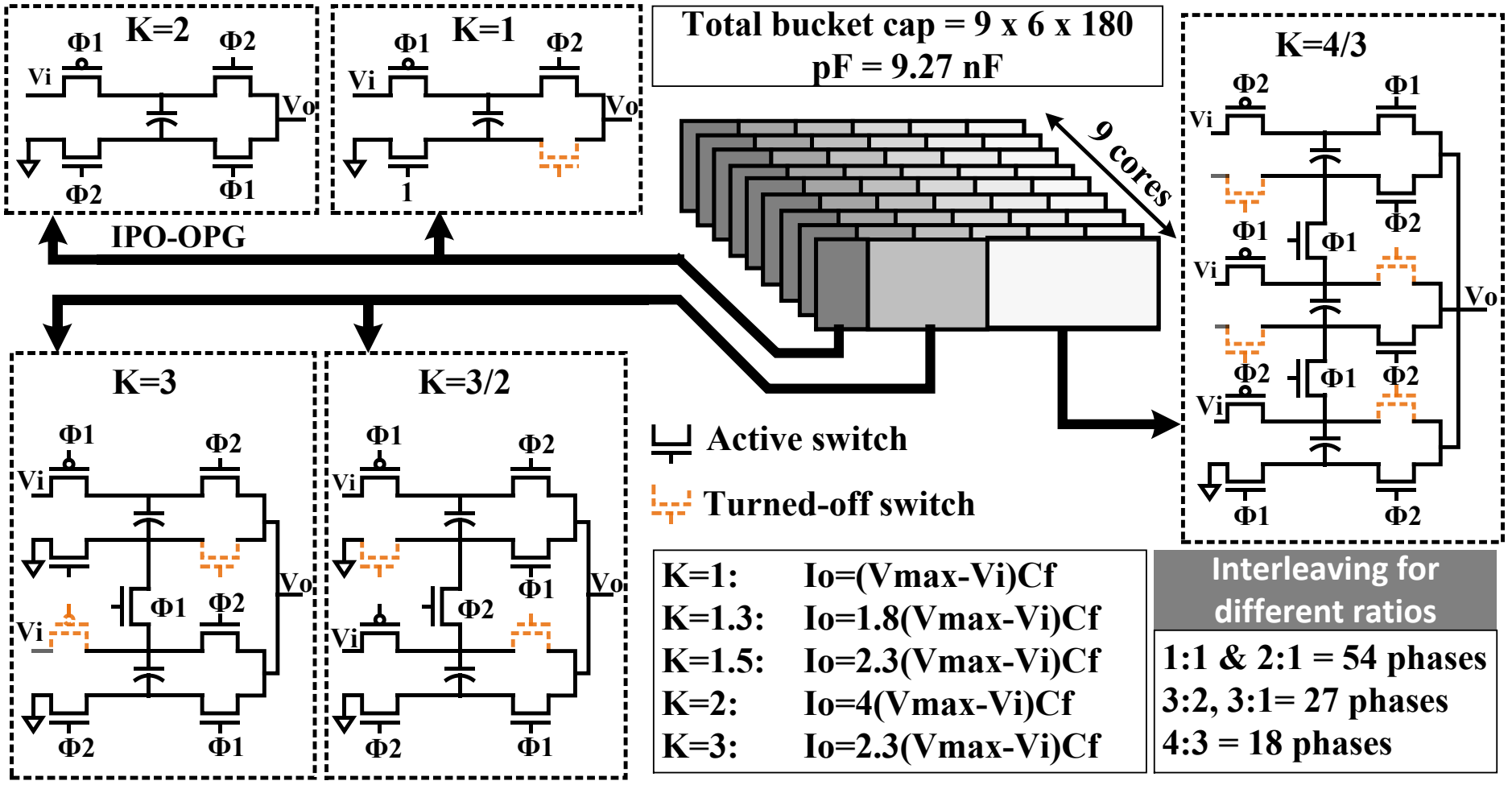
# DC-DC Converter - Open Loop




| | |
|---|---|
| K=1: | Io=(Vmax-Vi)Cf |
| K=1.3: | Io=1.8(Vmax-Vi)Cf |
| K=1.5: | Io=2.3(Vmax-Vi)Cf |
| K=2: | Io=4(Vmax-Vi)Cf |
| K=3: | Io=2.3(Vmax-Vi)Cf |

**Interleaving for different ratios**

1:1 & 2:1 = 54 phases
3:2, 3:1= 27 phases
4:3 = 18 phases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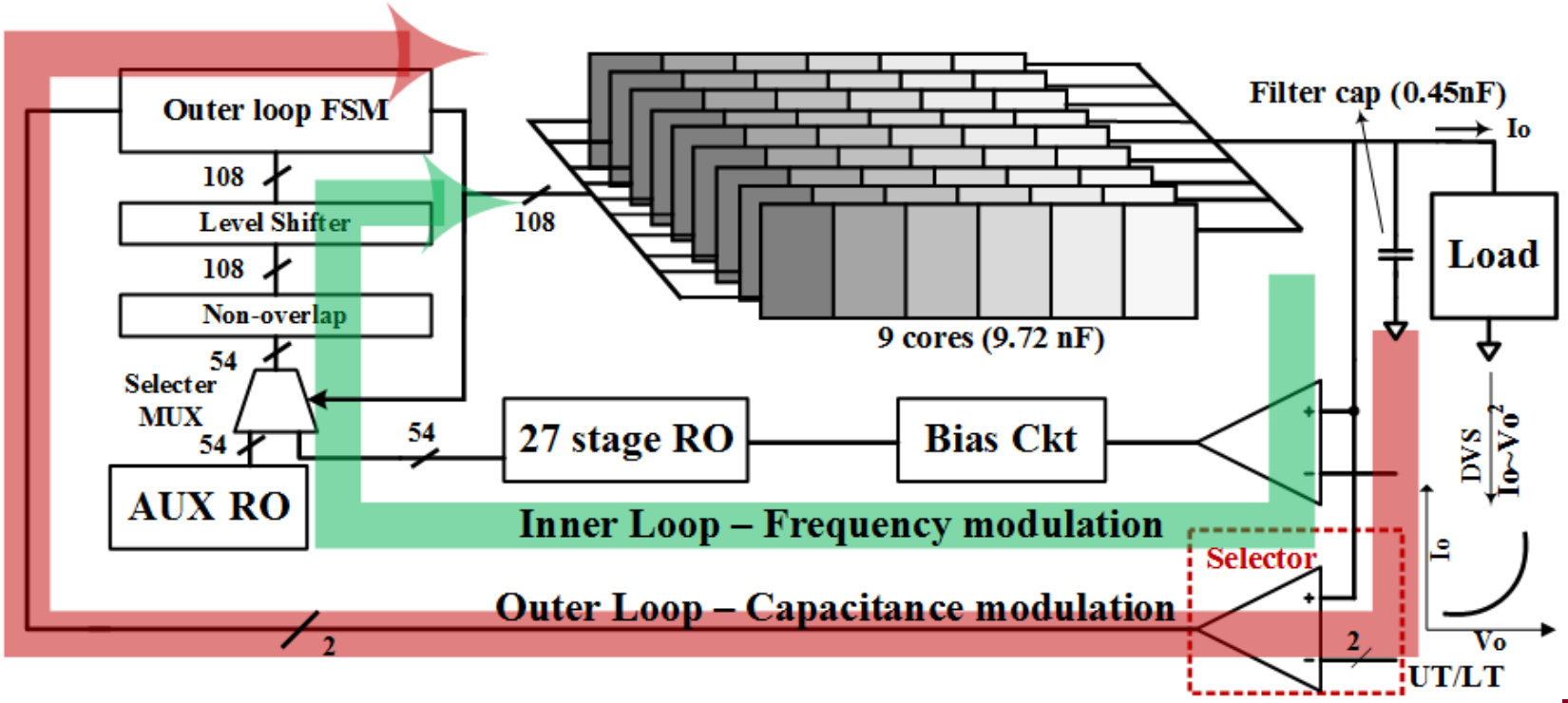
# Architecture

- Modular –digital standard cell based design
  - IPO-OPG cell is standard cell (180pF)
  - 6 cells → 1 core (1.08 nF)
- Dual loop modulation
  - Capacitive modulation (Nine levels) - Outer
  - Frequency modulation (RO based VCO) -Inner





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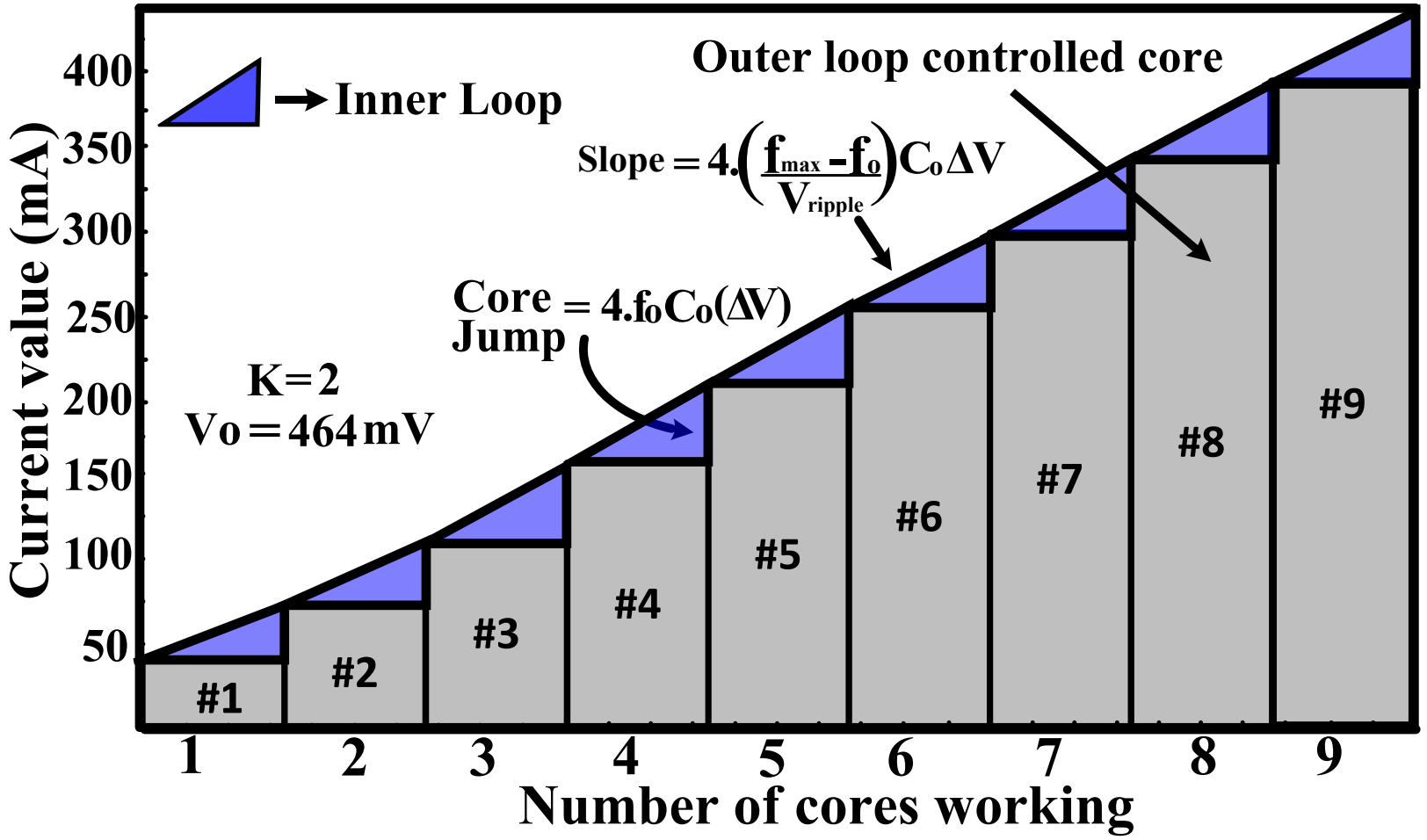
# Outer Control Loop





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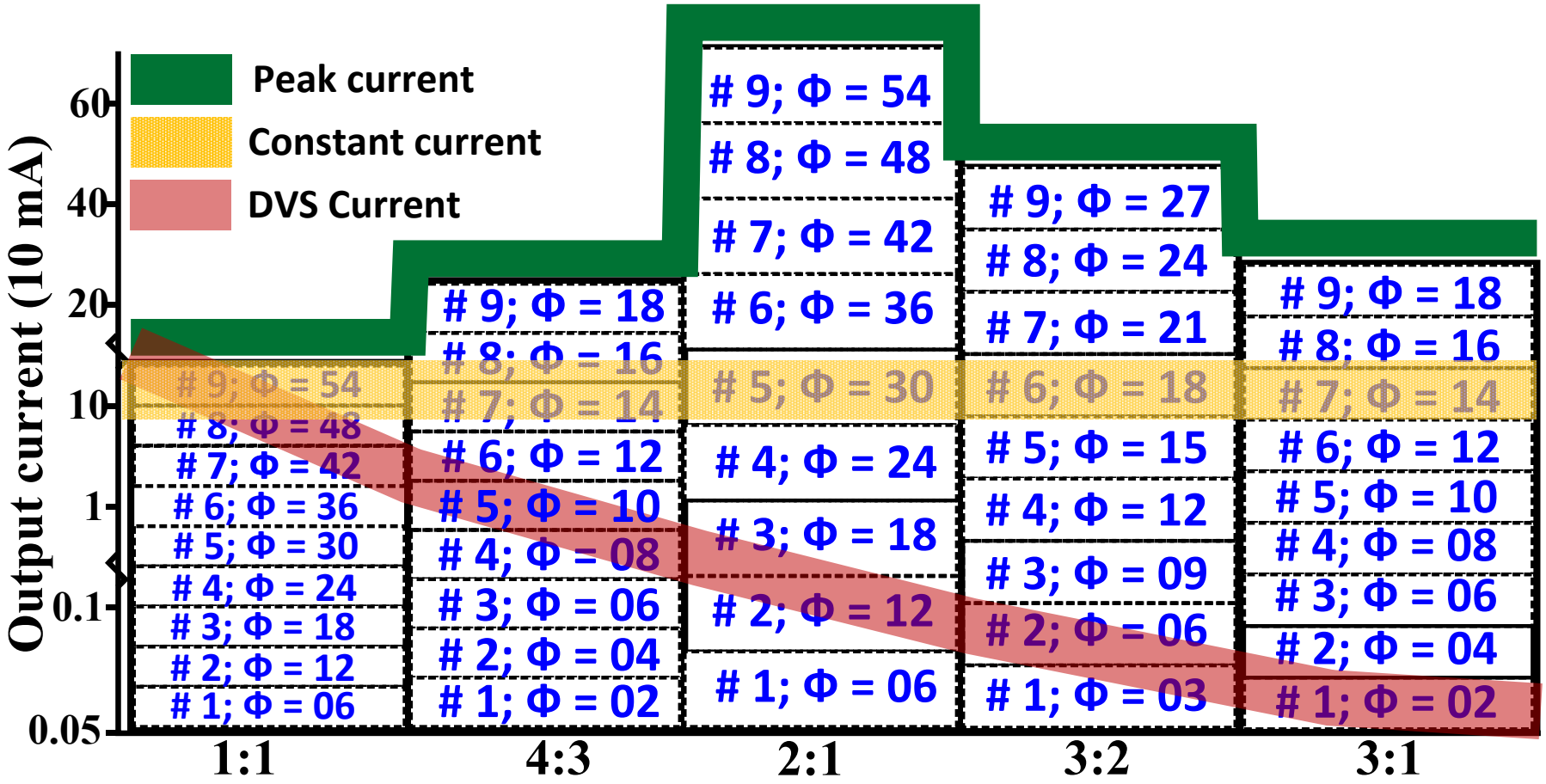
# Overall Converter Dynamics





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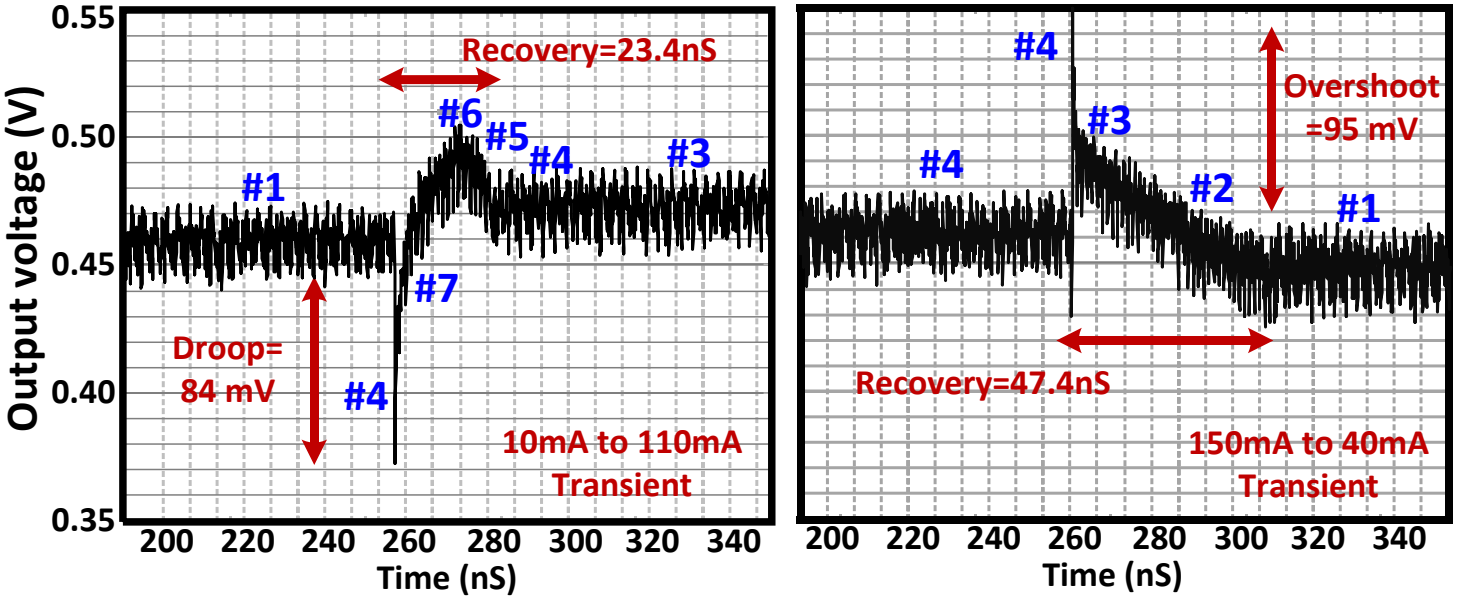
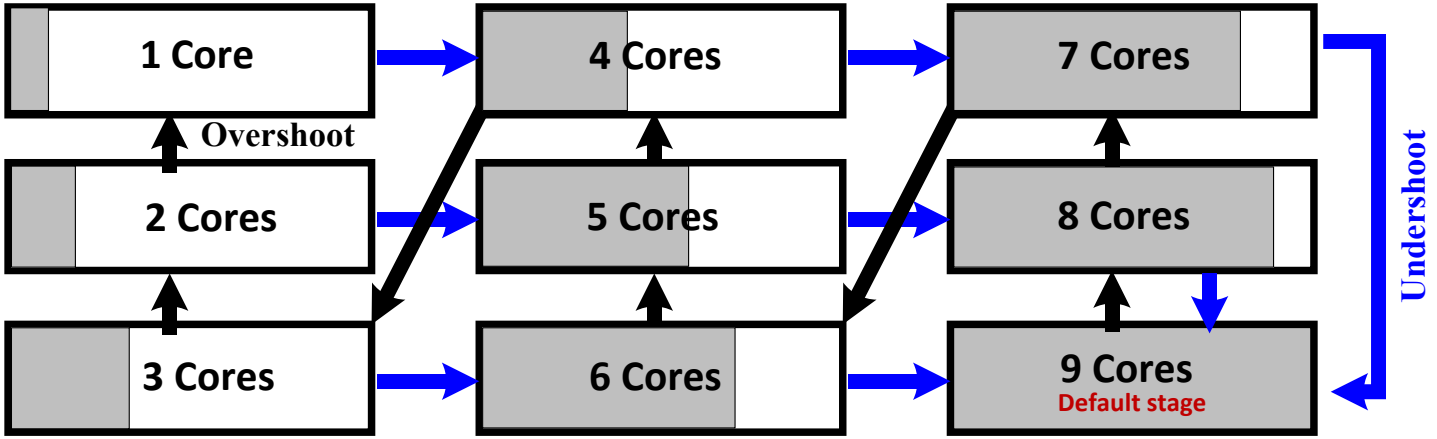
# Measurement Results I





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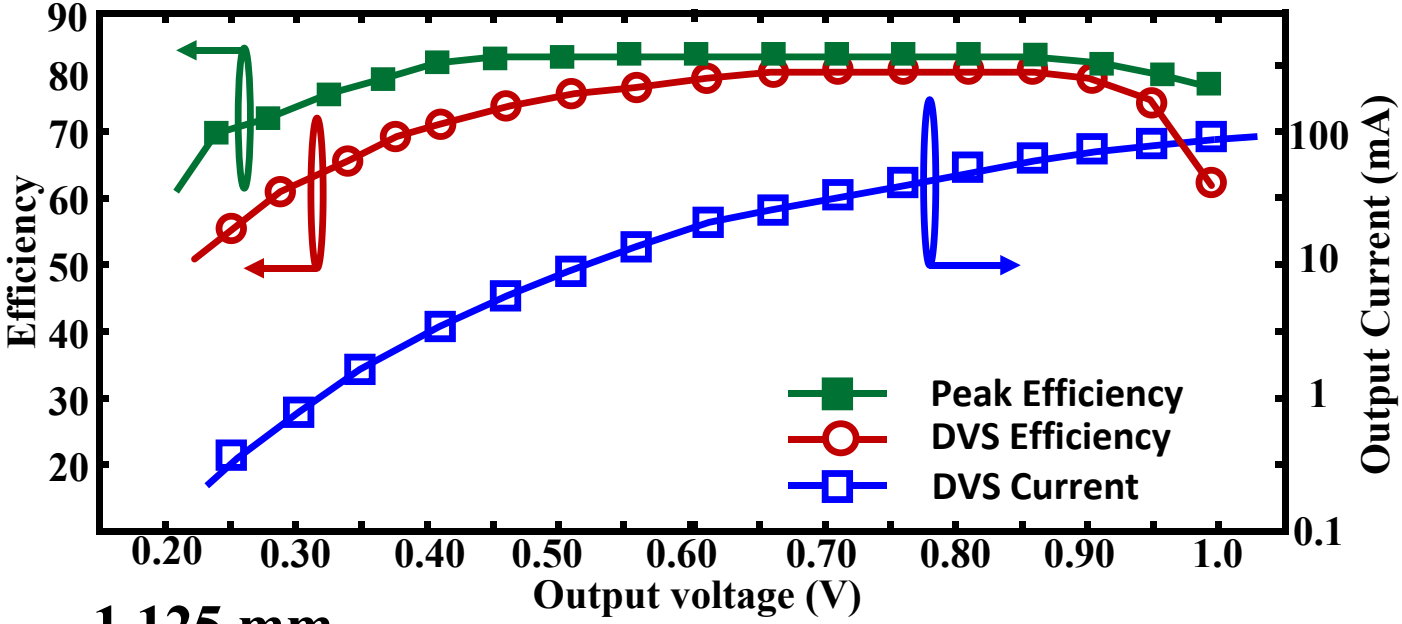
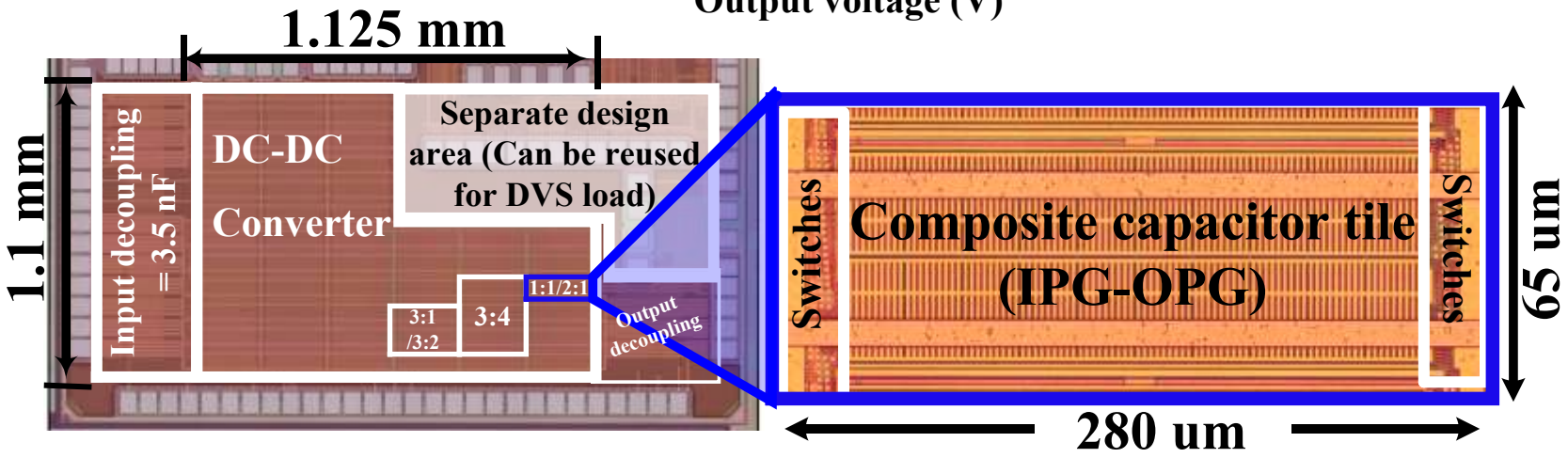
# Combined Efficiency





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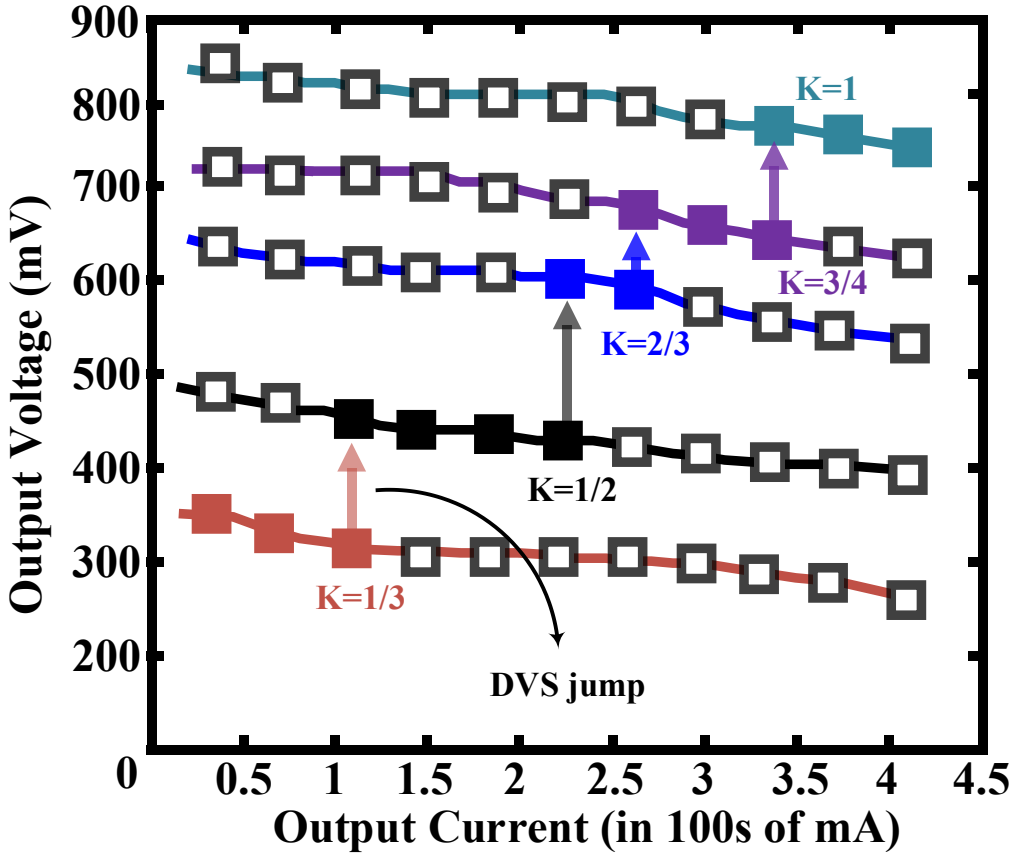
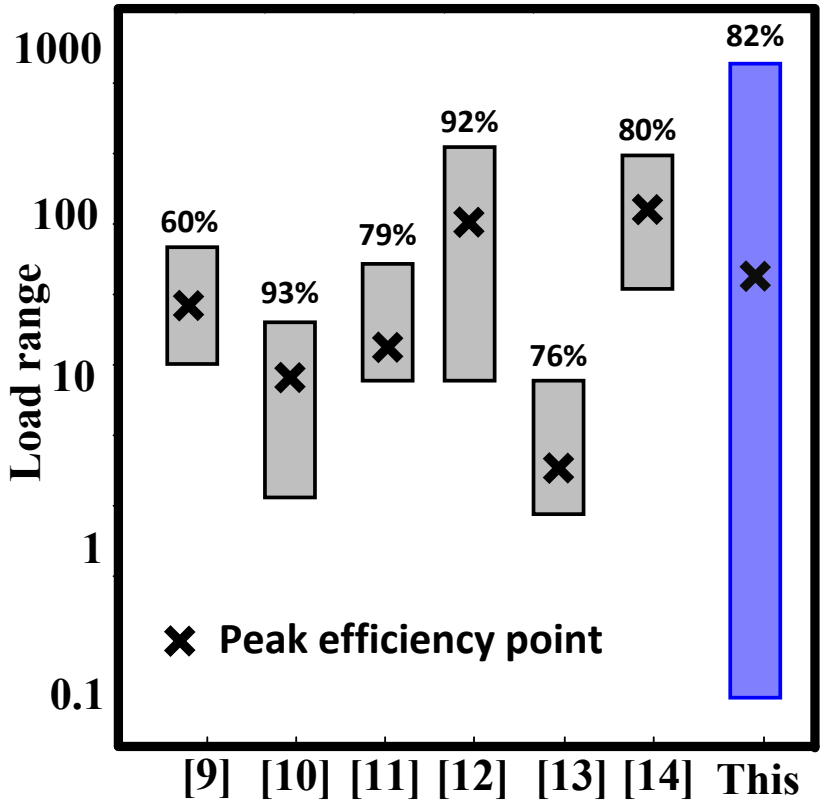
# Comparison

- Widest output current range support
- Supports DVS





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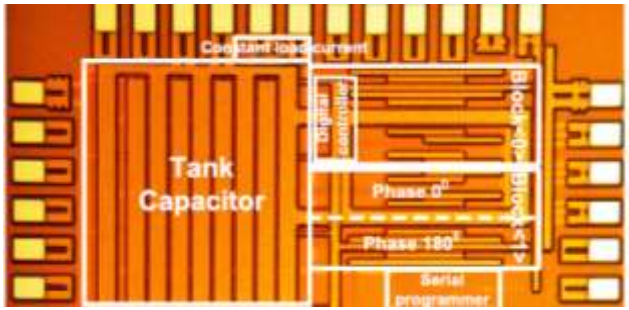
# Fully Integrated Capacitive Converter with All Digital Ripple Mitigation




**Process: IBM 130nm CMOS**
**Sudhir Kudva**
**IEEE CICC 2012, JSSC 2013**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# Ripple Control Techniques(I)

- Overshoot above nominal voltage
  - Results in wasteful power
- Ripple ↓ overall system efficiency ↑
- Conventional techniques
  - Increase switching frequency
  - Increase the interleaved stages
- Losses↑ or area↑ or need high frequency component
- Bucket capacitors designed for maximum load current
- Regulate the amount of charge transferred


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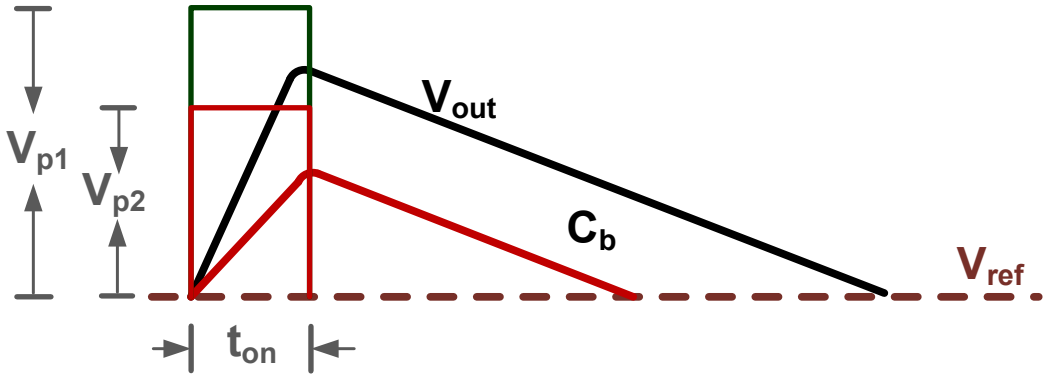
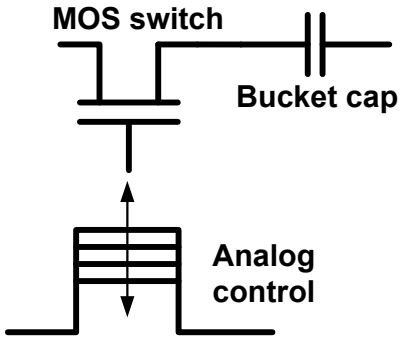
# Ripple Control Techniques (II)

- Regulate the charge dumped into decap
- Unconventional ways to control charge transfer
- Three possible methods
- Switch resistance (method #1)
  - Gate voltage to vary resistance
  - Requires analog components





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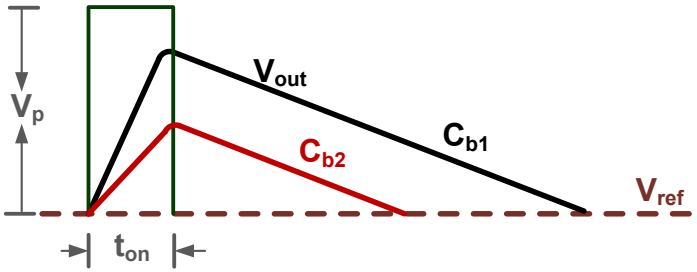
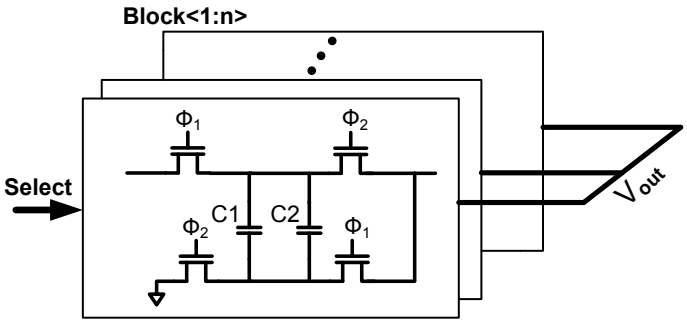
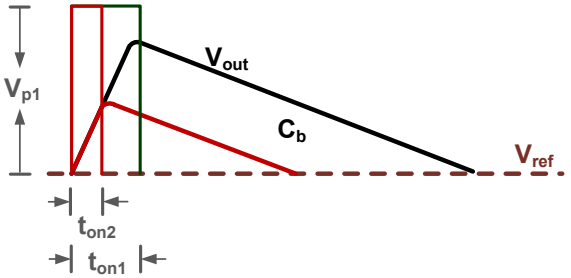
# Ripple Control Techniques (III)

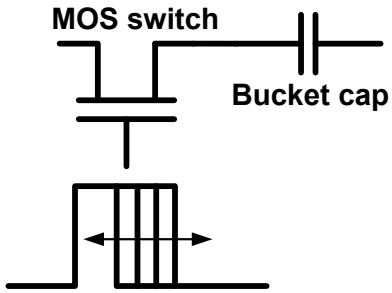
- Capacitance modulation (method #2)
  - Vary bucket cap size
  - Hard to attain fine resolution




- Pulse width modulation (method #3)
  - Vary time of charge/discharge
  - Limited range of control





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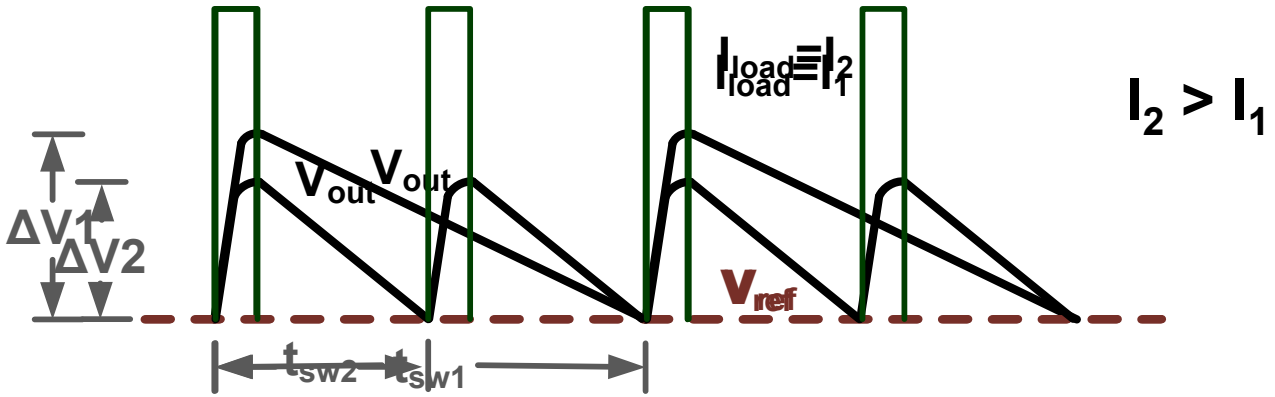
# Cap + Pulse Width Modulation (I)

- Both cap + pulse width modulation digital in nature
  - → No analog components
- Easily scalable with technology
- Primary loop for regulation
  - Changes switching frequency




- Freq used as an indirect measure of ripple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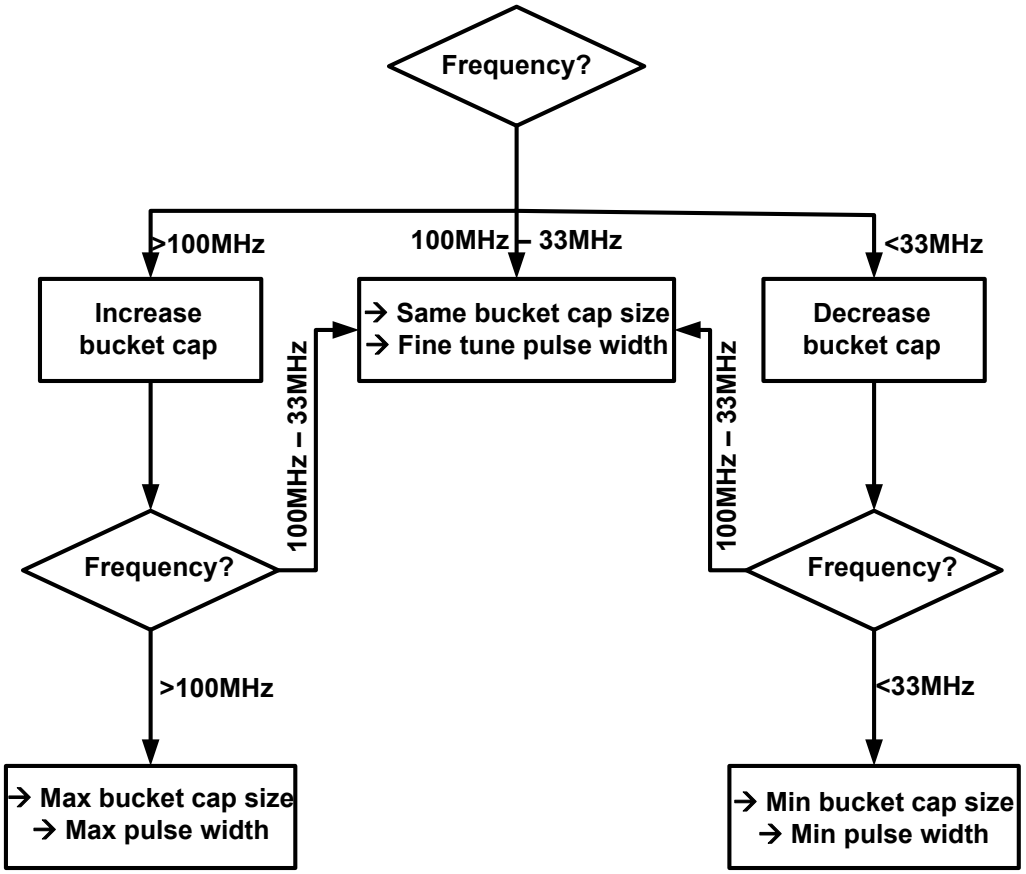
# Cap + Pulse Width Modulation (II)

- Two step control
  - Course control → capacitance modulation
  - Fine control → pulse width modulation




**All digital detection mechanism**

**Easily scalable with technology**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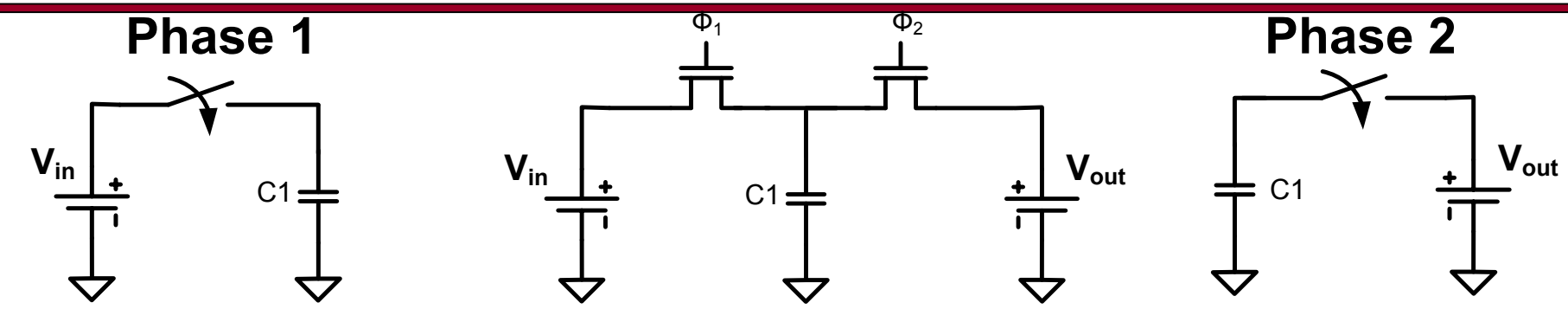
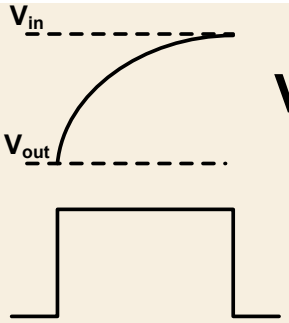
# Partial Charge/Dischage → Efficiency



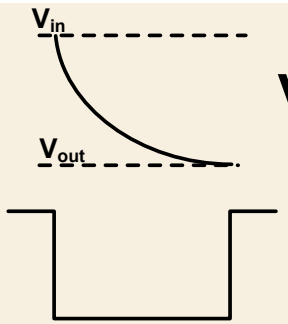

**Complete**



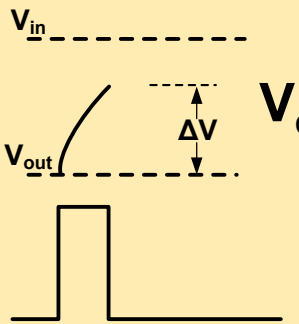

**1:1 converter**

$$\eta_{phase1} = \frac{(V_{in} + V_{out})}{2V_{in}}$$

$$\eta_{phase2} = \frac{2V_{out}}{(V_{in} + V_{out})}$$

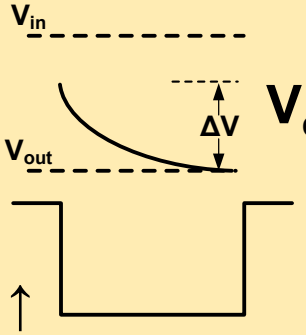



**Partial**




$$\eta_{phase1} = \frac{(\Delta V + 2V_{out})}{2V_{in}}$$

$$\eta_{phase2} = \frac{2V_{out}}{(\Delta V + 2V_{out})}$$




**Phase 1 efficiency ↓** **Phase 2 efficiency ↑**

**Total efficiency ($\eta_{phase1} \times \eta_{phase1} = \frac{Vout}{Vin}$) same**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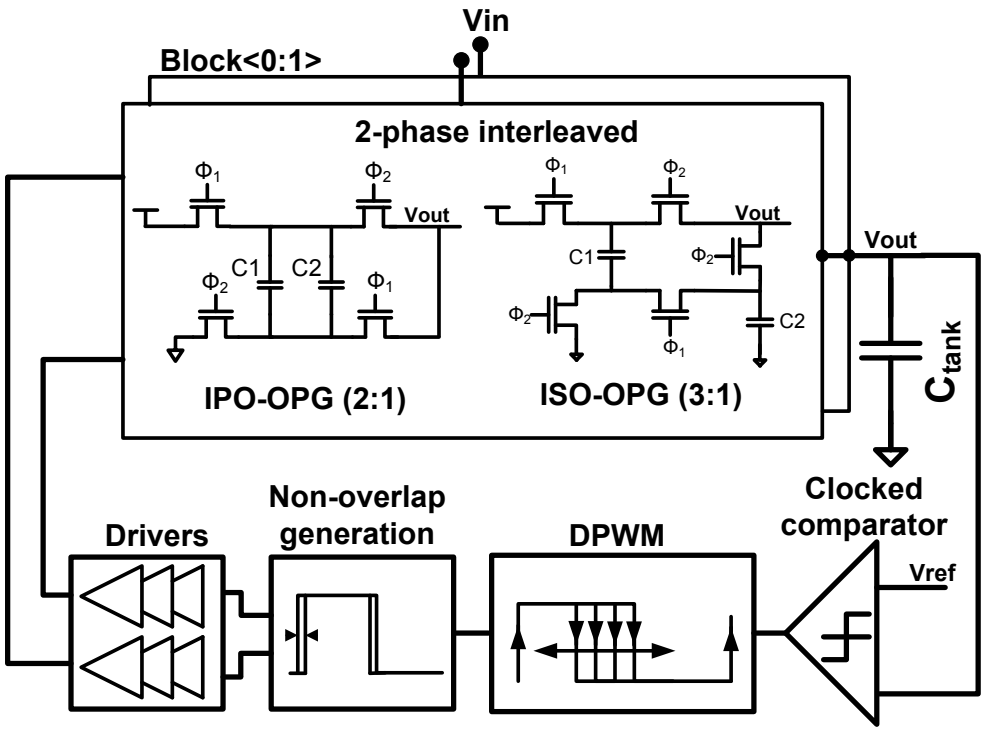
# Regulation




- Single bound hysteretic control → regulation
- Clk freq = 200MHz
- Two copies of the converter core block
- # of blocks operational decided by state machine

- **Converter → 2 phase interleaved**
- **Two modes**
  - **ISO-OPG (3:1)**
  - **IPO-OPG (2:1)**
- **Same bucket caps used in both modes**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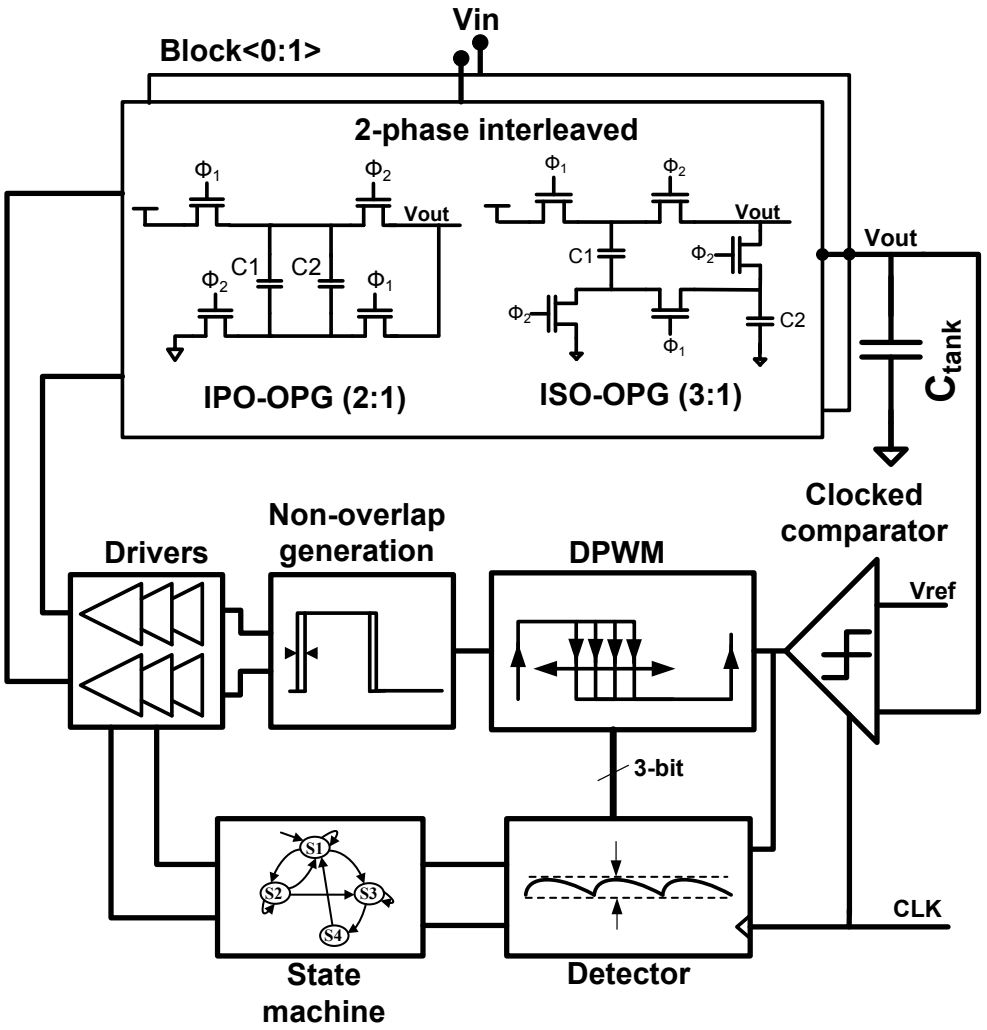
# Fully Integrated Converter




- Input to secondary loop
  - Primary switching frequency
- Capacitance modulation
  - All caps switching
  - Half of caps switching
- Pulse width → 3 bits
- Interaction between primary and secondary loop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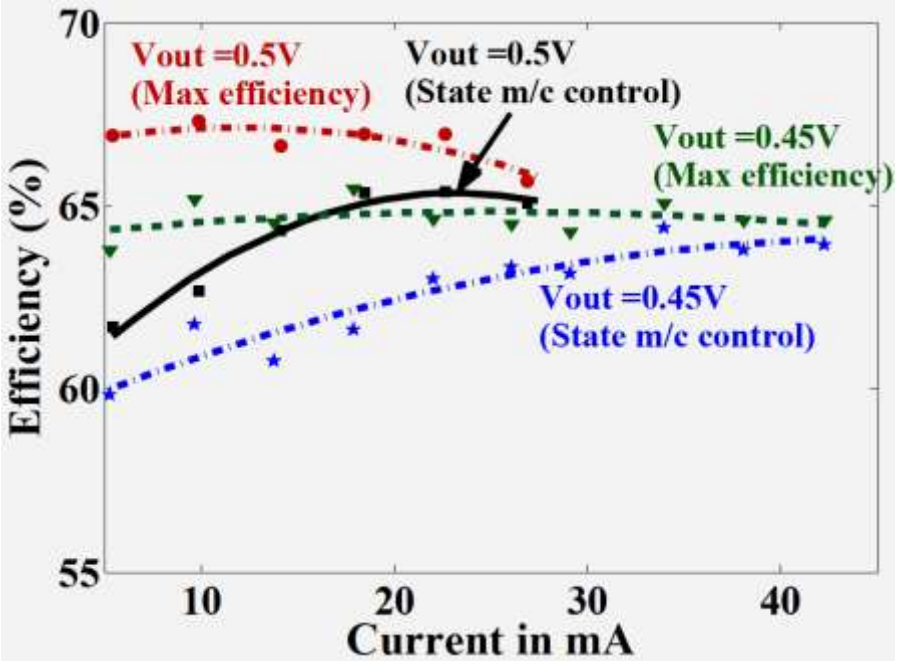
# Measurement Results (I)

- Max efficiency mode → all bucket caps switching
- State machine control
  - Based on ripple selects mode
  - Lower efficiency → higher frequency
  - Less ripple (next slide)
- Experiment
  - Load current varied @ different Vout
  - Manual control (no S/M control)
  - With state machine control





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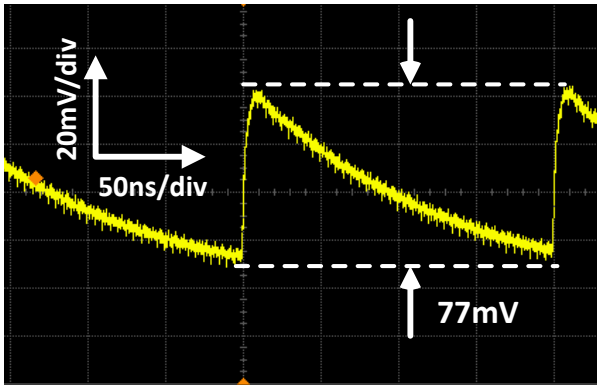
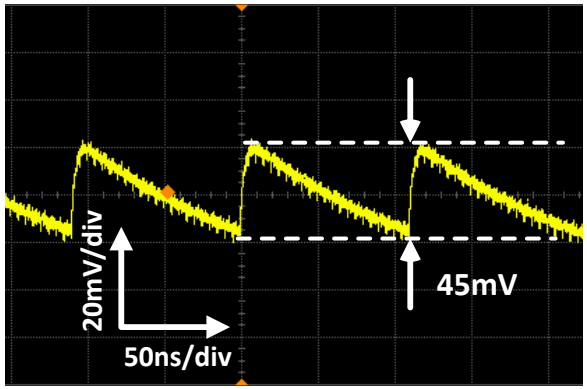
# Measurement Results (V)

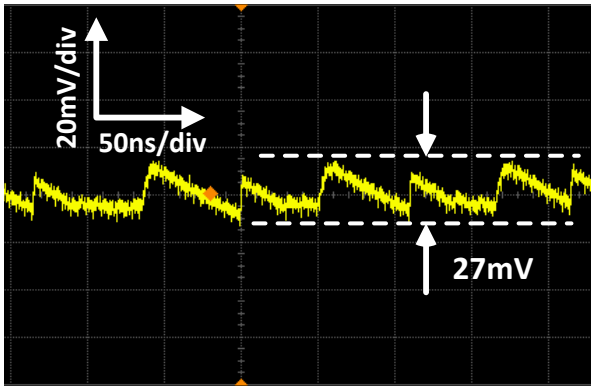
**Full capacitance switching**



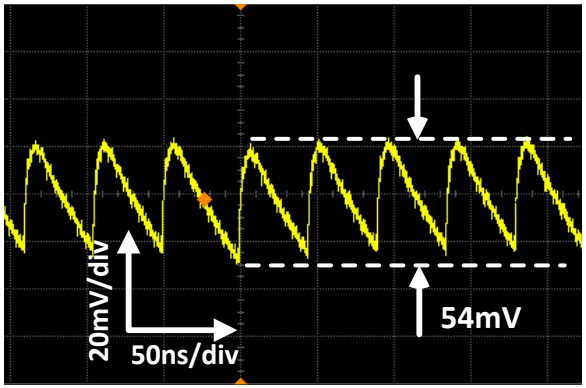

**Capacitance modulation**

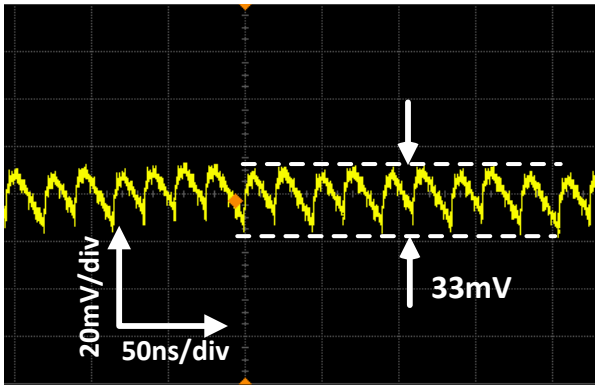


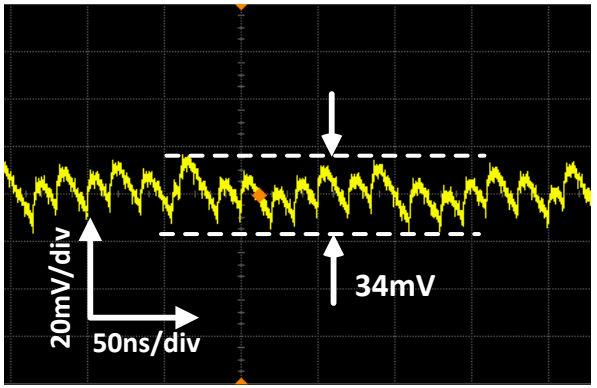

**Capacitance + Pulse width (State m/c control)**




$V_{out}$ = 0.4V $I_{load}$ = 2mA




$V_{out}$ = 0.45V $I_{load}$ = 7.33mA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# Comparison With Prior Work

- Achieves efficiency comparable to designs in lower tech. nodes
- Efficiency expected to increase with technology scaling

| Work | Technology | Design technique | Max efficiency | Comments |
|---|---|---|---|---|
| [Lee07] | 600nm | Resistance modulation | 87% | Off-chip capacitors |
| [Le11] | 32nm | 32-phase interleaved | 80% | Fully integrated |
| [Ramadass10] | 45nm | Capacitance modulation | 69% | Fully integrated |
| **This work** | **130nm** | **Cap + time modulation** | **70%** | **Fully integrated** |


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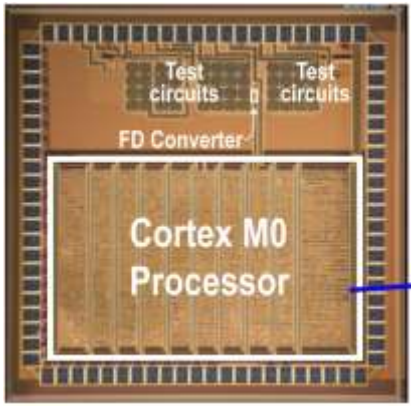
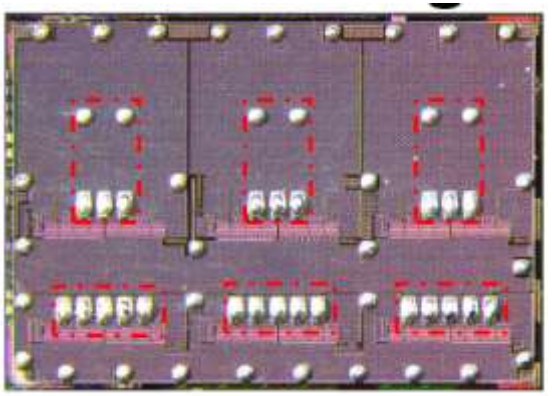
# SPECIAL CAPACITIVE CONVERTERS



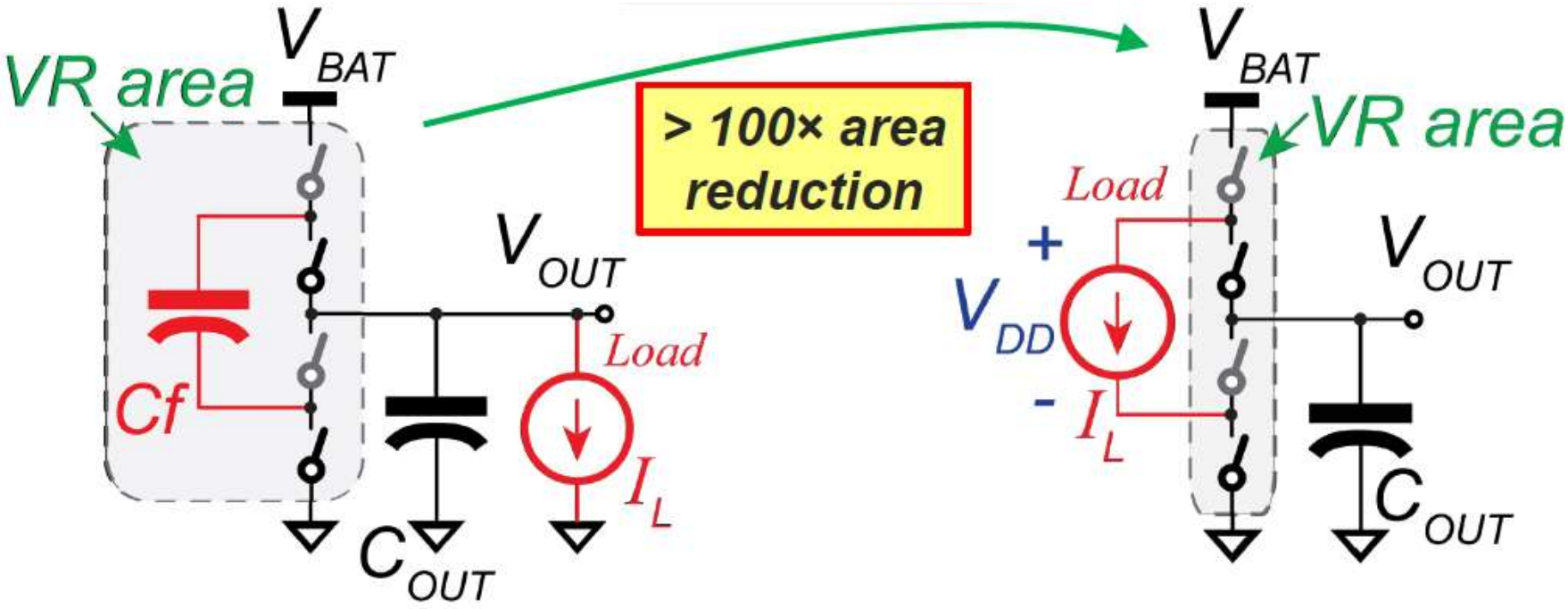

Flying Domain SC DC-DC
Process: 180nm SOI
Loai G. Salem, ISSCC 2016



Resonant SC DC-DC
C. Schaef, ISSCC 2015

# Flying Domain DC-DC Converter

- Flying domain DC-DC converter
- Interchange the bucket capacitor with load
- 100X area reduction, no parasitic loss
- Requires SOI





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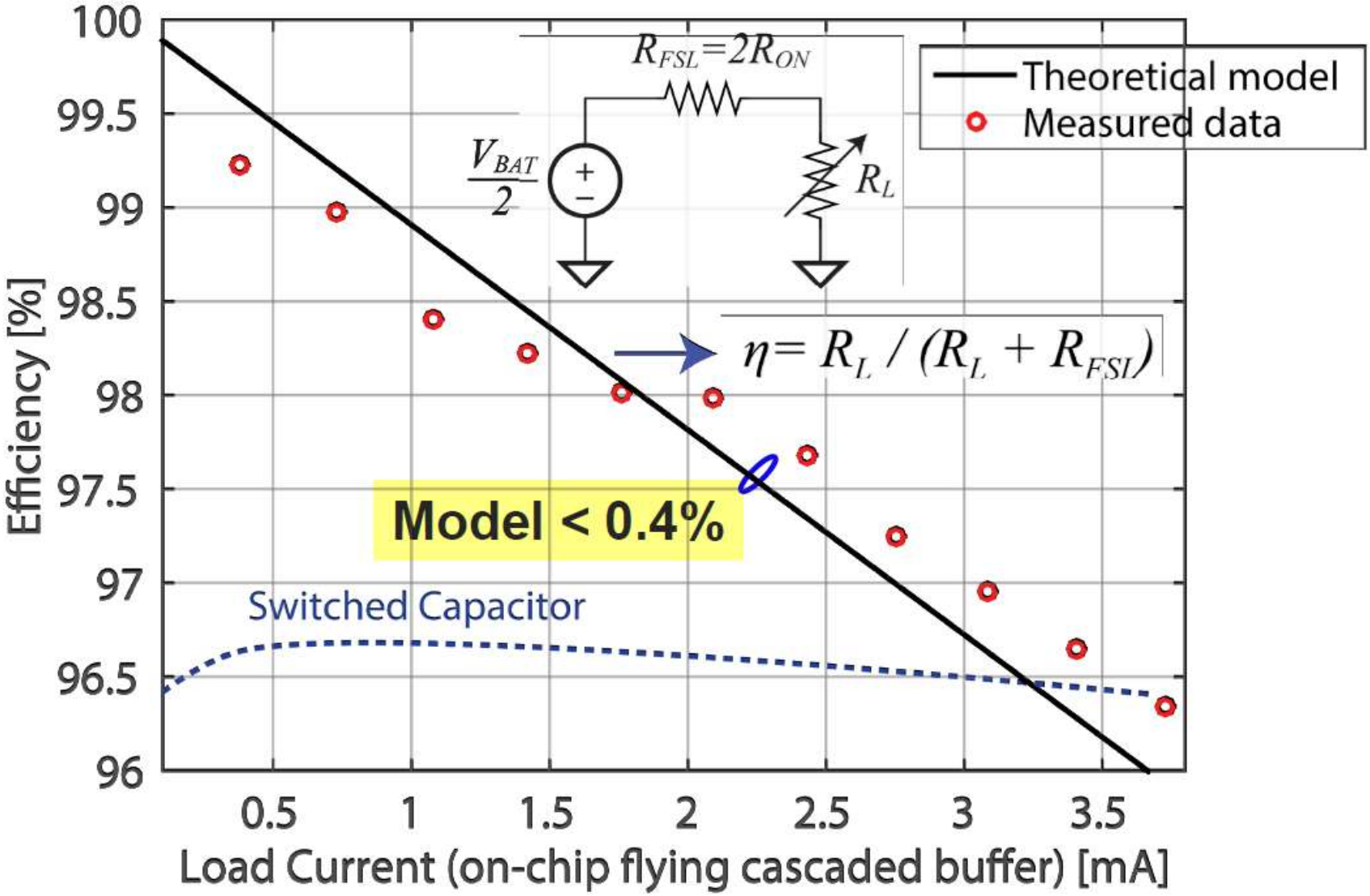
# Efficiency Measurement





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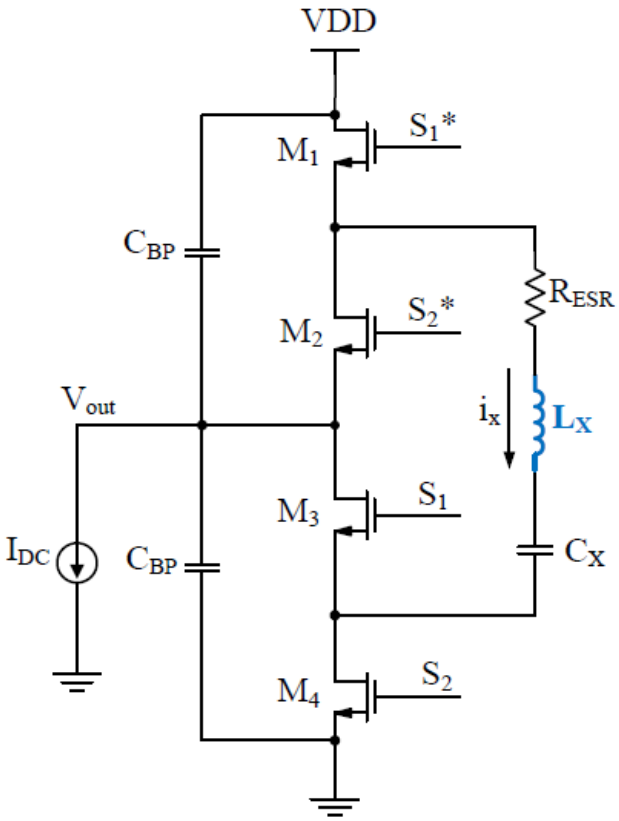
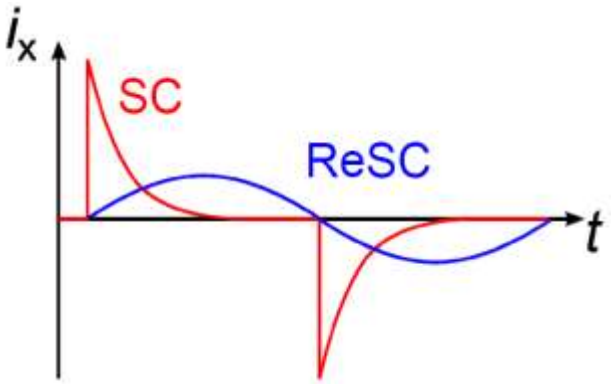
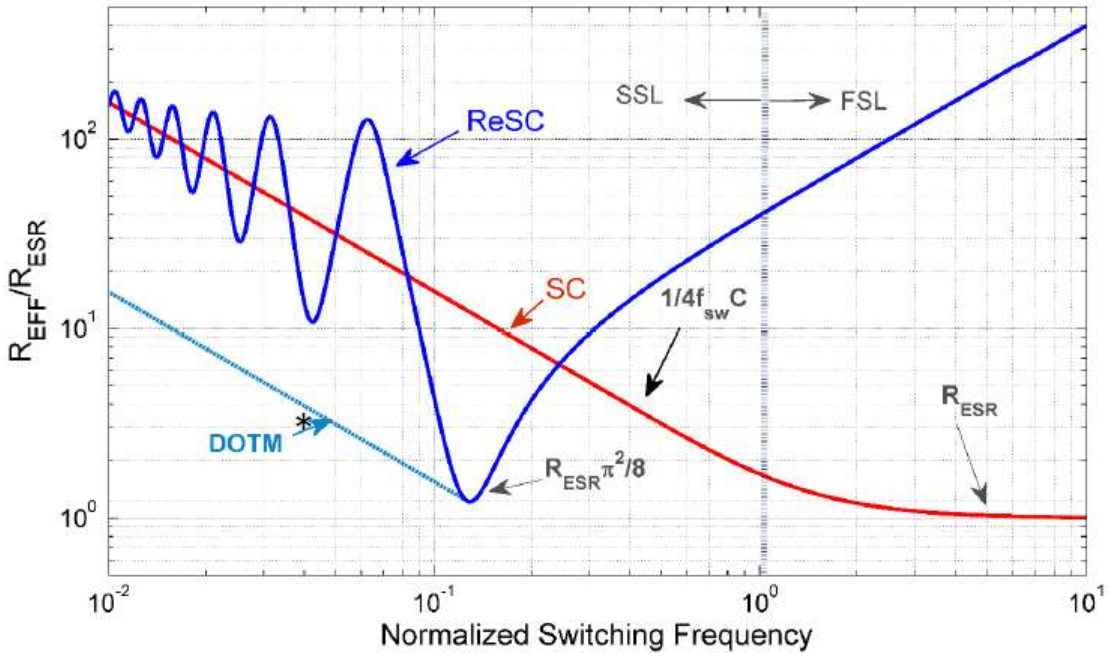
# Resonant Capacitive Converters




2:1 ReSC DC-DC





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# Conclusions

- Linear converters
  - 1:1 conversion ratio, series/shunt
  - Easy to implement
  - LDOs vs DLDOs (for lower supply voltages)
- Inductive converters
  - Theoretical 100% efficiency
  - Integrated inductors are problem. Low quality factor
- Capacitive converters
  - Series parallel design framework
  - Capacitive and frequency based output regulation
- Special capacitive converters
  - Flying domain
  - Resonant converters


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# Questions


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