Low-Power Wideband Analog Channelization Filter Bank Using Passive Polyphase-FFT Techniques

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***Abstract*— Polyphase-FFT (P-FFT) techniques allow for low power implementations of high performance multi-channel filter banks by utilizing computation sharing like a standard fast Fourier transform (FFT). Additionally, it enables a longer "effective window length" than is possible in a standard FFT. This characteristic breaks the trade-off between the main-lobe width and the side-lobe amplitudes in normal finite impulse response filters. Thus, P-FFT techniques have been employed for the channelization of wideband input signals in high speed digital communication receivers. In this paper, we present a prototype analog P-FFT based filter bank in discrete time that is used to channelize wideband input signals so as to reduce the speed and dynamic range requirement of the ADCs. The four-channel I/Q prototype is implemented using TSMC's 65 nm GP technology. Based on passive switches, the design operates at high speed, consumes low power, and offers high linearity performance. The measured transfer function shows >38 dB side-lobe suppression at 1 GS/s operation. The average measured IIP3 is +25 dBm differential power and the total integrated output noise is 208 μV_{rms}. The total power consumption for the P-FFT filter bank (eight-channels total) is 34.6 mW (34.6 pJ/conv).**

***Index Terms*— Analog-FFT (A-FFT), carrier aggregation, channelization receiver, cognitive radio, filter bank, polyphase-FFT (P-FFT), wideband signals.**

I. Introduction

FROM the very start of mobile communications, wireless data traffic volume and the number of applications have increased continuously. This continued increase will eventually necessitate the use of wider signal bandwidths (BWs) by the fundamental constraints imposed by Shannon's theorem. This is already evident with WiFi and LTE where channel banding and carrier aggregation have been deployed. Additionally, the air channel is a common limited resource that is shared by all users and applications, unlike in wired data transfer where each channel can be almost completely isolated. However, while this limited wireless resource has mostly been pre-allocated, the utilization at any given time is often very low [1]. For this environment, cognitive radio and carrier aggregation are potential solutions. Cognitive radio dynamically detects any unused spectrum and exploits it for more efficient spectrum reuse [2]. Carrier aggregation can dynamically adapt the signal BW resources used via both contiguous and non-contiguous aggregation as requirements change [3].

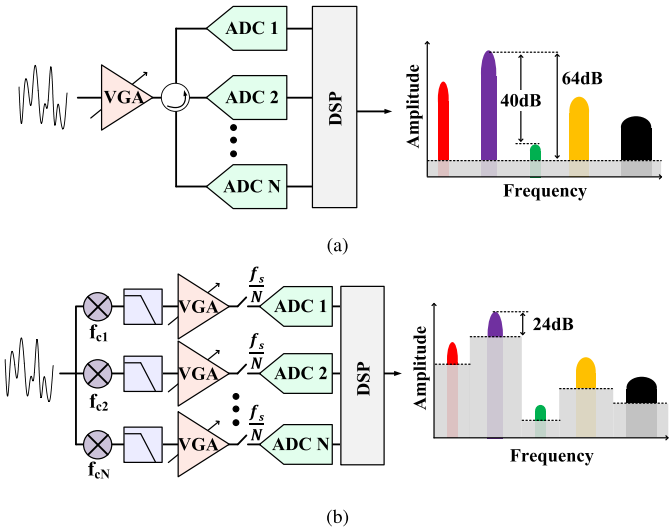

Fig. 1. (a) Time-interleaving ADC and (b) mixer bank based quantizer, and their SNR requirement for a 64 QAM modulated signal in the presence of a 40 dB larger interferer.

Both cognitive radio and carrier aggregation require the processing of wideband signals, which often contain multiple narrowband signals with different center frequencies and amplitudes, unlike the normal focus of conventional narrow band receivers. This in turn makes it necessary to design receivers with a large BW and a high dynamic range [4]. These conflicting requirements typically form the bottleneck for such systems, so significant research has focused on solving these problems.

A single ADC could, in theory, be employed for this system but would require both a wide BW and a large dynamic range due to the large blockers in other channels and the large peak-to-average power ratio resulting in an unrealizable set of ADC specifications [5]. Such ADCs are either not designable or, if possible, they would consume significant power as the advances in ADC speed and resolution have been much slower than Moore's law [6]. Time-interleaved ADCs can mitigate the speed requirement for individual ADCs [7], but the dynamic range requirement for each ADC still remains the same to satisfy the signal-to-noise ratio (SNR) specifications. For example, in the presence of an interferer that is 40 dB larger than the signal, the quantization noise must remain 64 dB below the full signal range for a 64 quadrature amplitude modulation (QAM) LTE signal, as shown in Fig. 1(a).

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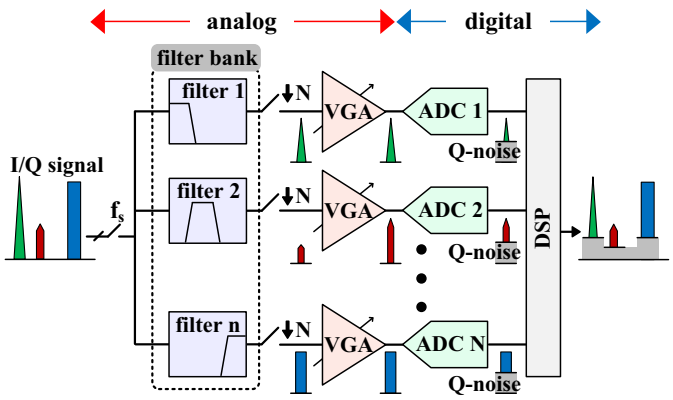


Fig. 2. Filter bank based quantizer.

An alternate method to tackle this problem is to channelize the wideband input signal into separate narrow bands using a mixer bank [8], [9], as shown in Fig. 1(b). In this structure, mixers with different center frequencies combined with low-pass filters are employed for channelization. The variable gain amplifiers that follow the low-pass filters allow for additional gain in the channels that have small amplitudes, which results in a smaller relative quantization error for small signals so that a nearly constant SNR per channel is maintained. Ideally, in this structure, if the channels are sufficiently narrow so that only single carriers are present in each channel, then the individual ADCs require only a 24 dB dynamic range for a 64 QAM modulated signal. This structure solves the dynamic range problem but normally consumes significant power due to the multiple copies of the mixers and the low-pass filters. With advancements in technology, the performance of either structure in Fig. 1 improves, but the operation is not efficient because of the redundant dynamic range and the multiple mixers and filters.

The filter bank based quantizer in Fig. 2 reduces the ADC dynamic range requirement via channelization and filtering out-of-band blockers and signals in other channels in a manner similar to the mixer approach, but it can be designed to be low power. In the mixer-based approach, I/Q mixers are used to down-convert the desired band to zero-IF. However, in the filter bank approach, complex filters with different center frequencies are used to channelize the wideband input signal. In this structure, the mixer bank is replaced with down-sampling to perform the frequency shift to dc, which reduces power consumption. This simple down-sampling is possible due to the prior bandpass filtering, which avoids signal aliasing. However, a naive implementation of the complex filter bank can still be power hungry. In [10], the filter bank was realized using a passive charge-domain radix-2 analog-FFT (A-FFT), which was extremely power efficient due to its zero static power consumption and efficient FFT algorithm. Additionally, FFT channelization allowed for easy reconstruction using an inverse FFT in the digital domain. However, the structure based on the simple rectangular window resulted in only -13 dB side lobes and this limits the out-of-band rejection performance. To mitigate this issue, a windowing-FFT can be employed [11]; however, as is well known for windowing functions, it results in a wider main-lobe width and limits the frequency selectivity [12].

We present a prototype analog discrete-time polyphase-FFT (P-FFT) filter bank design that solves these issues by using passive charge-domain switched capacitors for the channelization of wideband input signals. The proposed method achieves narrower main-lobe width and lower side-lobe amplitudes with low power consumption for multi-channel outputs. It also allows for the reconstruction of the original input signal in the digital domain if necessary [13]. The rest of this paper is organized as follows. Section II explains the operation of a P-FFT filter bank with analytical derivations. Details of the circuit implementation are presented in Section III. Measurement results are provided in Section IV, and some conclusions are provided in Section V.

II. Understanding the Polyphase-FFT Filter Bank

Different forms of polyphase structures have been used for a myriad of applications. In [14], [15], *continuous-time RC* polyphase circuits have been employed to implement complex notch and band-pass filters, i.e., asymmetrical along the $j\omega$ axis, for low-IF receivers. In [16] and [17], multiple discrete-time, i.e., with sample-and-hold values, switched-capacitor low-pass filters use polyphase clocks to realize high-Q bandpass filters. In [18] and [19], mixing-based N-path filters, i.e., with switch time-constants larger than the clock period, using multiple clock phases have been developed to generate high-Q and clock-frequency-tunable bandpass filters at RF frequencies. In both mixing-based and sample-and-hold N-path filters [18], each of the N paths operates at $1/N$th of the overall frequency with resulting aliases but at different phases. The final combination of the N paths cancels out all others, but one aliased signal remains. In all three of these polyphase structures, i.e., continuous-time RC, sample-and-hold N-path, and mixing-based N-path, the focus has been on generating a single frequency output. Additionally, in both N-path filter structures, sample-and-hold N-path and mixing-based N-path, all the N paths are identical with the main focus being on removing aliases. In the P-FFT structure we propose, we also rely on the multiple phase operation to remove aliases; however, our design generates multiple frequency outputs simultaneously and each of the N path transfer functions is not identical. The proposed discrete-time design is also a sample-and-hold design, i.e., there is complete settling during each clock period and the overall design is programmable by a single clock frequency. A number of advantages result from this structure as discussed in the next sections.

A. Window DFT as a Multi-Channel Filter Bank

The filter bank based quantizer in Fig. 2 consists of several copies of a single channel. Each channel has a band-pass filter with different center frequencies and can be implemented using a finite impulse response (FIR) filter where the input signal is convolved with a finite number of window coefficients, as shown in Fig. 3. Here, the length of the window coefficients is N and the center frequency of the band-pass filter is f_s/N. The band-pass filter is constructed from a

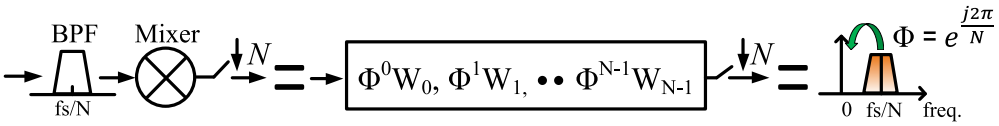


Fig. 3. Bandpass filter and down-conversion.

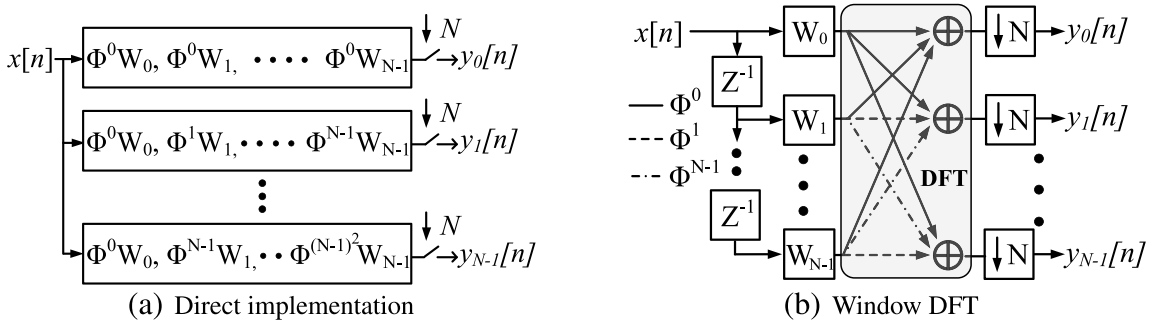


Fig. 4. Filter bank structures. (a) Direct implementation. (b) Window DFT.

frequency-shifted low-pass filter, which is generated by applying a phase rotation in discrete-time domain, as shown by

$$F^{-1}\{X(f-f_0)\} = x(n)\cdot e^{j2\pi\frac{f_0}{f_s}n}. \quad (1)$$

The low-pass filter is defined by the window coefficients in time domain $w[n]$ and its frequency response is given by the following equation, where the frequency is limited from $-f_s/2$ to $f_s/2$ due to the sampling operation:

$$H(f) = \sum_{m=0}^{N-1} w_m e^{-j2\pi\frac{f}{f_s}m} \quad -\frac{f_s}{2} \le f \le \frac{f_s}{2}. \quad (2)$$

A naive implementation of a filter bank based quantizer can be performed by simply using the same coefficients with different phase rotation steps per channel for the equally distributed center frequencies between $-(f_s/2)$ and $(f_s/2)$, as shown in Fig. 4(a). Alternately, a more efficient version can be designed as shown in Fig. 4(b). In this structure, the input signal is successively delayed and then the window coefficients are processed in parallel. The operations of the phase rotation and summation are performed at the end of the system, whereas they were done separately for each channel in the previous one. The phase rotation and summation in Fig. 4(b) is equivalent to the discrete Fourier transform (DFT) and the whole structure is called a window DFT. After the DFT operation, the N outputs are down-sampled by N for a down-conversion to dc. The output of each channel $y_k[n]$ is represented as

$$y_k[n] = \sum_{m=0}^{N-1} w_m \cdot x[Nn+m]e^{-j\frac{2\pi}{N}km}, \quad n \in [-\infty:\infty] \quad (3)$$

where $k \in [0 : N-1]$ is the channel number. This window DFT has been used extensively to process signals in the frequency domain and is efficiently implemented using the FFT algorithm, which provides low complexity and low power consumption through the sharing of computations. However, this structure has a limitation that the number of window

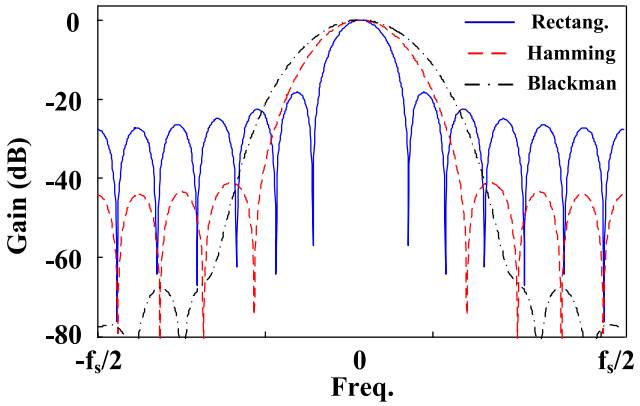


Fig. 5. Comparison of window functions.

coefficients is equal to the number of output channels. For this limited window length, the coefficient values can be traded off between the main-lobe width (frequency selectivity) and side-lobe amplitudes (signal leakage, out-of-band rejection). Fig. 5 compares the impact of different window functions with the same length. The rectangular window has the narrowest main-lobe width but the highest side-lobes. To break this trade-off, the length of the window function needs to be increased, but this is not possible in a standard FFT structure without increasing the number of channels.

B. Constructing a Polyphase-FFT Filter Bank

The P-FFT filter bank has been employed in digital applications because it is computationally efficient [20], can have an arbitrary effective window length, and can break the innate trade-off between selectivity and signal leakage in a standard FFT [21], [22]. In this section, the structure of the P-FFT filter bank for a multi-channel is derived from a simple single channel FIR filter to explain how the polyphase window coefficients and FFT together generate a multi-channel filter bank with different center frequencies.

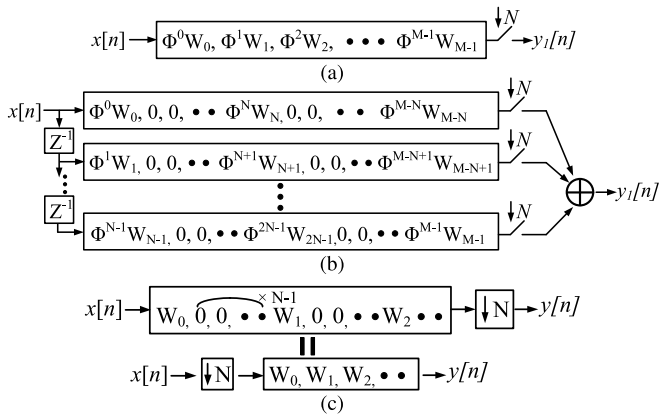


Fig. 6. (a) Frequency-shifted FIR filter with longer window length. (b) Polyphase band pass filter. (c) Noble identity.

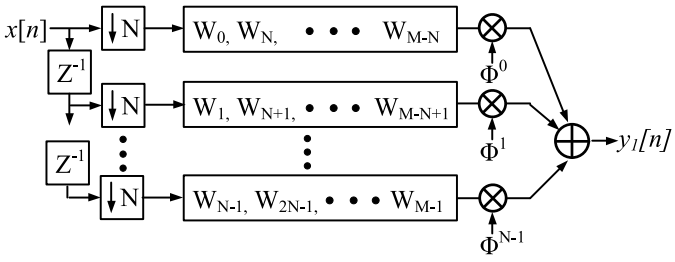


Fig. 7. Polyphase band pass filter after applying noble identity.

Fig. 6(a) shows a frequency-shifted FIR filter where the number of window coefficients M is larger than the down-sampling ratio N. The frequency translated window coefficients can be partitioned into N channels, as shown in Fig. 6(b). Here, in each channel, zeros are inserted and the input signal is successively delayed to compensate for the time offsets. An important property of this structure is that the phase values for the frequency shift in each channel are the same due to the periodicity of ϕ ($\phi^N = 1$). Using this property, the common phase values can be processed by one multiplication step at the end of each channel. The zeros of each channel can also be eliminated by performing the down-sampling operation prior to the window coefficients as shown in Fig. 6(c). This property is known as the noble identity [23], which shows that the replacement generates the same output as shown in (4). Or more precisely, the noble identity states concisely that "The output from a filter H(Z^N) followed by an N-to-1 down sampler is identical to that from an N-to-1 down sampler followed by the filter H(Z)" [21]

$$Y(f) = W(f)\frac{1}{N}\sum_{k=0}^{N-1} X\left(e^{-j\frac{2\pi}{N}k}e^{j\frac{2\pi f}{Nf_s}}\right) - \frac{f_s}{2} \le f \le \frac{f_s}{2}. \quad (4)$$

Then, the structure can be changed to that shown in Fig. 7. In this structure, the center frequency of the FIR filter efficiently changes due to the common phase operation per channel and the operating frequency of each channel is reduced by N. This technique can be applied to other center frequencies of $k \cdot (f_s/N)$, where N is the total number of channels and k is an integer from 0 to $N-1$. Fig. 8 shows the structure that simultaneously generates the N outputs with

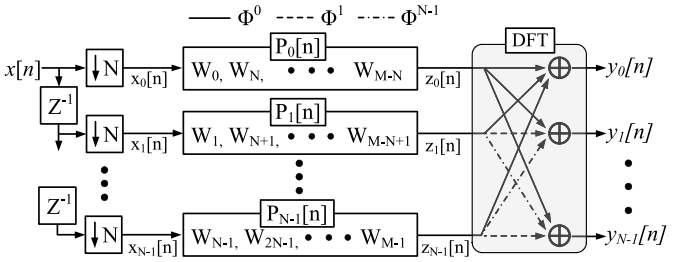


Fig. 8. N-channel P-FFT filter bank.

different center frequencies. In this structure, the outputs of the polyphase window are added together with different phase rotation steps for each output like a window DFT. This overall structure constructed of the polyphase window and the DFT generates a filter bank for multi-channel outputs. This results in an extremely efficient design due to the sharing of the computations like a window DFT, but it can have an arbitrary length for the window coefficients. Additionally, as long as the window function tap weights are symmetrical, it has linear phase within the frequency band of interest like other linear phase FIR filters.

C. Frequency and Phase Responses of the Polyphase-FFT Filter Bank

In Fig. 8, the down-sampled input signals and the window coefficients for each channel ($x_k[n]$ and $p_k[n]$) are convolved together and then the output, $z_k[n]$, can be represented as a multiplication in the frequency domain, as shown in (5). Note that in this equation, the phases of the down-sampled input signals $X_k(f)$ and those of the window coefficients $P_k(f)$ in each channel are opposite, because as the channel number k increases, the input signal is further delayed as we proceed through the window coefficients

$$\begin{aligned} Z_k(f) &= X_k(f) \cdot P_k(f), \quad k \in [0 : N-1] \\ X_k(f) &= \frac{1}{N}\sum_{m=0}^{N-1}\sum_{n=-\infty}^{\infty} x[n]e^{-j\frac{2\pi n}{f_s}\left(f-\frac{mf_s}{N}\right)}e^{j\frac{2\pi}{N}mk} \cdot e^{-j\frac{2\pi fk}{f_s}} \\ P_k(f) &= \frac{1}{N}\sum_{l=0}^{N-1}\sum_{q=-\infty}^{\infty} w[q]e^{-j\frac{2\pi q}{f_s}\left(f-\frac{lf_s}{N}\right)}e^{-j\frac{2\pi}{N}lk} \cdot e^{j\frac{2\pi fk}{f_s}}. \end{aligned} \quad (5)$$

After the polyphase window block, the DFT cancels any non-directional aliased signals. The frequency response of the final DFT output is shown in (6). The equation is identical to the discrete time Fourier transform of the signal, which is the output of a frequency-shifted FIR filter followed by the down-sampling

$$\begin{aligned} Y_k(f) = &\sum_{n=-\infty}^{\infty}\sum_{\tau=-\infty}^{\infty} x[-\tau + nN]w[\tau]e^{j\frac{2\pi}{N}\tau k} \\ &\times e^{-j2\pi\frac{f}{f_s}n} \quad k \in [0 : N-1]. \end{aligned} \quad (6)$$

Fig. 9 shows the frequency and phase responses at each stage of a simple P-FFT. For simplicity, there are four channels and the input signal has four tones, which are placed at

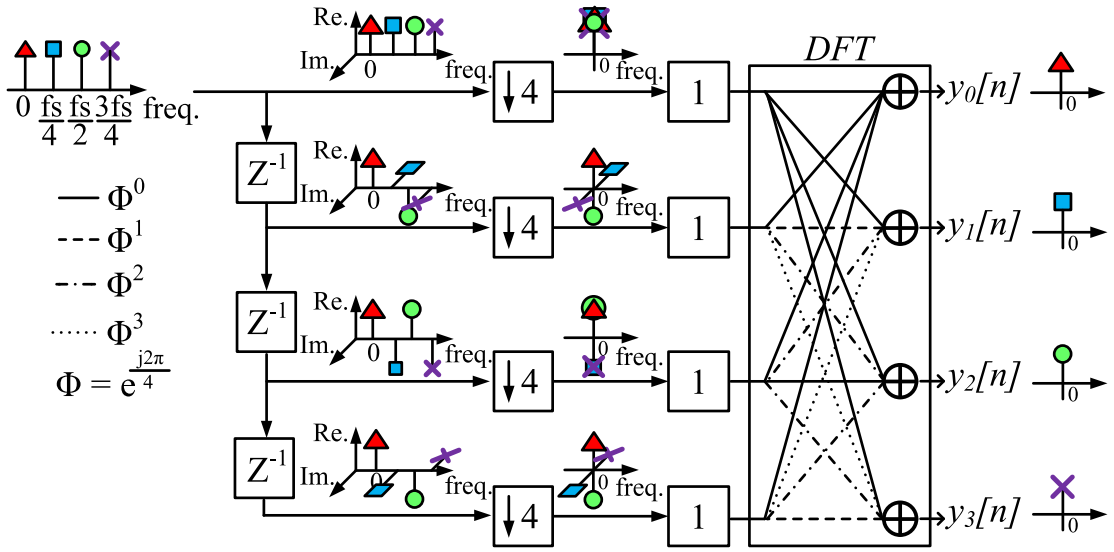


Fig. 9. Frequency and phase responses of the rectangular window P-FFT filter bank.

the center frequency of each channel for clarity. It is also assumed that the window coefficients are all ones (rectangular window) and the total window length is the same as the number of channels, i.e., four. Additionally, at the beginning, it is assumed that the phases of all the tones are aligned at zero. As shown in Fig. 9, after the delay operations, the phases for each of the tones change differently because they are located in the different channels of the input band. For example, after the first delay, the phases for each of the tones at 0, $f_s/4$, $f_s/2$, and $3f_s/4$ change by 0°, −90°, 180°, and 90°, respectively. With this delay operation, the tone at the dc of the input band does not change its phase over the channels, but the phases of the tone at $f_s/4$ becomes 0°, −90°, 180°, and 90° as the channel number increases. After the delay operation, the signals are down-sampled by four and all the four tones are placed at dc. Even though every tone is aliased onto dc, the tones in each channel have different phase relationship, which gives us the opportunity to channelize the tones. For example, if the down-sampled signals from all four rows are added directly with zero phase, then all others are cancelled, but the "red triangle" signal at "0" shows up at the output of the top row $y_0[n]$. Likewise, for the tone at $f_s/4$, the "blue square" is generated at the output of the second row $y_1[n]$, by the down-sampled signal of the 1st row, plus a 90° rotated down-sampled signal of the 2nd row, plus a 180° rotated down-sampled signal of the 3rd row, and plus a −90° rotated down-sampled signal of the fourth row of Fig. 9. The cancellation of any non-directional signals (i.e., signals that have equal magnitude and are equally spaced around the unit circle) is performed by the DFT through the summation process with the different phase rotation steps for each output. This property has been used in other applications such as the multi-channel beamforming receiver [24], [25]. After the DFT operation, only one down-converted tone remains at the output of each channel. We now see that the P-FFT provides an efficient implementation, due to the shared computations, of the filter bank based system shown in Fig. 2.

One of the main advantages of the P-FFT is that it can have an arbitrarily long window length with a more aggressive filtering performance that is virtually independent of the number of channels. To see this effect, we compare the phase responses of the rectangular P-FFT discussed above with a brick-wall P-FFT, i.e., with the extremely long FIR window function in Fig. 10. Also in Fig. 10, there are four channels, but we only use a two-tone input with one of the tones at dc and the other at slightly less than $3f_s/8$, such that it falls in the bin between $f_s/4$ and $f_s/2$. The response of the linear phase brick-wall filter, which is from $-f_s/8$ to $f_s/8$, and the *Sinc* response of the linear phase rectangular filter are both shown at the top of Fig. 10. The constant delay through the two filters is not shown in Fig. 10. After the successive delay in Fig. 8, the phase of the dc tone remains the same, whereas the phase of the tone at $3f_s/8$ rotates by −135° for one delay step, and then it is down-sampled by four and aliased to $f_s/8$, which is shown as $X_k(f)$ in (5) and Fig. 10. After the down-sampling operation, the signal of each channel is processed by the polyphase window. The down-sampled brick wall coefficients have a constant amplitude response over the frequency and change only the phase of the input signal by $e^{j2\pi fk/f_s}$, as shown in the $P_k(f)$ of (5). This phase term cancels the frequency-dependent phase variation of the delayed and down-sampled input signal, $e^{-j2\pi fk/f_s}$ in the $X_k(f)$. With this effect, the phase of the tone at $f_s/8$ rotates by 45° per channel number, k, and the result is shown in the third row of Fig. 10, $Z_k(f)$. The final outputs of the rectangular and the brick-wall P-FFTs are shown together in the second to the last row of Fig. 10, i.e., "After DFT, $Y_k(n)$. "They are the DFTs of $X_k(f)$ and $Z_k(f)$, respectively. The brick-wall and rectangular window based P-FFT operations are shown in the last row of Fig. 10. The results for the rectangular window based P-FFT are drawn with dotted lines, while those for the brick-wall are drawn with solid bold lines. In both cases of the rectangular and brick-wall coefficients, the dc tone remains only at Ch.0, but the tone that is slightly less than $3f_s/8$ shows

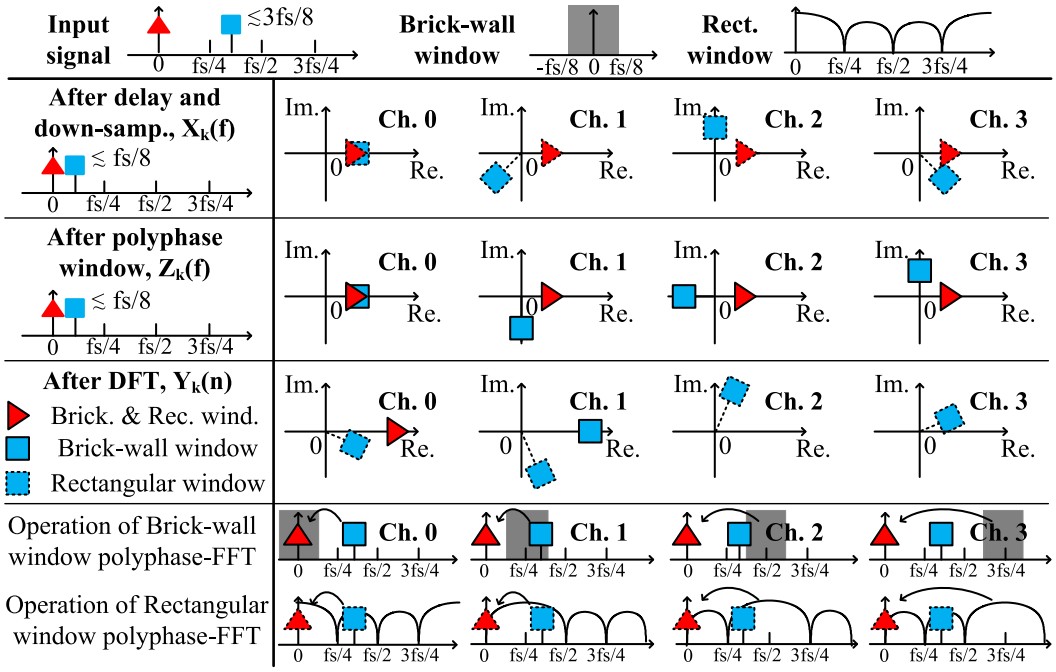


Fig. 10. Phase responses of rectangular and brick-wall window P-FFTs.

up at all channels for the rectangular window but it appears only at Ch.1 for the brick-wall case. This is the property that we wish to exploit in the P-FFT design using longer window coefficients.

D. Complexity Comparison

The main advantage of an FFT implementation over the direct implementation of the DFT is that the complexity is reduced through computation sharing. In the case of N channel outputs, a radix-2 structure reduces the complexity from $O(N^2)$ to $O(Nlog_2N)$ [26]. However, as discussed in the previous section, traditional FFT structures can use a window length that is limited to the number of channels [12]. In [10], an 8-tap rectangular window, and in [11], a 64-Hamming window was employed for 8 channels and 64 channels, respectively. In other words, to achieve the filtering performance of the P-FFT with an arbitrary window length, the number of channels and the complexity of the traditional FFT would inevitably need to increase. Using the structures in Fig. 4, the filter bank can be designed as in Fig. 8, where the length of window coefficients M is larger than the number of channels N. In the case of direct implementation, one channel consists of M coefficients so that the complexity of the total N channel is $O(NM)$. In a traditional window FFT, the total M channels would have to be implemented to achieve the equivalent filter performance, so the complexity is $O(M\log_2 M)$. Fig. 11 compares the complexities of different structures. Here, the complexity of the P-FFT filter bank was calculated as $O(M + N\log_2 N)$ considering the polyphase window block. In the result, the proposed structure shows the lowest complexity for every channel length. In particular, for 16 channels and a window length of 64, the P-FFT complexity

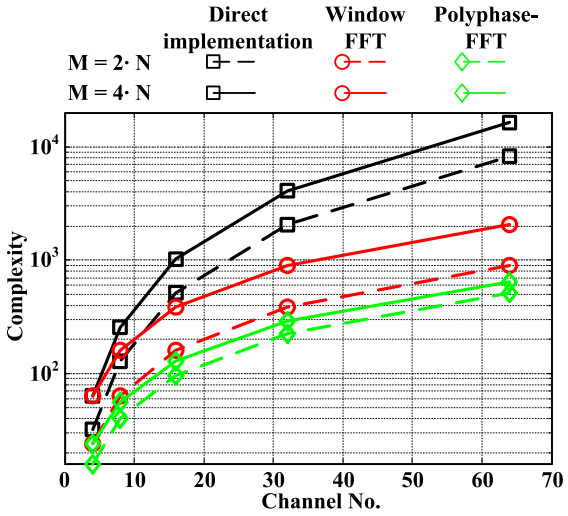


Fig. 11. Comparison of complexities for different structures.

is 3 times smaller than for a traditional window FFT. The savings increase as the number of channels increases.

III. Prototype Circuit Implementation

For the prototype implementation, we used 13-tap window coefficients ($w[n]$ = [1, 4, 10, 19, 29, 37, 40, 37, 29, 19, 10, 4, 1]). The coefficients were generated by a convolution of a 10-tap, 5-bit resolution Chebyshev filter ($w_1[n]$ = [1, 3, 6, 9, 11, 11, 9, 6, 3, 1]) and a 4-tap rectangular window ($w_2[n]$ = [1, 1, 1, 1]). These window coefficients were adopted considering the trade-off between the main-lobe width and the complexity. With a longer window coefficient length, a narrower main-lobe width and a better channel selectivity are achieved, but it requires more circuit

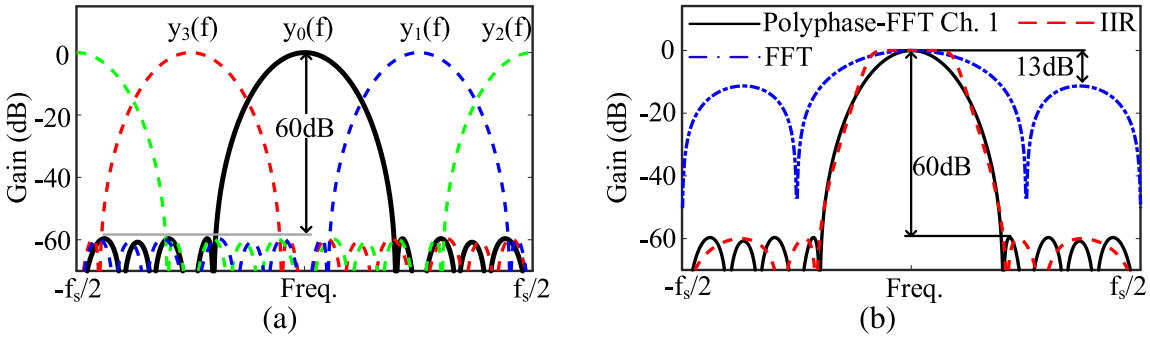


Fig. 12. (a) Frequency response of the P-FFT filter bank. (b) Comparison of frequency responses.

complexity and longer sampling phases. Fig. 12(a) shows the simulated resulting four outputs that are equally spaced from $-f_s/2$ to $f_s/2$. In Fig. 12(a), the center frequency of the third channel $y_3(f)$ is $-f_s/4$, because the frequency response at $3f_s/4$ in continuous-time domain is aliased to $-f_s/4$ in discrete-time domain. We note that there is an overlap in the frequency bands. This is a necessary condition if we are interested in reconstructing the full wideband signal in the digital domain. Fig. 12(b) shows a comparison with two other filter responses (a standard FFT with a four-tap rectangular window and a fifth order IIR Chebyshev II filter). As can be seen, the side-lobes of the P-FFT filter bank are -60 dB, like those of the fifth order IIR Chebyshev II filter, while the side-lobes of a standard FFT are only -13 dB. We also note that the main-lobe width is narrower than that of a standard FFT. Compared with the fifth order IIR filter, a P-FFT has the advantages of linear phase due to the FIR characteristic, easy extendibility to multi-channels using the FFT algorithm, the ability to easily reconstruct the original signal, and the potential ability to operate at higher switching frequencies since there is no feedback around the loop.

Using the window coefficients, a prototype analog four-channel-I/Q P-FFT filter bank was designed with passive switched capacitor circuits. The filter implementation through a charge sharing scheme [5], [27], [28] enables high speed and low power operation. Fig. 13(a) shows a detailed schematic for the analog polyphase window summation process. The related clock sequences are shown in Fig. 13(b), where non-overlapping clock signals are used for Θ_{p2}, Θ_{F1}, and Θ_{F2} to avoid unexpected charge sharing between capacitors. The pre-layout simulation shows that a 10% overlap between clock signals deteriorates the side-lobe performance by 30 dB. In the polyphase summation block, I/Q input signals are sampled on a set of different 9 fF unit capacitors during 13 sampling clock phases (e.g., 10 unit capacitors at Θ_{S2}). The number of unit capacitors during each sampling phase corresponds to the window coefficients, $w[n]$. After the sampling phases, the sampled values are shared for the polyphase window summation during Θ_{P1} and Θ_{P2}. Due to the different number of sampling capacitors, the window coefficients are implemented after the sharing operation. The standard A-FFT in the next stage requires 2 copies of each input for the butterfly operation, so the 60 shared capacitors for each path [see 1, 29, 29, 1 capacitors in the top slice of Fig. 13(a)] are separated into two halves after the falling edge of Θ_{P2}. The output of the polyphase window summation in each channel consists of 8 pairs (2 copies of $\pm I$, $\pm Q$) of capacitors, where each capacitor is composed of 30 "unit capacitors" with a total value of 270 fF.

The polyphase window summation outputs $Z_k[n]$, where $k \in [0{:}3]$, are connected to the input of the A-FFT as shown in Fig. 14. The A-FFT, which is implemented in a radix-2 structure, works for four phases (Θ_{RST}, Θ_{F1}, Θ_{F2}, and Θ_M). During Θ_{RST} (i.e., the input signal sampling phase in the polyphase window summation block), the input capacitances of the A-FFT in Fig. 14, C_{FFT}, are reset to VCM to eliminate any history effects. During the Θ_{F1} and Θ_{F2} phases, the FFT processes the input signals with addition, negation, and "multiply by $-j$" operations. Then, at the next phase, Θ_M, one output among the four channels is selected using the output MUX and connected to the output buffer for testing purposes. The required operations for the A-FFT are implemented with charge sharing for addition and swapping of signal lines for negation and "multiply by $-j$" operations, which guarantee a low power and high speed operation. In addition, the butterfly blocks in an A-FFT are designed with the RCX technique to mitigate the effect of a settling error, as shown in Fig. 15 [28]. For the entire structure, a total of 960 unit capacitors and sampling switches are used for the differential I/Q signals. Other switches for the sharing operation were implemented in CMOS with the same NMOS and PMOS size to reduce the clock feedthrough effect and to increase the signal range. The switch size during the Θ_{p1} phase is 270 nm/65 nm and other switches for Θ_{p2} phase and FFT were designed with larger size, 6.5 um/65 nm, to reduce the switch resistance and settling error. Even though the number of channels in this prototype design is limited to four, it can easily be extended to additional channels (i.e., 8, 16, or 32) at the cost of some increased complexity. For example, if we extend the 4 channels, where we have 2 processing stages and 4 multiplication coefficients in the radix-2 FFT structure, to 16 channels, then the number of processing stages would increase to 4 with 16 multiplication coefficients [28].

The schematics for the output MUX and buffer that were used only for testing purposes are shown in Fig. 16. In the output MUX, a total of 32 CMOS switches are used to sense

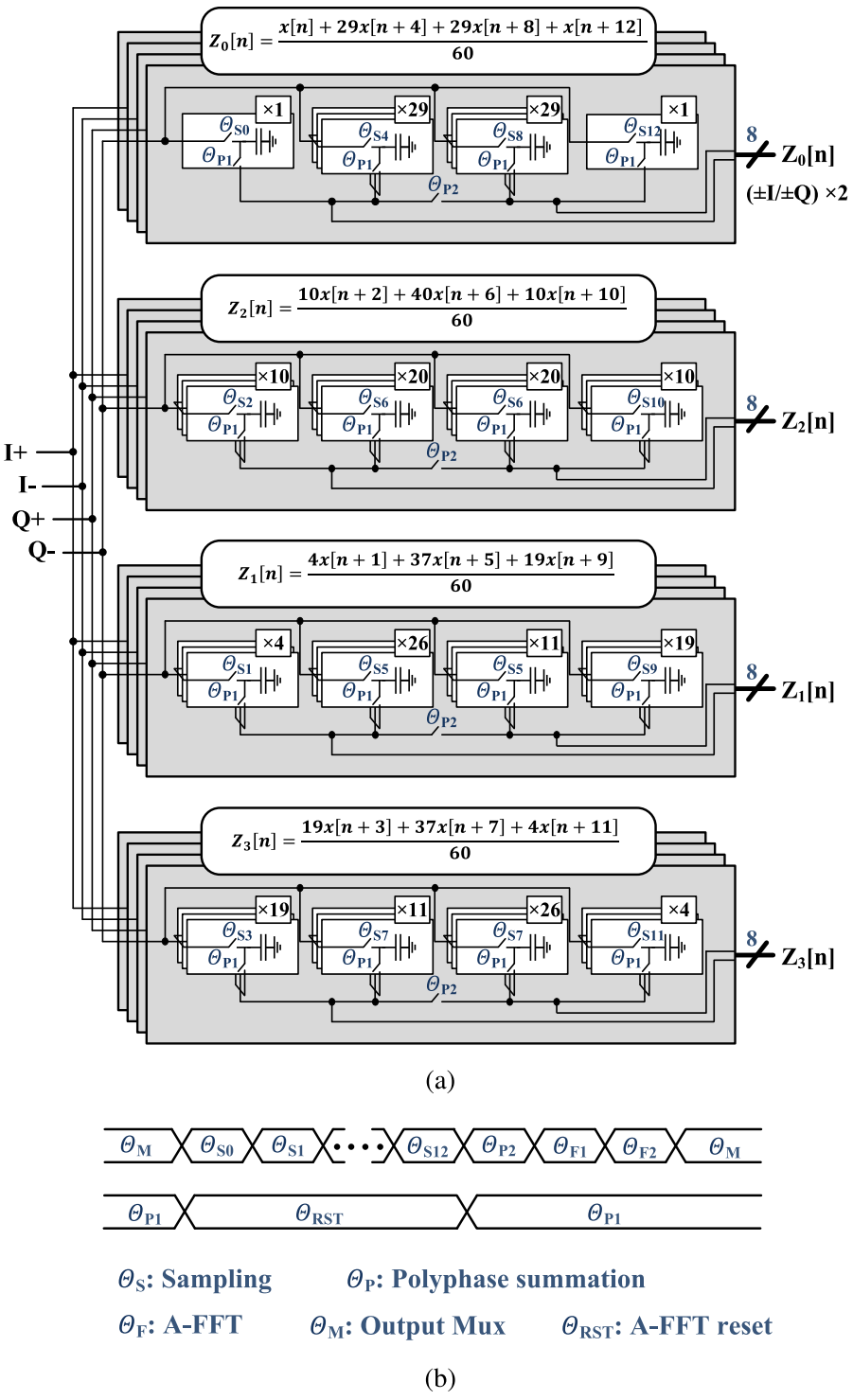


Fig. 13. (a) Schematic of analog polyphase window summation. (b) Clock sequence.

the 2 copies of the differential I/Q signals in the 4 channels. After selecting a channel to be connected to the output buffer, the speed is decimated to mitigate the speed requirement of the output buffer for testing. For the output buffer, PMOS source followers are employed for high linearity (i.e., no body effect). The simulation results show a +32 dBm IIP3 for the operation at 20 MS/s. Calculations for a cascaded system show that the total IIP3 degrades by 3 dB assuming 32 dBm IIP3 and 0 dB gain for the filter core. If the IIP3 of the filter core is less than that of the output buffer, the performance degradation is negligible (i.e., 0.8 dB degradation for 25 dBm IIP3 and 0 dB gain for the filter core). For both test structures (i.e., output MUX and output buffer), I/O devices are used with a 2.5 V VDD for a large signal range and linearity so that the performance of the core circuit with the 0.9 V VDD is not affected.

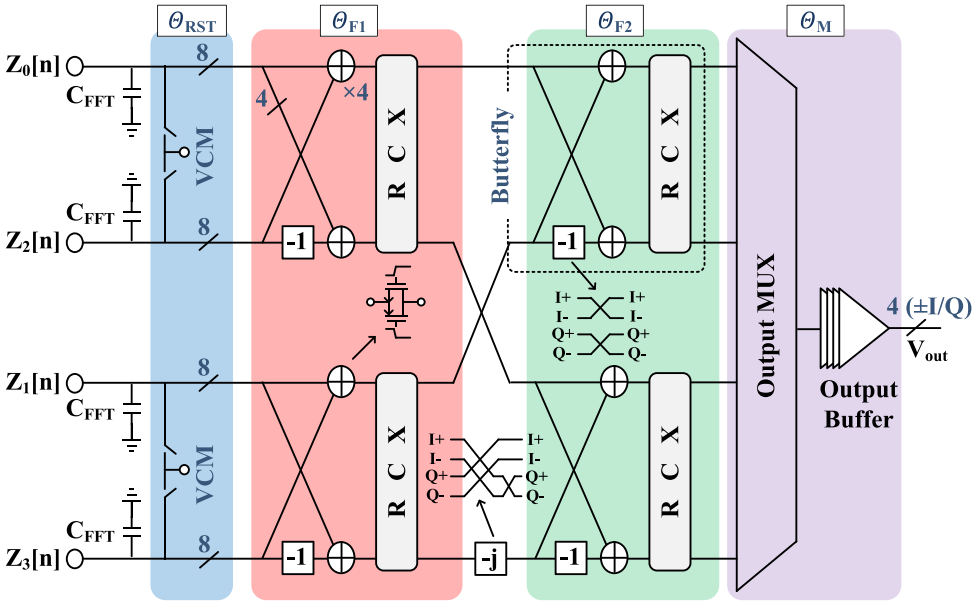


Fig. 14. Schematic of four-channel A-FFT.

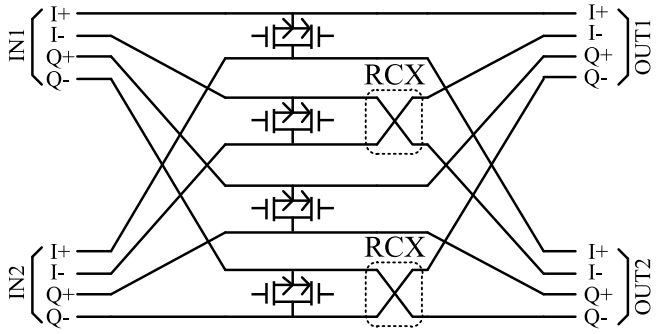


Fig. 15. Butterfly with RCX technique.

The required clock signals were generated from cascaded D flip-flops using external master clock and trigger signals. For non-overlapping signal generation, the output signal of the D flip-flop was delayed using an inverter chain and it was applied to an AND gate together with a non-delayed one. The schematic for the clock generation is shown in Fig. 17.

In this passive switched capacitor design, signal information is stored as charge in the capacitors, so the signals are vulnerable to corruption by coupling from an adjacent clock or adjacent signal lines. To mitigate these issues, the layout was done with ground shielding for all signal lines. All signal metal lines are surrounded by ground metals to prevent any signal coupling effects from other metal layers. With this ground shield methodology, the total parasitic capacitance increases, but any signal-dependent non-linearity errors are minimized.

In discrete-time circuits, the signals are processed as constant sample-and-hold values during each clock phase after the initial sampling operation. Therefore, for the mathematical computations described above, incomplete settling results largely in a gain error, but any clock variation or load variation with the input signal can result in some signal-dependent nonlinearity. In other words, the linearity performance is dominated by the initial sampling operation of the input signal at the start of the circuit. In this design, the sampling circuit was designed with the bootstrap technique [29] for high linearity, and the schematic for the bootstrap sampler is shown in Fig. 18. The pre-layout simulation results for the filter core (i.e., polyphase window including sampling circuit and A-FFT) show a 30 dBm in-band IIP3 for the 4 channels with 100 kHz to 20 MHz frequency offsets.

Each switching operation generates sampled noise (kT/C noise) on the capacitor. The total output noise can be calculated by considering the sampled noise power and noise gain of each stage [28]. Calculations show that the final differential output noise is $kT/(16C_{\text{unit}})$ when the FFT parasitic capacitance, C_{FFT}, is $30C_{\text{unit}}$. A larger sampling capacitor would improve the noise performance at the cost of speed. For our prototype, $C_{\text{unit}} = 9$ fF.

In this passive switched capacitor structure, the filtering performance is dominated by the quality of the capacitors that implement the window coefficients, where process variation and mismatch of the capacitors are likely to degrade the performance. To estimate this effect, a Monte Carlo simulation was performed. The simulation results show an absolute 3.4% variation, one sigma, of the 9 fF unit capacitor with a 2.7 μm $\times$ 2.7 μm area. The one sigma differential mismatch variation is 0.265%. Since the window coefficients are implemented with multiple unit capacitors, absolute process variation has little impact and only the relative mismatch variation is important. The simulation results show that the standard deviation of the side lobe at -60 dB is 1.12 dB due to the absolute process and relative mismatch effects.

The proposed circuit has an advantage that the operation is programmable by a clock signal like many other analog discrete-time circuits, but the performance is vulnerable to the jitter noise of the clock signal. The timing error from the clock jitter causes an equivalent amplitude error during the sampling

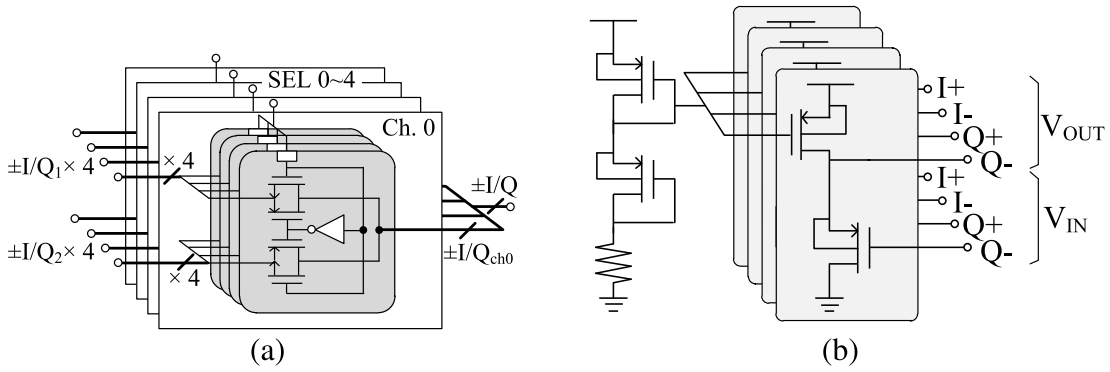


Fig. 16. Schematics of the output (a) MUX and (b) buffer.

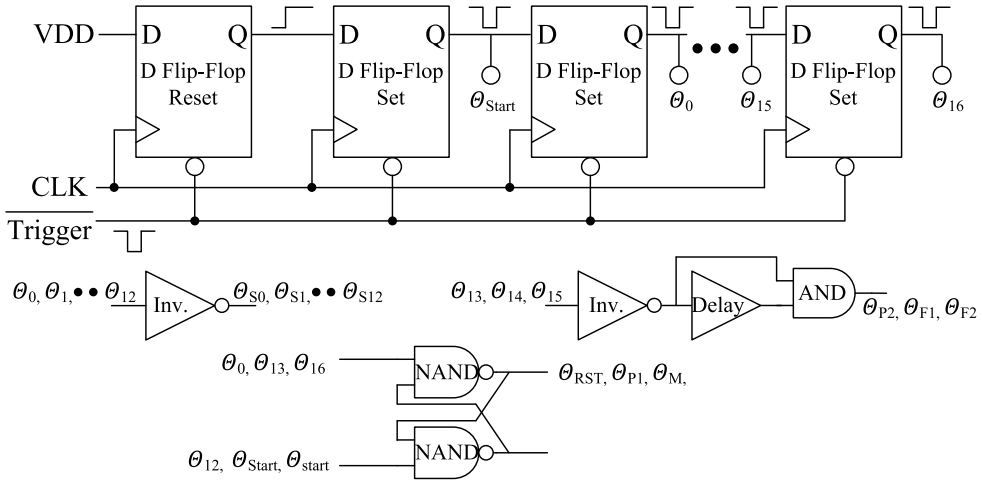
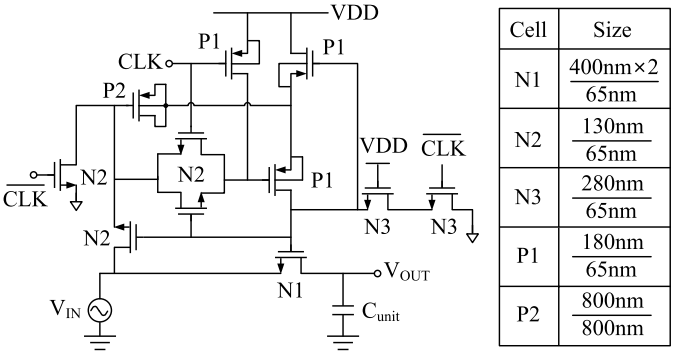


Fig. 17. Schematic of clock generator.



Cell	Size
N1	400nm×2 / 65nm
N2	130nm / 65nm
N3	280nm / 65nm
P1	180nm / 65nm
P2	800nm / 800nm

Fig. 18. Schematic of bootstrapped sampling circuit.

operation and limits the SNR performance. The equivalent SNR is given by the following equation for wideband white jitter noise [30]:

$$\mathrm{SNR}_{\mathrm{jitter}} = \frac{1}{(2\pi f_{\mathrm{in}}\sigma_t)^2}, \quad \sigma_t = \sqrt{E\left[\Delta t_{\mathrm{jitter}}^2\right]}. \tag{7}$$

In our case, we filter the output after it has been sampled. Therefore, the amount of jitter noise present in our filtered band is reduced. It can be shown that the noise power is reduced by 9.2 dB after the FIR filter considering the window coefficients that have been used in this design. With this result, the jitter noise at the sampler should be less than 459 fS to satisfy a 60 dB SNR for the full 1 GHz signal BW at the input.

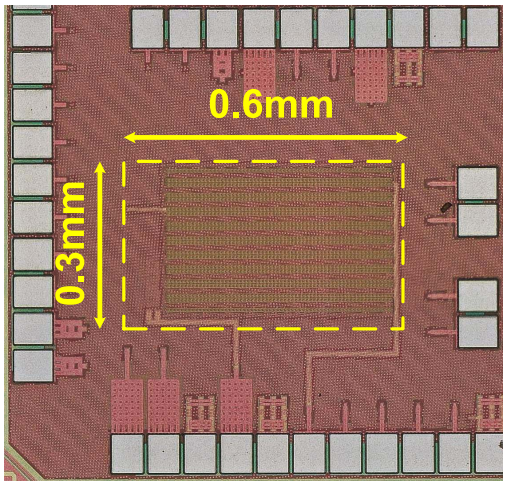


Fig. 19. Die photo.

IV. Measurement Results

The proposed P-FFT filter bank was implemented using TSMC's 65 nm GP process as shown in Fig. 19. The active

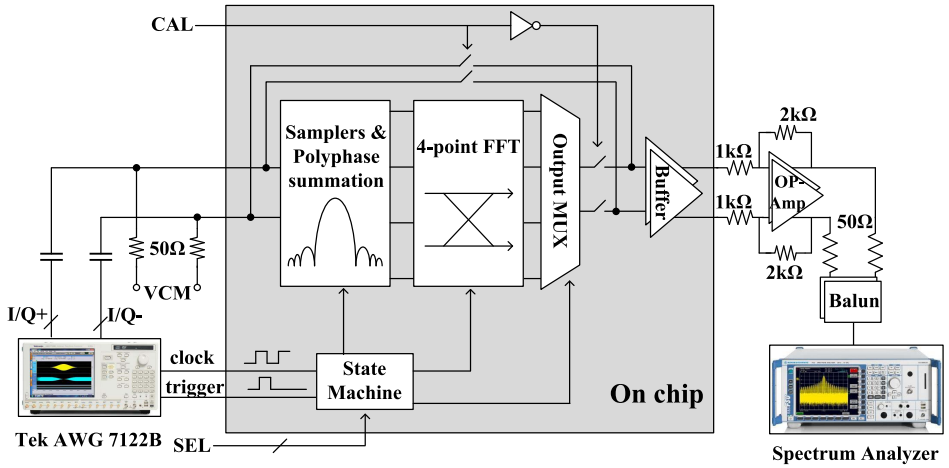


Fig. 20. Test setup.

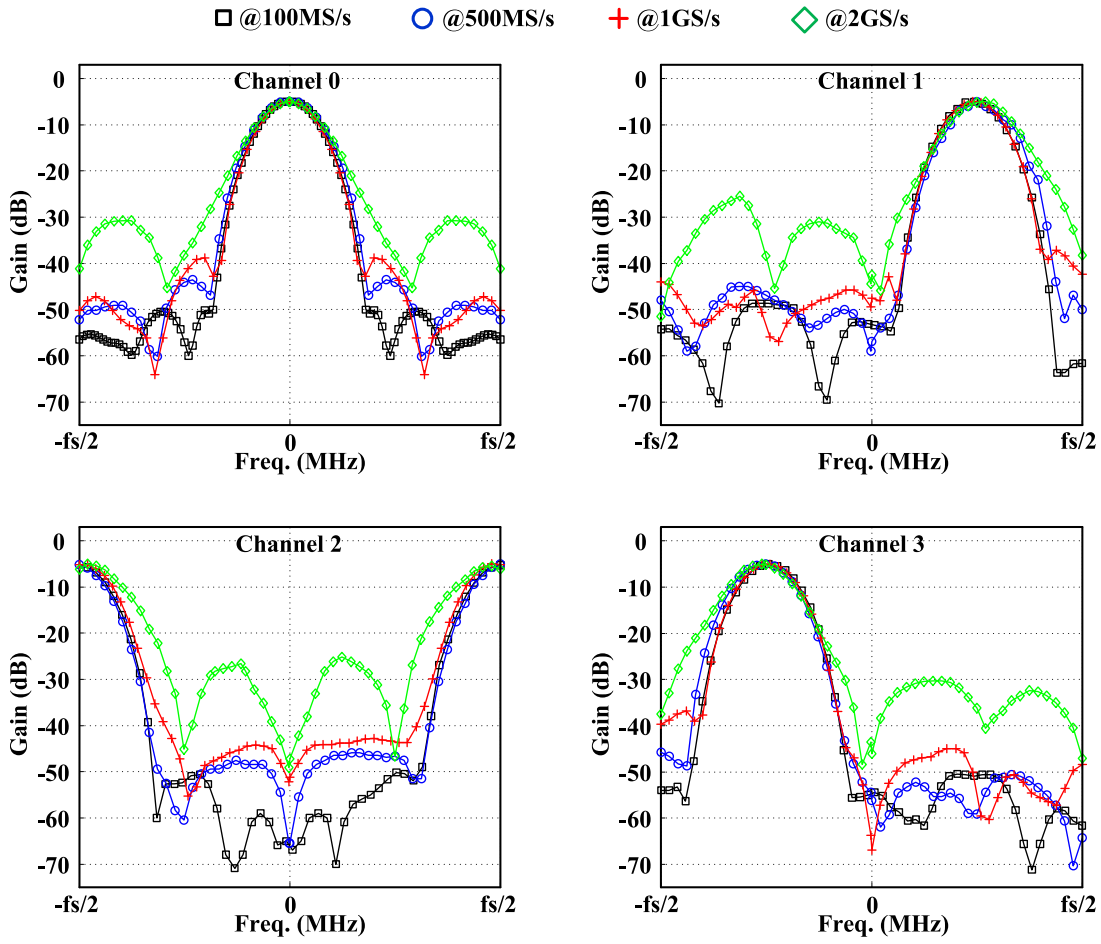


Fig. 21. Frequency response of the four-channel P-FFT filter bank.

area, including the state machine, output MUX, and buffers for testing, is 0.18 mm^2 and the area is dominated (80%) by the unit sampling capacitors that are used in the polyphase window summation block. The test setup is shown in Fig. 20. The differential I/Q inputs are supplied by a single signal generator to reduce the effect of an I/Q mismatch. The simulation result shows that a 5% amplitude and a 5° phase mismatch deteriorate the side-lobe performance by 9 dB and 16 dB, respectively. The master clock signal is also generated from the same instrument (*TEK AWG 7122B*). The control signals (SEL and CAL) for channel selection and calibration mode are set manually. In the calibration mode, the filter core is bypassed to measure the finite gain and output noise of the buffer. Wide BW and high linearity operational amplifiers (ADA4927 with 2.3 GHz and −3 dB BW and −98 dBc HD3 at 70 MHz) are employed on the printed circuit board so as

TABLE I
SUMMARY AND COMPARISON OF PERFORMANCES

	This work	[28]	[32]	[33]	[34]	[35]	[36]
Technology (nm)	65	65	45	130	65	90	65
Topology	FIR	FIR	FIR	FIR	FIR	FIR	FIR + IIR
Number of channels	4 x I/Q	16 x I/Q	1	1	1	1	1
Useful signal BW (GHz)	1.0	5.0	0.8	0.014*	0.05*	0.25*	0.026*
Power/channel (mW)	4.33	1.91	48	15.7	12	16.6	8.4**
Sampling speed (GS/s)	1.0	5.0	3.2	0.64	2.4	2.0	0.48
Side lobe gain (dB)	-38	-13	-30	-66	-40	-40	-85.5
Center gain (dB)	-5	-8.4	0	30	0	29	41
Linearity	25.3dBm IIP3	NA	-50 HD3	-17dBm IIP3	NA	-22dBm IIP3	-19 dBm IIP3
IRN (dBm/Hz)	-146	-155.2	NA	-156	NA	-155	-145
Area (mm2)	0.18	0.144	0.15	0.464	0.1	0.19	0.52

* -3dB bandwidth ** BW calibration is included.

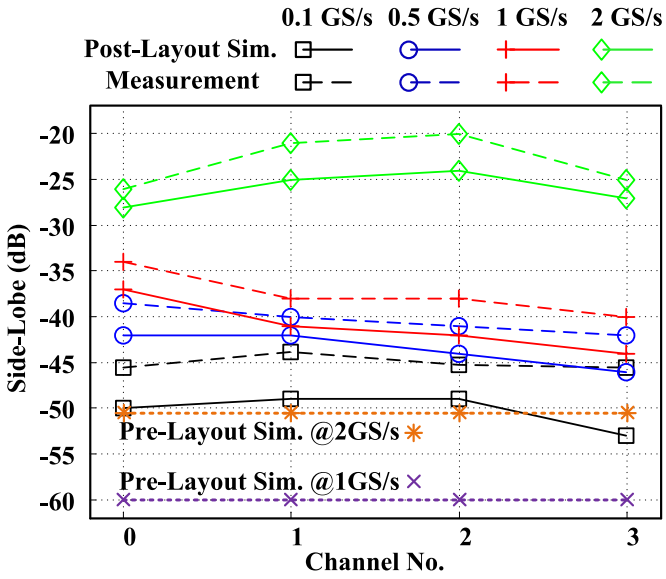


Fig. 22. Side-lobes per channel at different operating frequencies.

not to load the high output impedance of the system. The calculation shows that the impact of this OP-AMP on the linearity performance is less than 0.01 dB. The differential output signal of the OP-AMP is combined into a single-ended signal through a balun. The effect of the gain and phase mismatch of this balun is negligible for the performance measurements.

The frequency responses $((I^2+Q^2)^{1/2})$ of the four channels were measured at different sampling frequencies to evaluate the effect of settling errors. The result is shown in Fig. 21. In the result, Ch.2 has the highest center frequency, because the center frequency of Ch.3 is aliased to $-f_s/4$. The source follower's finite gain was calibrated out. The measured dc gain is -5 dB. This is due to the charge stealing by the input capacitance of the A-FFT during the Θ_{P1} phase. Specifically, the measured average side-lobe amplitudes of the 4 channels are -45, -40, -38, and -23 dB at 100 MS/s, 500 MS/s, 1 GS/s, and 2 GS/s, respectively. These results are 32, 27, 25, and 10 dB better than for a standard FFT (-13 dB). Fig. 22 shows the side-lobe amplitudes of each channel at different operating frequencies together with the post-layout simulation results, which include parasitic capacitances. The performance degradation from the ideal pre-layout one, i.e., -60 dB side-lobe, is due to the window coefficient variation caused by parasitic capacitance and due to settling errors. As the sampling frequency increases, we note that the degradation is more severe at 2 GS/s due to the finite settling errors of the switched paths.

For the linearity tests, the in-band IIP3 of each channel was measured using two tone signals. The signal spacing is 100 kHz and the center frequencies of the 2 tones are 1 MHz offset from the center frequency of each channel. Fig. 23 shows the measured results together with the IIP2 and P1dB performances at the 1 GS/s sampling frequency. The average IIP3 of the four channels is 25 dBm. This high linearity performance shows the benefit of passive switching [31]. The slightly lower IIP3 value at Ch.2 is caused by the higher frequency of the input signal and increased sampling error. Recall that Ch.3 at $3f_s/4$ is really operating at $-f_s/4$. The average IIP2 and P1dB performances of the four channels are 49.7 and 10.5 dBm, respectively.

For noise measurements, the input signal was grounded and the total output noise was measured. To calibrate out the effect of the buffer, the filter core was disabled and the output noise of the buffer was measured. The filter noise was calculated by subtracting the total noise power and buffer noise power [31]. The measured total average integrated differential output noise up to 1 GHz for the 4 channels is 208 $\mu V_{\rm rms}$. This is equivalent to an input referred noise power spectral density of -146 dBm/Hz considering the -5 dB dc gain.

Fig. 24 shows the energy and the corresponding power consumption including clock generation for the four-channel-I/Q (eight total) P-FFT filter bank at different operating frequencies. Due to the leakage power, the energy consumption per conversion decreases with a higher sampling rate and the power consumption increases almost linearly with an offset. (Ideally, the energy consumption per conversion should have been constant.) At 1 GS/s output, the total power consumption is 34.6 mW and the power consumption on a per channel basis

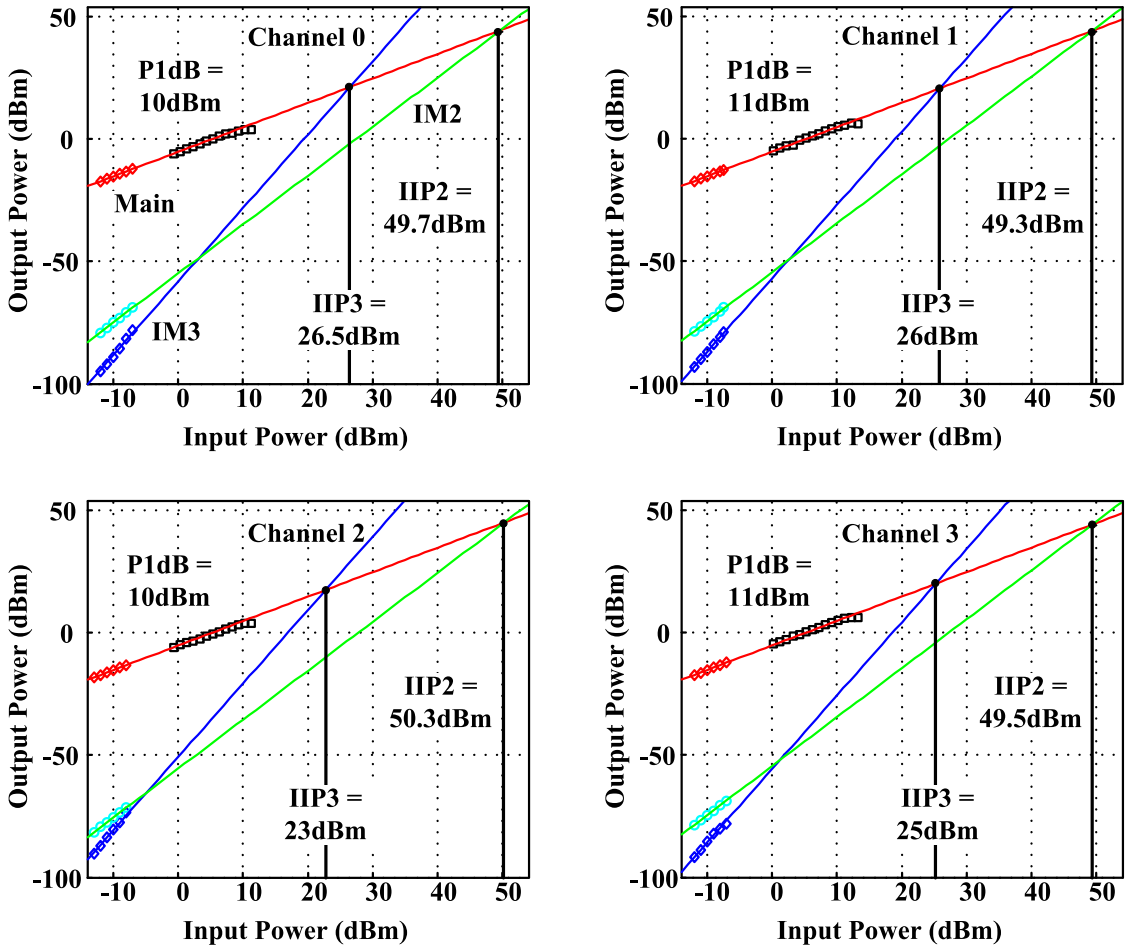


Fig. 23. IIP3, IIP2, and P1dB of four-channel P-FFT filter bank.

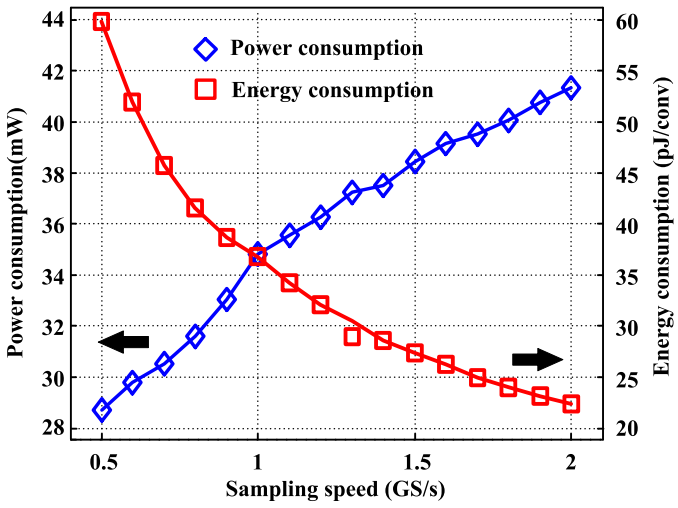


Fig. 24. Power and energy consumption of the four-channel P-FFT filter bank.

is 4.33 mW. The energy consumption at 1 GS/s is 34.6 pJ/conv. The simulation results show that 62% of this total measured power is consumed by the state-machine to generate the clock signals.

Table I summarizes the performance and compares it with those of other state-of-the-art discrete-time filters. With the proposed P-FFT technique, we implemented a four-channel-I/Q FIR filter bank. Due to the multi-channel outputs at the different center frequencies, it achieves a large ratio of the signal BW to the sampling speed as in [28]. It also shows low side-lobe amplitudes like other single channel filters due to its windowing operation. The passive switching operation provides high linearity. The power consumption per channel is the smallest among the window FIR filters because of the passive operation and the FFT-like power efficient algorithm. (There is no window function in [28].)

V. Conclusion

In this paper, a prototype analog four-channel-I/Q P-FFT filter bank was demonstrated using a 65 nm GP CMOS process. The structure allows an arbitrary effective window length. It enables a linear phase FIR filter bank with a narrower main-lobe width and lower side-lobe amplitudes than those for a standard FFT. Due to the FFT-like power efficient algorithm where common window coefficients are shared between the different filter outputs, low power operation is possible. The passive switched capacitor implementation enables high speed, high linearity, and low power consumption. Moreover, this scheme improves with technology scaling. The measured results of the 1 GHz signal BW, 25 dBm IIP3, and 4.33 mW power consumption per channel at 1 GS/s operation verify the superiority of the proposed scheme. The proposed structure

can be employed for low power channelization of wideband signals particularly in software-defined cognitive radios and for carrier aggregation. P-FFTs have the advantages of linear phase due to the FIR characteristic, easy extendibility to multi-channels using the FFT algorithm, the ability to easily reconstruct the original signal, and the ability to operate at higher switching frequencies as there is no feedback around the loop. The prototype here was designed to showcase the capabilities of the P-FFT for channelization but can be adapted to different standards specifications.

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