A 4GHz Instantaneous Bandwidth Low Squint Phased Array using Sub-Harmonic ILO Based Channelization

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***Abstract*—This paper presents a wideband channelized phased array receiver that uses sub-harmonic injection locked oscillators. The combination of channelization and sub-harmonic injection locking synchronizes the center of the sub-bands so beam squinting is reduced by the number of bands. Channelization additionally, reduces the performance requirements for the ADCs by reducing their speed requirement and also by reducing the SNR requirements due to a reduction in PAPR. The two-band prototype design realized in 65nm GP CMOS is centered at 9GHz, provides 4GHz instantaneous bandwidth, reduces beam-squinting by half (i.e., for 2 channels), consumes 31.75mW/antenna and occupies $2.7mm^2$ of chip area.**

I. Introduction

Multi-antenna systems use beam steering and spatial filters to combat co-channel interference. This becomes particular important as our data rate needs continue to increase and we increasingly need wideband systems for communications. Multicarrier radar systems that use instantaneous wide bandwidths are increasingly desired for multifunction (imaging and communications) systems [1].

Low squint wideband phased arrays can be realized using transmission lines [2] or RC delay elements [3]. The first technique is extremely chip area hungry and the second is limited to lower frequencies. Realizing wideband arrays using traditional phase compensation techniques causes beam-squinting due to the difference between phase and delay. A beam direction delay can be compensated at a given frequency by a fixed phase. However, the amount of phase compensation required changes with frequency and causes beam-squinting. Additionally, the extremely wide bandwidths desired places unrealistic constraints on the baseband data converters where there is a direct tradeoff between the maximum data rate and the feasible resolution [4].

Frequency channelization can be used to reduce the performance requirements for the ADCs. Channelization not only reduces the clock rate of the ADC but also reduces the number of in-band signals, hence, reducing the peak to average power ratio (PAPR) leading to an overall reduction in power consumption even though there are N parallel converters [5]. Prior frequency channelization for phase arrays has not directly solved the beam-squinting problem [6]. Here beam-squinting was only avoided by using an additional delay in the digital baseband.

The architecture proposed here simultaneously solves two problems, i.e., it solves the data converter performance requirement bottleneck by channelization but also reduces the beam-squinting problem by compensating for the required additional delay as a natural consequence of locking on to a higher order harmonic of the phase compensated local oscillator for the higher frequency bands. Section II discusses the new system architecture. Section III describes the circuit details and Section IV shows the measurement results. Section V concludes the paper.

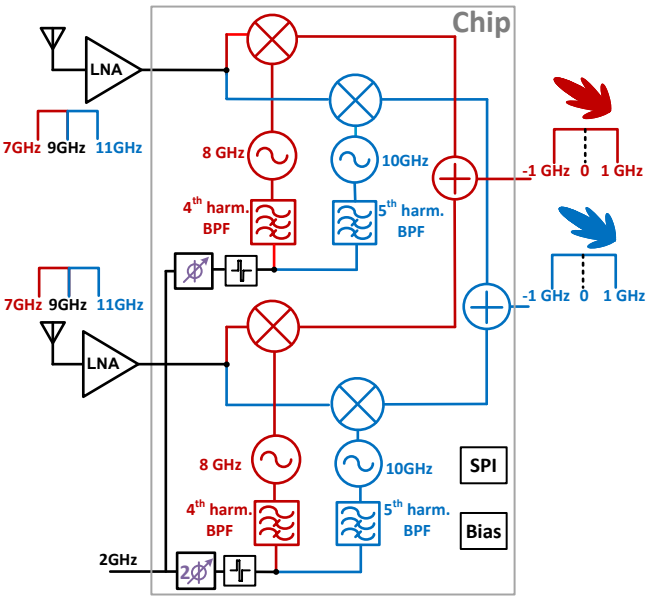


Fig. 1: Proposed low squint wideband phased array architecture using sub-harmonic ILO based channelization

II. Proposed Low Squint Wideband Architecture

The proposed architecture for the low squint wideband phased array architecture is shown in Fig. 1. The 4GHz bandwidth is centered at 9GHz and is broken up into two 2GHz bands. The first band is centered at 8GHz and uses the 4^{th} harmonic of a 2GHz LO and the second band centered at 10GHz uses the 5^{the} harmonic of the LO for down-conversion.

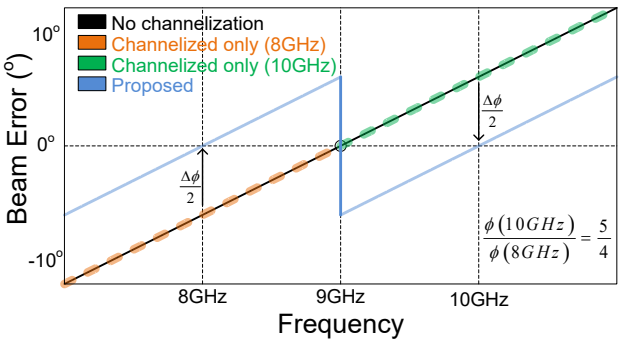


Fig. 2: Phase error vs. frequency for wideband phased array

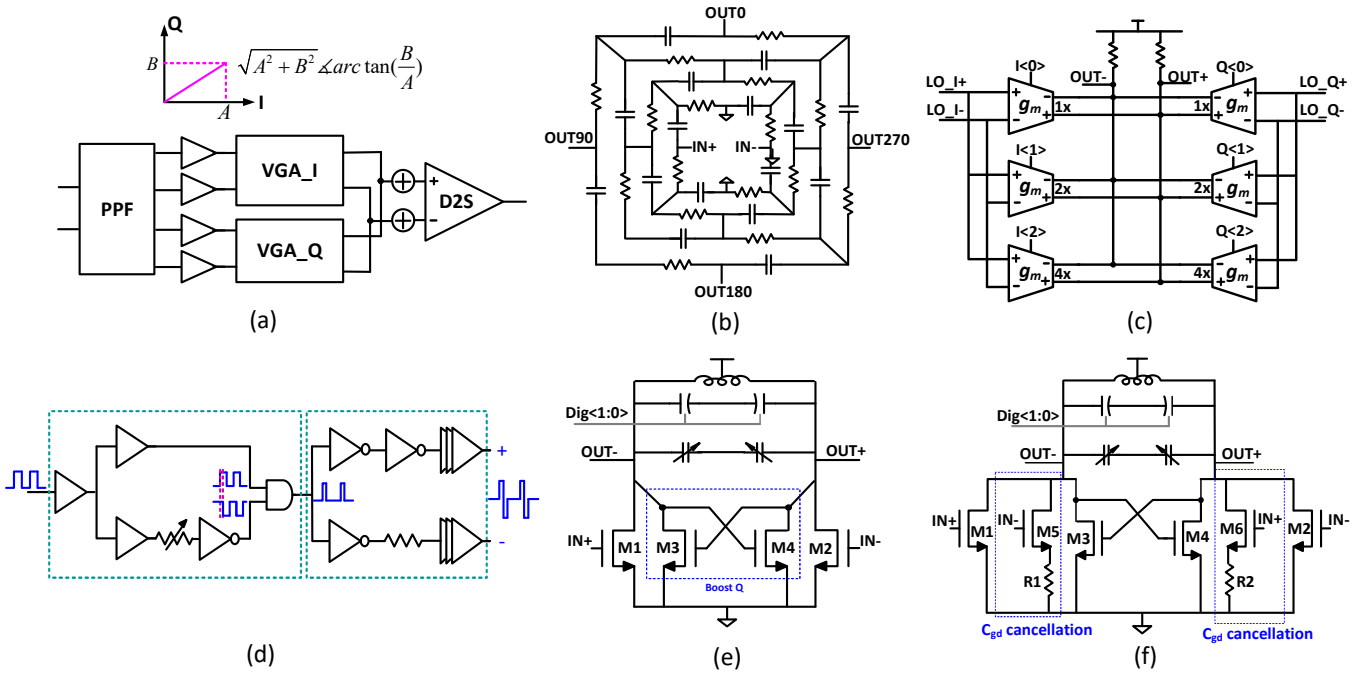


Fig. 3: (a) Phase shifter, (b) PPF, (c) I and Q interpolator, (d) Pulse slimmer, (e) BPF and (f) ILO

Before diving into the architecture details let us focus on the squint angle for a wideband phase array. The squint angle for a wideband phased array is given by Eqn (1), where Θ_0 is the desired beam angle, $\phi(\Theta_0, f_0)$ is the necessary phase compensation required at the band center, f_0, f is the frequency of operation, c is the speed of light and d is the inter-antenna spacing.

$$\Delta\Theta = \arcsin\left[\frac{\phi(\Theta_0, f_0)\cdot c}{2\pi f \cdot d}\right] - \Theta_0 \qquad (1)$$

The beam error vs. frequency for three different cases is shown in Fig. 2. Case 1, shown with the black line is the case when no channelization is done. Case 2, shown in orange (center at 8GHz) and green (center at 10GHz) is shown for the case when the total bandwidth is broken up into two bands. We note that the beam error remains the same. This is because there is an extra phase delta necessary to compensate for the sub-band center frequencies of 10GHz and 8GHz. In our architecture we injection lock to the 4^{th} and the 5^{th} harmonic of the 2GHz input. Note, in Fig. 1 that the progressive phase per antenna (ϕ and 2ϕ) is included before frequency multiplication. The frequency multiplication process multiplies the total phase such that the phase offset for the 5^{th} harmonic at 10GHz is greater than for the 4^{th} harmonic at 8GHz. This extra phase is exactly what is needed to offset the band center frequency phases such that we get the blue proposed line in Fig. 2. Note, we show straight lines for simplicity in Fig. 2. However, the actual lines are somewhat curved due to the arcsin.

The proposed channelization method reduces the beam error by approximately N times, where N is the number of frequency channels. For example, for our prototype design, the numerical values for the worst case beam error in the non-channelized design for a desired beam direction of -36^o from broadside is 13.1^o, while the worst case beam error for our two band design is 7.7^o. Additional channelization could be used to reduce beam error even further.

III. Circuit Design

The proposed 2-antenna phased array RX architecture was shown in Fig. 1. For each antenna, an external LNA amplifies the 7GHz to 11GHz signal, which is then down-converted and channelized into two sub-bands by two different LOs at 8GHz and at 10GHz. Each sub-band has a 2GHz instantaneous bandwidth. This design uses LO phase shifting.

Details for the circuit components are shown in Fig. 3. The LO path consists of a phase shifter, pulse-slimmer, band-pass filter (BPFs), and an ILO. The cartesian combiner based phase shifter, is shown in Fig. 3a. It consist of a four stage poly-phase-filter (PPF) that generates quadrature signals, a variable gain amplifier (VGA) with digitally controlled I/Q weights, and a differential to single-ended converter (D2S). The majority of the power is consumed by the phase rotators (i.e., two VGAs). Driven by a common LO input, the phase shifters provide the 2GHz LO signals with a progressive phase difference of ϕ.

The pulse slimmer (shown in Fig. 3d) that follows the phase shifter is a semi-digital circuit that NANDs two paths with different delays to created a reduced duty cycle pulse. The pulse width is optimized to be 14% so that is rich in the 4th and 5th harmonics for the 8GHz & 10GHz LO paths [5]. For the 8GHz LO, a BPF is tuned to select the 4th harmonic and suppress the other harmonics. The BPF is based on a high-Q ILO shown in Fig. 3e. It consists of a differential pair, one cross-coupled pair (X-pair), and a LC tank. The X-pair increases the Q of the LC tank.

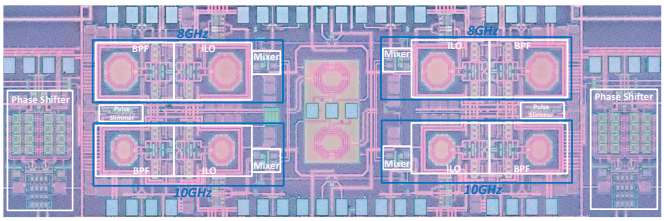


Fig. 4: Chip micrograph

An ILO tuned to 8 GHz is placed after the BPF, and injection locked by the BPF output, generates the 8GHz LO for down-conversion. The ILO in Fig. 3f uses a similar circuit to the BPF but adds an auxiliary X-pair consisting of M5, M6, R1 and R2, which cancels the drain-to-gate parasitic capacitance of the injection transistors. It not only provides isolation between the LC-tanks of the ILO and the BPF, to avoid high-order oscillations, but also reduces the parasitic capacitance added by the injection circuits, which nominally would have decreased the frequency tuning range. In simulations, this method shows better efficiency in comparison to the folded-cascode scheme in [7]. The phase difference between the two 8GHz ILO outputs is 4ϕ due to 4^{th} harmonic multiplication.

In a similar fashion, for the 10GHz LO path, another BPF selects 5^{th} harmonic of the same pulse slimmer output, followed by another ILO at 10GHz, that generates the 10GHz LO with a phase difference of 5ϕ for down-conversion. The phase difference between the two 10GHz ILO outputs is 5ϕ due to the 5^{th} harmonic multiplication. The two LOs that are generated provide the required frequencies for the sub-bands and also generate the necessary phase difference for each of the sub-bands. We note that the ratio of the phase difference for two sub-bands, i.e., $5\phi/4\phi$, is the same as the ratio of LO frequencies, which is 10/8. This additional phase eliminates beam-squinting at sub-band centers.

IV. Measurement Results

The micrograph for the chip fabricated in TSMC's 65nm CMOS process is shown in Fig. 4. The active area of the chip is $2.7mm^2$. The BPFs and VCOs operate at 0.5V supply, and the phase shifters operate at 1.5V. All the other blocks are operated at 1V. The overall power consumption is 63.5mW.

For our measurements, the two RF inputs are connected to a R&S ZVA67 network analyzer via SGS probes. A R&S SMW signal generator supplies the 2GHz LO signals. The outputs are connected to a R&S FSW43 spectrum analyzer via an off-chip balun. Additional on-chip GSSG PADs (via buffers) are used to characterize the ILO performance. A Total Phase AArdvark SPI host adaptor provides the necessary interface for the on-chip register setup. The entire measurement setup is controlled via Labview for accurate beam pattern generation. The measured return losses for the two RF inputs are better than -12dB over the frequency range of 7GHz to 11GHz.

GSSG PADs after the ILO test buffers were connected to a FSW43 spectrum analyzer to evaluate LO performance. Two digital bits for the capacitor array and a varactor were

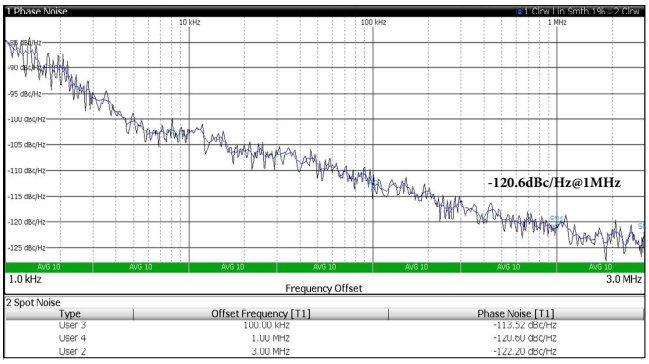


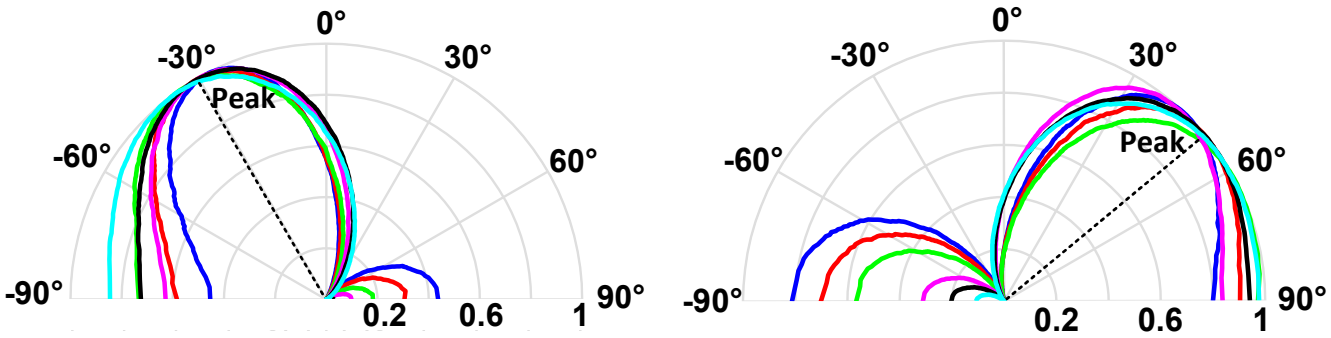
Fig. 5: Measured phase noise at 8GHz

used to adjust the ILO center frequency. The ILO center frequencies varied from 6.66 GHz to 8.551 GHz for the low frequency sub-band, and from 8.04 GHz to 10.498 GHz for the high frequency sub-band. The measured ILOs phase noise characteristic for the LO at 8 GHz is shown in Fig. 5. The measured phase noise is -120.6dBc/Hz @1MHz offset and the measured phase noise for the 10GHz LO at the same offset was -118.1dBc/Hz. Theory suggests a 1.94dB offset which is close to the measurements.

To accurately test wideband phase arrays the RF antenna inputs must use progressive time delays. We use a R&S ZVA67 to generate our RF inputs. However, by default when the ZVA67 is set up in coherent mode the two signals that are generated have relative phases (instead of delays). We resolve this issue via programming the phases for each individual frequency. Specifically, for a spatial beam direction of θ corresponding to a phase difference of ϕ at 11GHz, the phase difference at 10GHz, 9GHz, 8GHz, and 7GHz are set to be $\frac{10}{11}\phi$, $\frac{9}{11}\phi$, $\frac{8}{11}\phi$ and $\frac{7}{11}\phi$ respectively. We use the same methodology to generate the equivalent phases for each beam direction and frequency.

The measured normalized array patterns for two different spatial angles are shown in Fig. 6. The different curves represent measurements for RF signals at 7GHz (cyan), 8GHz (black), 9GHz-(magenta), 9GHz+ (green), 10GHz (red) and 11GHz (blue). The first three are measured at the 8GHz sub-band, and the latter three are measured at the 10GHz sub-band. The left plot shows the measurements for a beam direction of -30^o and the right plot shows the measurements for a beam direction of 52^o. We can see that after channelization, i.e., reducing the fractional bandwidth, and automatic compensation for beam-squinting among sub-bands, the peaks of the beams are aligned at the desired spatial angles. In particular, the beams peaks at 8GHz and 10GHz are perfectly aligned and beams at 7GHz and 9GHz- are well aligned and the beams at 9GHz+ and 11GHz are well aligned as might be expected from Fig. 2.

The measured null-depth is better than 23dB for all cases. Note, the nulls are not aligned and are a function of antenna spacing and frequency. The performance of the prototype is summarized and compared with other work in Table I. Among the other designs that attempt to mitigate the beam-squinting issue, this work exhibits a smaller size in comparison to



(a) (b)

Fig. 6: Measured normalized array patterns for the receiver at different frequencies (different colors) [LHT -30^o, RHT 52^o]

TABLE I: PERFORMANCE COMPARISON

Ref. No.	Technology	Area (mm^2)	Channel No.	Delay/Phase Shifting	True Time Delay	Cent. Freq. (GHz)	Frac. BW (%)	Null-depth (dB)	Power/antenna (mW)
[2]	CMOS 130nm	9.9	4	RF	Syn. T-line	8	175	-	138.75
[3]	CMOS 140nm	1	4	RF	Analog Delay	1.75	87.2	>20	112.5
[6]	CMOS 65nm	0.94	2	IF	Spectral Channel.[1a]	8	-	>19	13.7
[7]	BiCMOS 90nm	7.1	2 x 2^2	LO	No[3]	78	20	>17	168.1
[8]	CMOS 130nm	15.6	4	LO	No[3]	12	100	>12.5	86.8
[9]	CMOS 65nm	1.08	4	IF	No[3]	2.5	120	>25	23.1
This work	**CMOS 65nm**	**2.7**	**2 x 2^{2b}**	**LO**	**Spectral Channel.[1b]**	**9**	**44.4[4]**	**>23**	**31.75**

[1a] Beam-squinting not solved among bands. [1b] Beam-squinting solved among bands. [2a] 2 antenna x 2 antenna. [2b] 2 antenna x 2 spectral band. [3] Beam-squinting not considered. [4] Can be extended by more spectral bands.

conventionally synthesized transmission line methods, and can work at a high frequency range in comparison to the analog delay approach [9]. The power consumption is lower than most of other delay/phase shifting methods except [6] and [9] which adopt IF phase shifting. Only [6] and this work feature simultaneous spectral channelization and beamforming, but [6] does not solve the beam squinting problem. This architecture reduces beam-squinting by using a combination of channelization and sub-band phase correction.

V. Conclusions

This paper presents a new 4GHz instantaneous bandwidth phased array receiver based on sub-harmonic injection locked oscillators. The combination of channelization and sub-harmonic injection locking synchronizes the center of the sub-bands so beam-squinting is reduced by the number of bands. Additionally, channelization reduces the performance requirements for the ADCs by reducing their speed requirement and also by reducing the SNR requirements due to a reduction in PAPR. Thus reducing total power. The two-band prototype design realized in 65nm GP CMOS is centered at 9GHz, provides 4GHz instantaneous bandwidth, reduces beam-squinting by half, consumes 31.75mW/antenna and occupies $2.7mm^2$ of active area. Using frequency channelization and phase compensation for the two sub-bands reduces worst case beam-squinting by nearly half. Additional channelization can be used to reduce beam-squinting even further. The methodology introduced here allows for wideband phase arrays to have low beam-squinting without relying on true-time delay elements that are difficult to program and consume significant area.

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