A 2.4GHz IEEE 802.15.6 Compliant 1.52nJ/bit TX & 1.32nJ/bit RX Multiband Transceiver for Low Power Standards

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***Abstract*—This paper describes an 802.15.6 compliant 2.36-2.484GHz multiband transceiver that uses an energy efficient programmable digital power amplifier on the transit side and a zero power passive voltage gain frontend using a 1:3 balun on the receive side to achieve low power operation. A 7th harmonic injection locked oscillator and zero power passive polyphase filter generates the phases at 2.4GHz required for phase modulation on the transmit side and for LO generation on the receive side. This enables channel selection using a 342.86 MHz PLL, i.e., at 1/7th of the RF frequency of 2.4GHz to result in low power consumption. The prototype transmitter consumes 1.48 mW of power while delivering -9.47dBm output power resulting in an energy efficiency of 1.52nJ/bit at 971kbps data rate. The measured RMS EVM for $\pi/4$ DQPSK modulation is 5.68%. The prototype receiver consumes 1.29mW of power resulting in an energy efficiency of 1.32nJ/bit while achieving a receiver noise figure of 10.2dB and an IIP3 of -24.1 dBm. This design does not use offchip inductors.**

I. Introduction

Due to the large expected number of connections in 5G and the advent of IoT and WBAN there is an increased demand for low power radios [1]–[3]. Unfortunately, traditional radio transmitters based on homodyne or super-heterodyne conversion schemes are power hungry due to the presence of phase locked loops (PLLs) operating at the RF frequency, need for linear mixers and high performance data converters. Further, transmitters based on polar modulation lead to more complex circuit designs. On the receive side, traditional architectures turns out to be power hungry due to the presence of the LNA at RF, linear mixers and high performance ADCs. In this paper we present a transceiver compatible with the IEEE 802.15.6 standard [4] which employs 7th harmonic injection locking to generate phases at RF thereby drastically reducing power. The transmitter uses an energy efficient fully programmable digital power amplifier with pulse shaping capability. The receiver has a zero IF architecture and uses zero power passive voltage gain and passive voltage mode mixers to substantially reduce power consumption.

II. Block Diagram

The block diagram of the complete transceiver is shown in Fig. 1. The transmitter consists of a digital phase-MUX based PA which uses sinusoidal quadrature phases for PSK modulation. The sinusoidal quadrature phases are generated by a passive polyphase filter driven by an oscillator at 2.4GHz which is injection locked to the 7th harmonic of the reference at 342.86MHz. A pulse slimmer [5] enhances the 7th harmonic

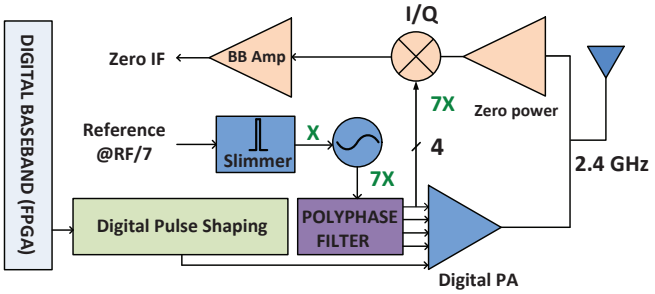

Fig. 1. Block diagram for the proposed low power transceiver

content at 2.4 GHz. Consequently, channel selection can be achieved by an integer N PLL running at 1/7th the RF frequency which drastically reduces power consumption for frequency synthesis. In this prototype design the standard integer-N PLL needed has not been included. However, its impact on the overall architecture and power consumption has been discussed in the measurements section of the paper. The receiver is based on a zero IF I/Q architecture. It employs a passive gain stage followed by passive mixers and class AB baseband amplifiers for demodulation of the received signal.

III. Circuit Diagram

The circuit diagram for the transmitter is shown in Fig. 2. A 342.86 MHz external reference at 1/7th RF frequency is applied to a pulse slimmer. The slimmer generates pseudo differential outputs suitable for injection locking. It consists of a duty cycle control stage to enhance the 7th harmonic followed by a differentiator which suppresses lower harmonics and eliminates even order harmonics [5]. The ILO is a PMOS-NMOS current reuse oscillator which is followed by a low power LC tuned buffer. The cross-coupled pair transistors are low threshold (Vt) devices so that they contribute maximum gm for the same overdrive voltage. However, the tail current source transistor is a high threshold (Vt) device to prevent leakage due to the low threshold (Vt) devices in the cross-coupled pair. The LC buffer drives a zero power passive RC polyphase filter and generates sinusoidal quadrature I/Q phases. The quadrature phases are again buffered by a drive amplifier (DA)/LO buffer which distributes the signal to the digital power amplifier on the TX side as well as to the mixers on the RX side to serve as the LO.

The transmitter consists of a digital phase-MUX based power amplifier which uses the sinusoidal quadrature phases to

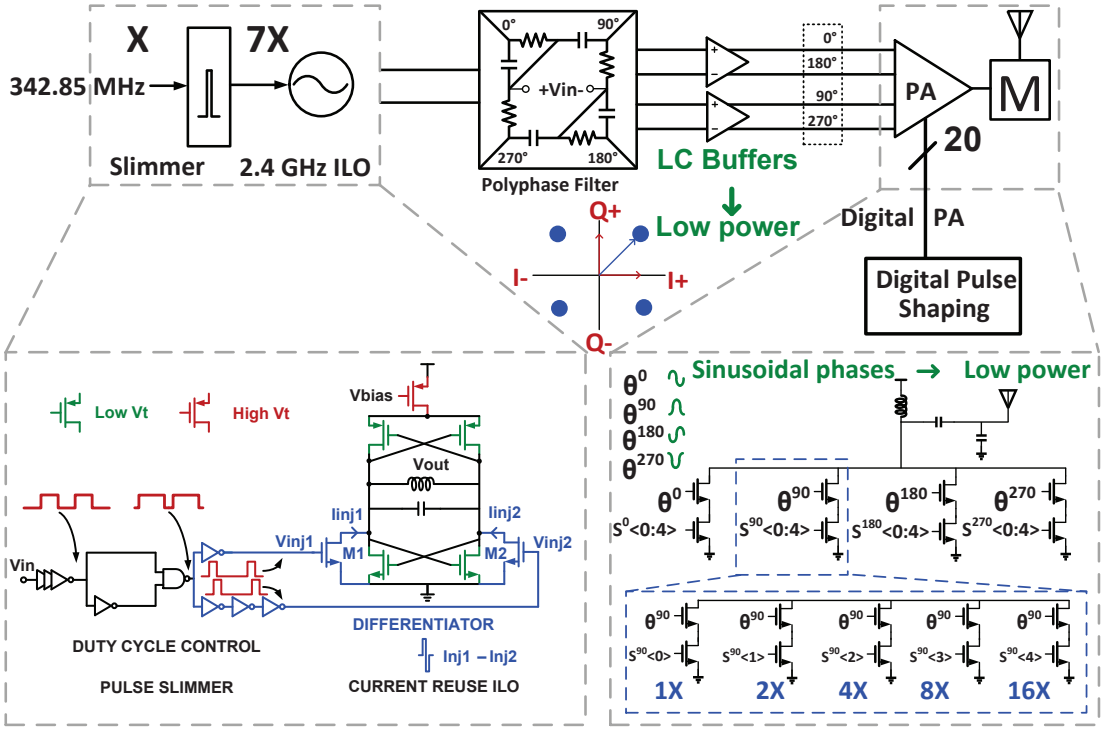

Fig. 2. Overall circuit details for the proposed transmitter

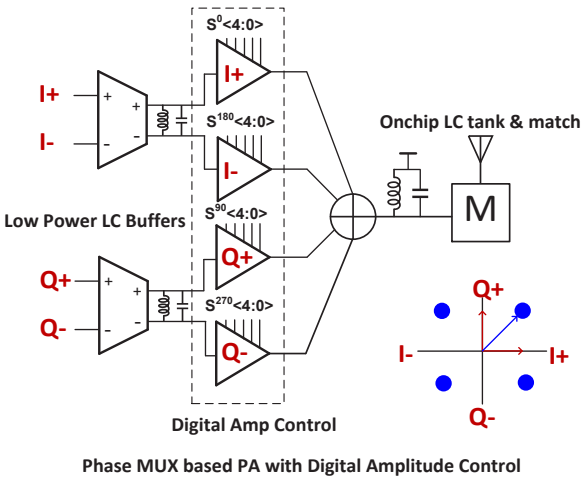

Fig. 3. Conceptual circuit block diagram for the PA

perform modulation. The transistor level circuit was shown in Fig. 2 but a more easily understood conceptual block diagram is shown in Fig. 3 for clarity. The digital amplitude control block serves both as a MUX performing phase selection and as a DAC performing amplitude control which satisfy the key requirements for phase modulation with baseband pulse shaping. Currents due to the selected phases of the appropriate amplitudes are summed at the PA output to achieve digital phase modulation. There are 4 phases and each phase has a 5 bit amplitude control resulting in 20 bit control lines. These lines are controlled by the digital pulse shaping logic which implements the square root raised cosine filter as specified in the standard. In this prototype the digital control block is implemented offchip in an FPGA. In contrast with traditional designs [6], the PA uses sinusoidal phases generated by the polyphase filter instead of square wave phases which reduces the power consumption of the buffers driving the PA and improves the spurious response. The buffers consume low power because for the same swing, the power consumption of a tuned buffer is Q/π times lower than that for CMOS inverter based buffers where Q is the quality factor of the inductor. These buffers have a supply voltage of 0.5VDD which further reduces their power consumption. The inductive load enables a swing of 1V peak to peak. Unlike other designs [6] an integrated matching network is included onchip.

The receiver uses a zero IF I/Q architecture as shown in Fig. 4. The onchip 1:3 step up balun provides zero power passive voltage gain. We have designed a symmetric low loss balun to minimize phase imbalance. The mixers used are passive double balanced voltage mode mixers. Unlike current mode operation, voltage mode operation does not require low input impedance transimpedance amplifiers (TIA) in the baseband which consumes significant power. Though voltage mode operation has lower linearity it is sufficient for this standard. The baseband amplifiers operate in class AB mode to achieve low power and sufficient linearity.

IV. Measurement Results

The prototype transceiver was implemented in Global Foundry's 130nm CMOS technology and occupies an area of 1.57mm^2. The die-micrograph is shown in Fig 5. The

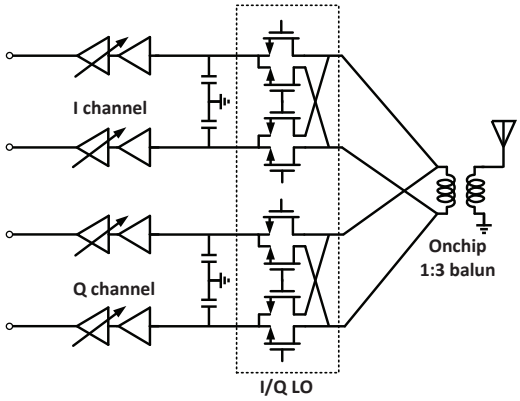

Fig. 4. Receiver frontend circuit details

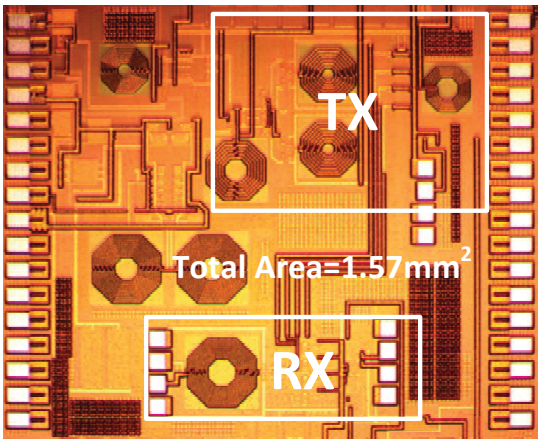

Fig. 5. Die-micrograph for the proposed transceiver

measured RMS EVM for $\pi/4$ DQPSK modulation is 5.68% as shown in Fig. 6. The transmitter output mask is shown in Fig. 7 which shows an ACPR of -27.07dB at a transmit power of -9.47dBm. The PA consumes 520µW power while delivering -9.47dBm output power to a 50 ohm load. The noise figure of the receiver chain is 10.2dB at 2.36GHz as shown in Fig. 8 and the IIP3 is -24.1dBm which is sufficient for the standard (-19dBm [7]). The conversion gain is 62.7dB at RF frequency of 2.36 GHz as shown in Fig. 8. The prototype does not include a PLL. Fig. 9 shows the plot of the power consumption vs frequency of recent PLLs in literature which indicates an increasing trend of power at higher frequencies. The plot validates the viability of a 342.86 MHz PLL consuming approximately 450 µW. The phase noise requirement for the PLL at 2.4GHz for this standard is -94.26dBc/Hz at 1MHz offset . Therefore, the phase noise specification for the 342.86 MHz PLL will have to be 20log(7)dB lower due to 7th harmonic lock, i.e., -103.8dBc/Hz. In order to achieve a reasonable power estimate only PLLs satisfying this phase noise criterion [8]–[11] have been included in Fig. 9. The required channel spacing and reference frequency for this integer N PLL is 1MHz/7, i.e., 142.8KHz due to 7th harmonic lock. A 10MHz crystal followed by divide by 70, consuming a few microwatts of power, may be used for

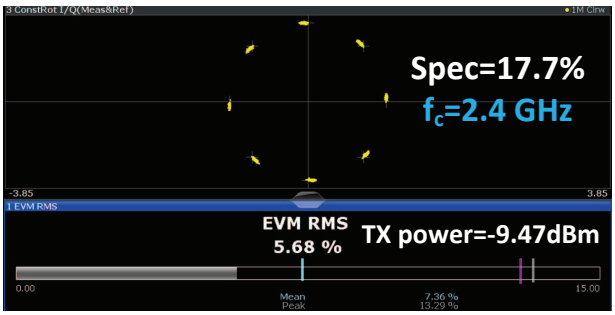

Fig. 6. Measured EVM for the transmitter

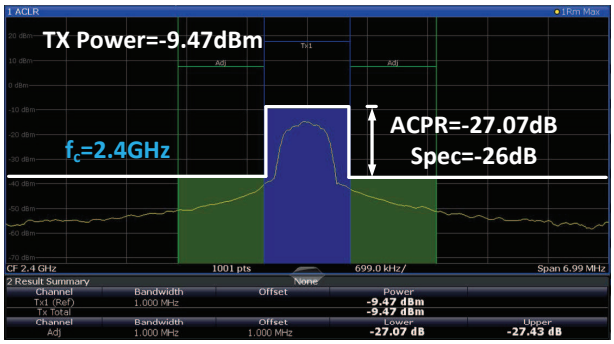

Fig. 7. Measured ACPR for the transmitter

reference generation. After including the estimated PLL power the total power consumption for the transmitter is 1.48mW with 1.52nJ/bit efficiency and that for the receiver is 1.29 mW with 1.32nJ/bit efficiency. The performance of the prototype is summarized and compared with state of the art designs in Table I. The design has the lowest power and highest efficiency per bit. The noise figure is sufficient for the standard.

V. Conclusion

We have proposed a new architecture for a fully integrated low power transceiver compatible with the IEEE 802.15.6 standard which employs 7th harmonic injection locking. The design has no offchip inductors. The transmitter uses an

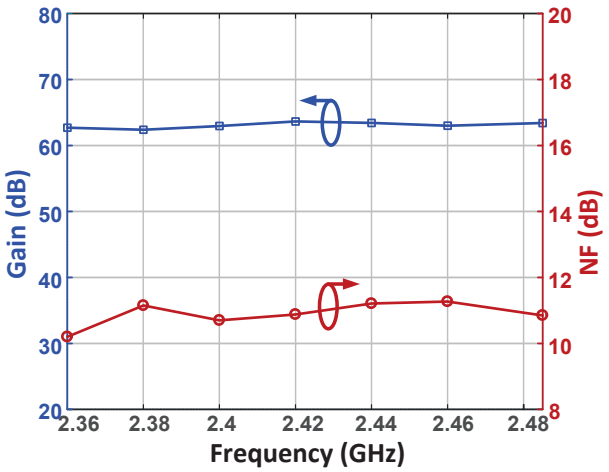

Fig. 8. Measured gain and noise figure for the receiver

TABLE I
PERFORMANCE COMPARISON

References	[12]	[13]	[14]	[15]	[1]	**This Work**
Publication title	-	ISSCC′12	ISSCC′12	ISSCC′13	RFIC′14	-
Standard	BLE	802.15.6	802.15.6	802.15.6	802.15.6	**802.15.6**
Frequency (GHz)	2.4-2.484	2.36-2.4	2.36-2.484	2.3-2.484	2.3-2.484	**2.3-2.484**
Data rate	1Mbps	971kbps	971kbps	971kbps	971kbps	**971kbps**
Modulation	GFSK	$\pi/2$DBPSK	$\pi/4$DQPSK	$\pi/4$DQPSK	$\pi/4$DQPSK	$\pi/4$**DQPSK**
Technology	-	90nm	130nm	90nm	130nm	**130nm**
TX Pout (dBm)	0	-10	-10	-10	-10	**-9.47**
TX EVM (%)	-	7.6%	10.1%	7.3%	3.21%	**5.68%**
TX power[1](mW)	17.8	5.2	5.9	4.6	3	**1.48**
TX energy efficiency[2](nJ/bit)	17.8	5.35	6	4.73	3.1	**1.52**
RX noise figure (dB)	-	-	6	6	-	**10.2**
RX power[1](mW)	21	-	6.5	3.8	-	**1.29**
RX energy efficiency[2](nJ/bit)	21	-	6.7	3.91	-	**1.32**

[1] Total power excluding digital baseband power.
[2] Energy efficiency calculated using the data rate in this table.

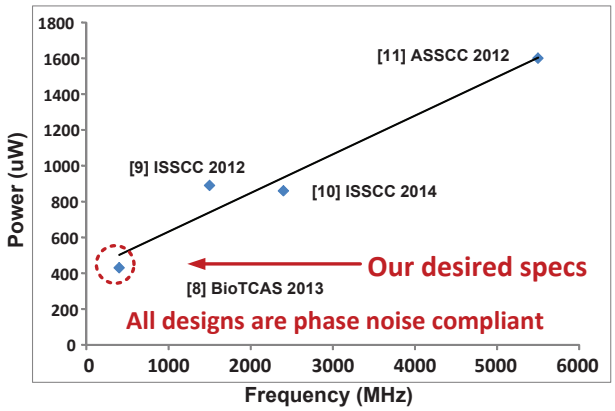

Fig. 9. Power vs frequency of existing PLLs in literature

energy efficient programmable digital power amplifier. The power amplifier uses quadrature phases generated by a simpler passive polyphase filter as compared to our previous design. The simpler polyphase filter results in less signal loss and lower buffer power. The receiver uses passive voltage gain and passive voltage mixers to reduce power. This design is simpler and more robust in comparison to standard polar modulation schemes. The transceiver is more energy efficient than the state of the art by a factor of 2X on the transmit side [1] and 3X on the receive side [15]. Traditionally, high data-rate transceivers with complex architectures and higher order modulation schemes result in high spectral efficiency. The new simple architecture and design changes made here allow us to approach the 1nJ/bit limit for low power transceivers. Though the design was made to be IEEE 802.15.6 compliant, much of design and circuit architecture is easily portable to emerging low power standards.

ACKNOWLEDGMENT

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