A Multi-Mode DC-DC Converter for Direct Battery-to-Silicon High Tension Power Delivery in 65nm CMOS

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***Abstract*—We present a multi-mode DC-DC converter that directly takes the output of a Li-ion battery and converts it to on-chip voltages suitable for integrated electronics. The design in standard 65nm CMOS converts the Li-ion battery voltage that can vary between 4.2V to 2.8V directly to a internal V_{DD} voltage that ranges between 1.5V to 0.3V. The 65nm design safely handles the high voltage delivery while providing conversion ratios between 1 to 13. To maintain high efficiency throughout, the proposed DC-DC converter functions in three distinct modes - resonant, soft-switching and four-level-buck. We use a bond wire inductor (≈11nH) as the high Q passive for all three modes. The design uses core devices only. The converter handles load currents between 0.5-200mA (400X), achieves a peak efficiency of 86.6% and has a peak power density of 0.3W/mm^2. The prototype was fabricated in TSMC's 65nm GP CMOS.**

I. Introduction

According to the 2015 ITRS road map, future VDDs will continue to decrease, i.e., 0.75V (14nm) and 0.6V (6nm). Technology scaling has enabled implementations of entire systems on a chip. But the primary power source for these systems continue to be chemical batteries with Li-ion dominating. Unfortunately, there is a voltage mismatch (i.e., an impedance mismatch in the voltage domain) between the 4.2-2.8V battery voltage and the desired sub-1V preferred for the low power SOCs (Fig. 1). Currently, the voltage conversion from the battery to the SOC is done via a separate power management IC (PMIC) which is normally fabricated in higher voltage processes such as BCD (Bipolar-CMOS-DMOS). The PMIC, in Fig. 1, adds to the PCB footprint, increases efficiency-loss and increases costs. Our design allows for a plug and play direct-battery-to-silicon (DBS) power transfer in standard CMOS processes. The circuit has been designed to be modular and to be easily ported across processes.

As seen in Fig. 1, the DBS technique allows for direct power transfer from the Li-ion battery and eliminates the addition of a PMIC in between. Considering an average Li-ion voltage of ≈3.6V and average SOC voltage of ≈0.9V we get a conversion ratio of 4. So, ideally, the current going into the SOC is now 4X lower than with a PMIC present. This high tension power delivery lowers the board level I^2R routing losses by 16X and the Ldi/dt issues by 4X. Thus, it will lead to an improvement in the overall efficiency of the power transfer pathway. Additionally, eliminating the PMIC reduces the bill of materials (BOM) costs. Further, a DBS system allows plug and play design solutions that simplifies system changes. A new SOC can easily be added or swapped into the battery grid without the need of a PMIC interface.

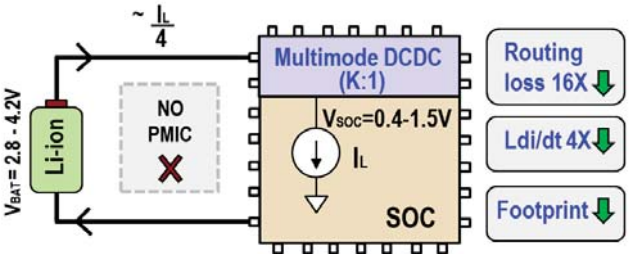

Fig. 1: Motivation for direct battery to silicon (DBS) via a multi-mode DC-DC converter with a variable conversion ratio (K). High tension power delivery reduces the power loss, Ldi/dt issues and footprint.

There is significant interest in high-tension power delivery. Both inductive and capacitive converters have been used to address this problem of handling higher voltages in standard CMOS while maintaining a good power conversion efficiency. In an inductive buck converter described in [1], a cascode of three 1.8V I/O PMOS devices and 4.2V-VDS drain-extended NMOS is used to handle 3.6V+ voltages. The use of non-core devices leads to efficiency reduction. In [2] switched capacitor DC-DC converters are used. Although high conversion ratio capacitive converters typically have very low efficiencies, this design achieves a decent 74% efficiency by reducing parasitic capacitances via body-biasing. The design [3] utilizes soft-switching in a hybrid Dickson charge pump to achieve 92% conversion efficiency. But it achieves this largely due to the high-quality passives available in the flip-chip interposer design. Ref [4] uses resonant converters. This topology becomes increasingly complex for high conversion ratios. More recently [5] used a 4-level integrated buck converter. This design achieved 76% peak efficiency due to topological improvements and FDSOI. Multilevel converters are discussed in detail in [6] and their design methodology outlined in [7].

Clearly, an ideal DBS solution needs a large range of conversion ratios and should be able to handle a large load range. Prior solutions have had good efficiency but only in limited ranges. We propose a DBS solution that utilizes the optimal converter for each of the input-output ratios. In particular, we use three distinct modes of conversion. In the next section, we discuss the main features of our multi-mode DC-DC converter followed by its implementation details.

II. Multi-mode DC-DC converter

At full charge the unloaded output voltage for a Li-ion battery is 4.2V. As the battery initially discharges, the output voltage drops rapidly and then levels off to a nominal voltage of 3.6V when it reaches 10% discharge. It then maintains this

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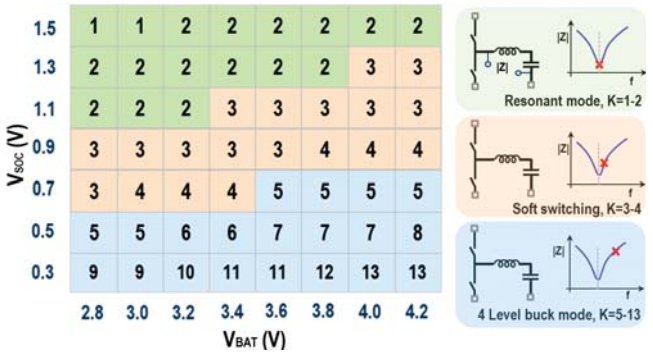

Fig. 2: Left -Variation of conversion ratio (K) vs V_{BAT} and vs V_{SOC}, Right -Different modes of the proposed multi-mode DC-DC converter

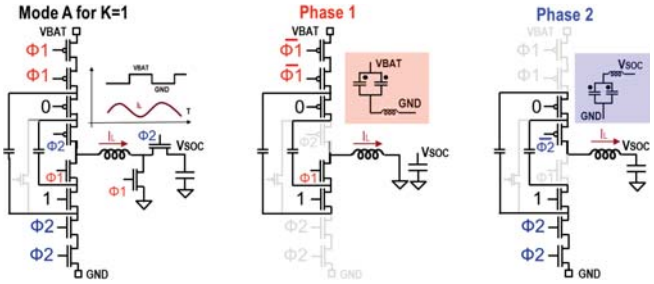

Fig. 3: Phase-wise resonant mode circuit operation for K=1.

voltage from 10% discharge to nearly 90% discharge. After this point the battery voltage reduces again and is considered to be fully discharged at $V_{BAT} = 2.8V$. In summary, for a constant discharge rate, 10% of the time is spent from 4.2V to 3.6V, 80% of the time is spent at 3.6V and a final 10% of the time is spent from 3.6V to 2.8V. So, the efficiency at 3.6V is most critical but good conversion efficiencies at both lower and higher voltages extends the usage time by 20%.

A DBS solution needs to handle the full range of input voltages from 4.2V to 2.8V. Quite often integrated on-chip voltages are reduced to improve power efficiency, particularly for digital circuits via DVFS (dynamic voltage and frequency scaling). To accommodate both the battery voltage variation (4.2V to 2.8) and the load voltage variation (1.5V to 0.3V) a wide range of DC-DC conversion ratios (K) (between 1 to 13) are needed as shown in the 2-D matrix in Fig. 2-left.

To efficiently realize the full range of conversion ratios in CMOS, we have developed a triple-mode hybrid (capacitive & inductive) DC-DC converter that we call multi-mode DC-DC converter. The right-hand of Fig. 2 shows the three converter modes (resonant, soft-switching and 4-level buck) that are

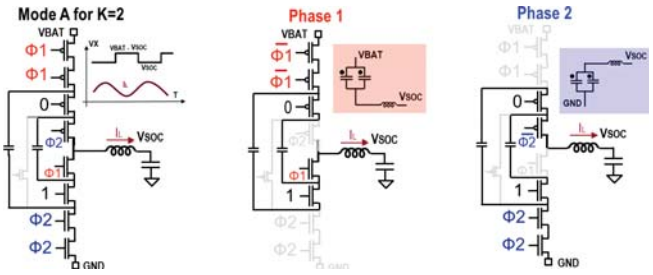

Fig. 4: Phase-wise resonant mode circuit operation for K=2.

utilized for the different conversion ratios. The resonant mode is used for K=1 and K=2, i.e., this conversion ratio is used when the battery voltage is low and the output voltage is high. Soft-switching is used for K=3, and K=4 and the 4-level buck converter is used for K=5-13. During the resonant mode (42-54MHz), the output tank impedance is at a minimum. During soft-switching (≈60-100MHz), we are operating from and above resonance where the output tank smoothes the capacitive current and during the 4-level buck mode (100-200MHz), the output tank looks mostly inductive from the converter perspective. Next, we describe the three modes of operation in more detail.

A. Resonant

This mode is used for conversion ratios of 1 and 2. In this mode, the output capacitor (2x500pF) and inductor (11nH) are resonant at 48MHz. Nearly, resonant behaviour is enjoyed between 42MHz and 54MHz. In resonance, the inductor current is nearly-sinusoid. The converter R_{OUT} is independent of capacitance and switching frequencies, unlike in switched capacitor converters, thus, boosting the efficiency. As shown in Fig. 3, for the K=1 mode, the series combination of inductor and capacitor is switched between V_{BAT} and gnd nodes at the switching frequency. The top two core-PMOS switches have their gate clock level varying between V_{BAT}-to-V_{BAT}/2 and V_{BAT}/2-to-0 respectively thus protecting them from breakdown. For the K=2 mode, the series tank oscillates between V_{BAT} and V_{SOC} as shown in Fig. 4.

B. Soft-switching

This mode is used for conversion ratios of 3 and 4. In this mode, we switch at 60-100MHz, which starts near resonance frequency of 48MHz and continues above. So, the converter is essentially a switched-capacitor DC-DC converter but with an inductor in series. The series inductor reduces the peak current that flows through the capacitors and switches which reduces the conduction loss as they are proportional to $I^2 \times$

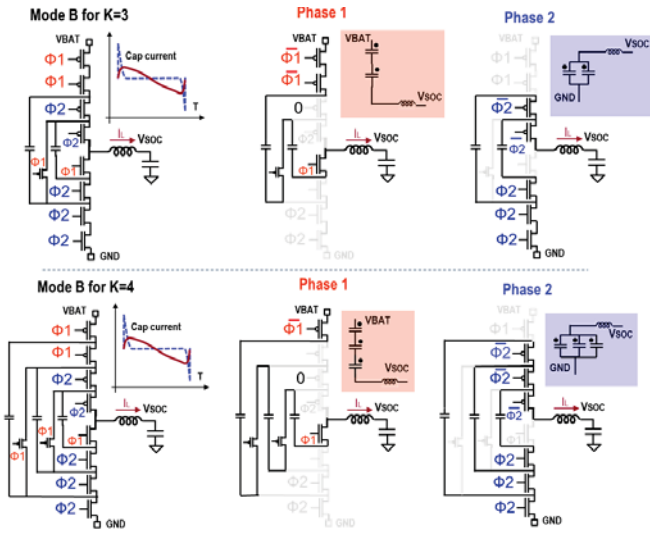

Fig. 5: Soft-switching mode circuit operation. Peak capacitor currents reduced.

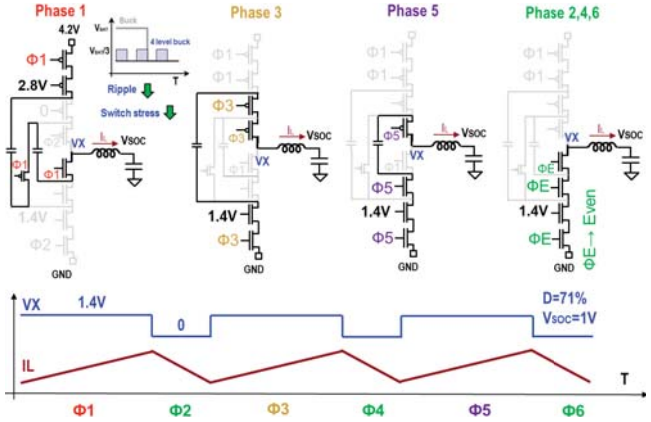

Fig. 6: Circuit operation during the multi-level buck converter mode.

R_{switch}. Fig. 5-top shows the switch waveforms during the two phases in this mode for K=3. The core-MOS switches get the appropriate logic-voltages to avoid breakdown. Fig. 5-bottom shows the case for K=4. The design procedure for this mode is based on findings in [6].

C. 4-level-buck

This mode is used for conversion ratios of 5-13 (Fig 6). In this mode, we use a switching frequency that varies between 100MHz and 200MHz, which is higher than both resonance and soft-charging. In this mode, we modify the operation of a normal buck converter by introducing 4 voltage levels as compared to 2 levels in a conventional buck converter [7]. Fig. 6-top-left shows the conceptual difference in voltage levels of a normal buck converter and the 4 level buck converter. In this design, the PWM bulk converter can select from two of four voltage levels (0V, 1.4V, 2.8V, and 4.2V). The multiple levels are provided by capacitive voltage division. Fine output voltage regulation is provided by duty cycle control. By toggling between smaller voltages, the output ripple is reduced and so is the voltage stress across switches. Fig 6-bottom shows the switching waveform in six phases for a full duty cycle for an overall conversion ratio of $(V_{BATT} = 4.2V)/(V_{SOC} = 1V)$. In this figure, the multi-level buck toggles between 1.4V and 0 and utilizes a 71% duty cycle for the PWM.

III. Proposed Architecture of Mutli-mode DC-DC

This section describes the implementation details of the proposed multi-mode DC-DC converter.

A. Architectural details

Fig. 7 shows the block diagram for the multi-mode DC-DC converter. As the figure shows, a 13-level modified-ADC selects the mode of operation of the multi-mode DC-DC converter. The output of the modified-ADC goes to the digital FSM based mode-selector block. The mode-selector block controls the drivers of the power cores (based on the digital control-word input from digital PID controller). The drivers provide the switching signals to the 3-mode power core. The 3 mode power core consists of switches and capacitors in such a fashion that based of the signals from mode-controller

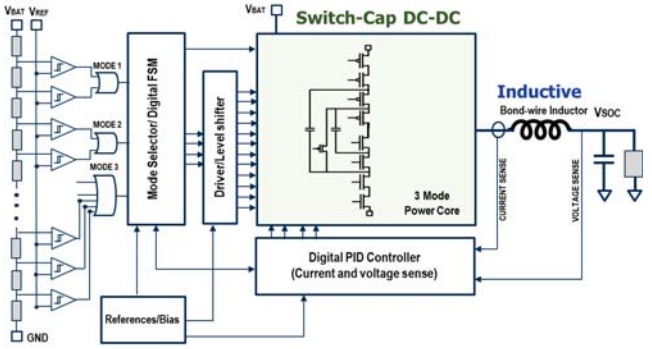

Fig. 7: Overall architecture of the proposed multi-mode DC-DC converter facilitating DBS in standard CMOS

block, it can configure itself to any of the three DC-DC converter modes. The topology for the circuit connections is shown inside the 3-mode power core block in Fig. 7. The inductor in this design is an in-package bond-wire. It provides an inductance around 11nH. The switching frequency varies from 42MHz to 200MHz based on the mode of operation (48-54MHz for mode A (resonant), 60-100MHz for mode B (soft-charging), and 100-200MHz for mode C (4-level-buck)). The converter handles load currents from 0.5mA-200mA.

B. Voltage regulation control of muti-mode DC-DC

The proposed multi-mode DC-DC converter functions in three distinct modes of power conversion so it needs to have three different control schemes to regulate both the input and output voltages. We support a load range of 0.5mA to 200mA for the output voltage range of 0.3-1.5V.

The resonant mode uses dead time control for voltage regulation. The output current and thus the resulting output voltage is regulated by modulating the dead-time between phases 1 and 2 in Fig. 3. This modulation changes the average current supplied to the load by keeping the system in resonance. More details of this can be found in [4]. The control mechanism for the soft charging is based on designs in [6]. Since this mode is fundamentally very similar to conventional switched capacitor DC-DC converters, we use conventional hysterical control similar to [8]. Finally, for the 4-level buck mode, we use a traditional buck converter duty-cycle PWM control mechanism. To have more stable control in this mode both current and voltage feedbacks have been implemented thus reducing the order of the overall system and improving the transient response. For all three modes the control type is selected digitally via a state machine as shown in Fig. 7.

IV. Measurement Results

Fig. 8-left shows the measured efficiency-Vs V_{BAT} characteristics for three levels of load current at a fixed output voltage of 1.2V. We observe the peak efficiency region is in the resonant mode for 10mA of load. At lower load currents, the efficiency drops due to the constant bias losses. At much higher currents I^2R losses increase. As we move to higher battery voltages for the fixed SOC voltage, we enter the soft charging switch-capacitor DC-DC mode (indicated as

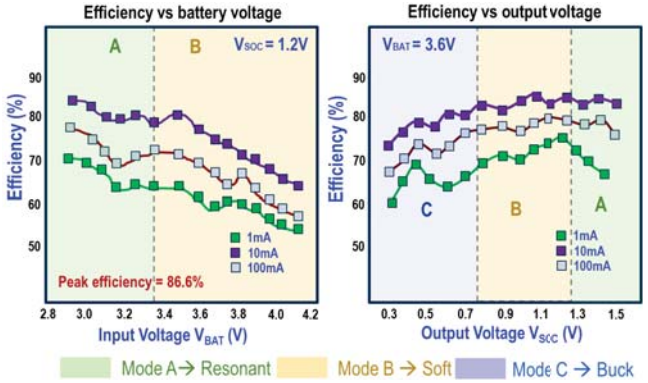

Fig. 8: Left- Efficiency Vs battery voltage VBAT for three current levels at fixed output voltage. Right-Efficiency Vs output voltage VSOC for three current levels at fixed battery voltage

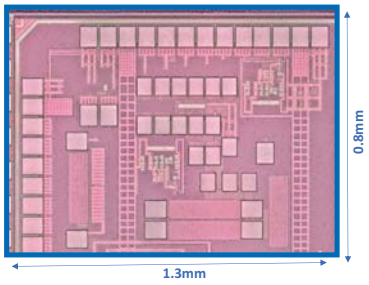

Fig. 9: Chip micrograph of the proposed multi-mode DC-DC

region-B). The efficiency drops for the three load currents as compared to the resonant mode. However, we note that the efficiency is near its peak value at $V_{BAT} = 3.6V$ where the system spends a majority of its time. Fig. 8-right shows the efficiency vs output voltage for three load currents at a fixed input battery voltage of 3.6V. Fig. 9 shows the chip micrograph of the design. The total active area is $1.3 \times 0.8mm^2$. Fig. 10a shows the transient response of the multi-mode DC-DC converter. The undershoot and overshoot recovery for a 10mA-100mA transient is 45.5nS and 23.62nS @1.2V output voltage respectively. The voltage droop is 40mV for the undershoot case. Fig. 10b shows a nearly sinusoidal inductor current in the resonant mode with a pk-to-pk current of 58mA. We pass a copy of inductor current through a test resistor for this measurement. The output voltage range is the highest in comparison to any published works as indicated in TABLE I. Our peak efficiency is 86.6%, second only to the flip-chip based design which uses better quality interposer based passives. Additionally, [3] uses a 20X larger inductor and a 2000X higher capacitor value. We have an improvement of 2X in the output voltage range compared to [3]. Also, the power range is larger than all other 65nm designs [2], [3].

V. Conclusions

We present a multi-mode DC-DC converter for direct battery to silicon power transfer in a single conversion stage. It uses three operating modes, resonant for K=1-2, soft charging SC for K=3-4 and 4 level buck converter for K=5-13. We use core devices for all the switch stacks to improve efficiency. The measured peak efficiency is 86.6% in the resonant mode.

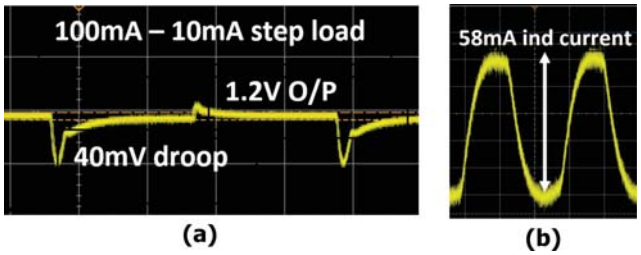

Fig. 10: Left-Transient o/p voltage measurement at Vin=3.6V, Vout=1.2V, load step=100mA to 10mA. Right- Inductor transient current in resonant mode, Iload=100mA

TABLE I: Comparison summary with related works

	[1]	[2]	[3]	[4]	[5]	**This**
Technology(nm)	45	65	65	180	28	**65**
Input(V)	2.8-4.2	3-4	3.0-4.5	3.6	2.8-4.2	**2.8-4.2**
Output(V)	0.6-1.2	1	0.3-1	1.8	0.6-1.2	**0.3-1.5**
O/P range	2X	-	3X	-	2X	**5X**
Cap(nF)	2000[1]	18/3.9[2]	44000	1.67	-	**0.5**
Inductor(nH)	10000	-	180	15	3	**11**[1]
Topology(mA)	B	SC	D	R	4-B	**Multi**
Peak Eff%	87.4	74.3	94.2	85	76	**86.6**
Max Pwr(mW)	100	115		1300	40	**300**
Pwr-Max/Min	5000X	50X[3]	100X[3]	250X	4000X	**400X**
Area (mm2)	4	0.64	4	7.2	1.5	**2.2**

[1] Offchip, [2]18nF-fly cap, 3.39nF-out, [3]approx

It handles a load range of 0.5-200mA at a peak power density of 0.3W/mm^2. The system was designed in TSMC's 65nm GP.

VI. Acknowledgments

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