A 0.4–1.0 GHz, 47 MHop/s Frequency-Hopped TXR Front End With 20 dB In-Band Blocker Rejection

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***Abstract*— In this paper, we present a prototype ultra-fast hopping spread spectrum transceiver front-end that realizes 20 dB of processing gain in the RF before any amplification occurs along the receiver chain. This means that a narrow-band in-band interferer is rejected by 20 dB before the low noise amplifier (LNA). The correlation function at RF is made possible by using a passive mixer-first receiver architecture that is driven by an ultra-fast hopped local oscillator (LO) signal. The 47 MHop/s LO is generated using an all-digital oscillator circuit that is followed by a memoryless digital-to-analog converter (DAC). The prototype chip fabricated in a Taiwan Semiconductor Manufacturing Company (TSMC) 65 nm RF CMOS process occupies 3.1 mm^2 of active area. The receiver and the transmitter each consume ≈25 mW from a 1 V power supply.**

***Index Terms*— Correlator, digital oscillator, fast frequency hopping, *N*-path, processing gain, spread spectrum, transceiver.**

I. Introduction

DIRECT sequence spread spectrum (DSSS) techniques form the core of code division multiple access and is primarily used for multiple accesses in civilian applications. DSSS techniques are able to spread in-band jammers by the processing gain and have been exploited by military communication systems for in-band jammer immunity. Traditionally, direct sequence processing is done at baseband frequencies, such that the RF front end can still be overloaded by in-band jammers. More recently, direct sequence processing has been attempted at RF frequencies to improve in-band jammer resilience [1], [2].

Frequency-hopped spread spectrum (FHSS) techniques have traditionally been used for secure and resilient communications. Conventionally, FHSS systems avoid blocking signals by completely avoiding their frequency of operation. However, this requires blocker identification to continue communications. In addition, any in-band blocker would eventually end up jamming the active front-end circuits. Currently, the fastest FHSS systems operate at a maximum of one symbol per hop [3]. FHSS schemes, in theory, have the capability of suppressing in-band jammers if a single symbol is spread over multiple hops. Unfortunately, this has traditionally not been possible due to the limited transient response of phase locked loop (PLLs). In particular, the transient response of PLLs, while hopping from one frequency to another, is limited by the filter loop bandwidth. Given a loop bandwidth that is 1/10th of the input reference frequency and approximating the settling time as four time constants, the maximum hop rate for a 30 MHz input reference frequency PLL is limited to 75 kHop/s [4].

Conventional FHSS systems are classified as either slow hopping or fast hopping depending on the number of symbols transmitted per hop. Slow-hopping FHSS systems transmit multiple symbols per hop, while the traditional fast-hopping FHSS systems transmit the same symbol during one or more (but usually limited to two or three) hops. This handful of hops is usually done to provide frequency diversity and is not intended for blocker rejection. Hopping speeds for slow-hopping systems are usually limited to a few kHop/s, while that for fast-hopping systems is limited to about 200 kHop/s [3]. The ultra-fast FH design presented here (architecture shown in Fig. 1) is able to hop at 47 MHop/s and provides 20 dB of processing gain at RF that improves the in-band blocker suppression by the same amount. For 20 dB of processing gain, the system uses 100 hops per symbol.

The ultra-fast hopping transceiver front end discussed in this paper provides the 20 dB of processing gain at RF. Thus, the blocker is rejected before any amplification occurs in the receiver chain. Two issues have been addressed to make this system possible. First, a circuit architecture is introduced that enables the correlation to be performed at RF. This circuit is able to perform the correlations in extremely short periods of time that has not been possible prior to this work. Second, low-power local oscillator (LO) circuits are designed that can hop extremely fast. Simultaneously solving both these issues has been critical to making ultra-fast hopping with processing gain at RF possible.

Series *N*-path *band-stop* filters have, sometimes, been used to suppress in-band blockers [5]. However, they suffer from poor linearity, limited jammer rejection and require *a priori* knowledge of the exact location of the blocker in the

Manuscript received November 23, 2018; revised February 15, 2019 and March 29, 2019; accepted April 1, 2019. Date of publication May 22, 2019; date of current version June 26, 2019. This paper was approved by Guest Editor Kaushik Sengupta. This research was funded in part by the DRAPA SPAR Program under Grant HR0011-17-2-000. *(Corresponding author: Naser Mousavi.)*

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Digital Object Identifier 10.1109/JSSC.2019.2911407

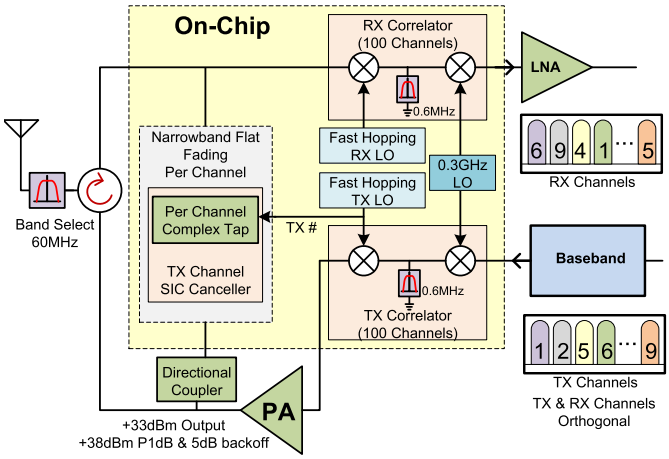


Fig. 1. Ultra-fast frequency hopping transceiver front-end architecture.

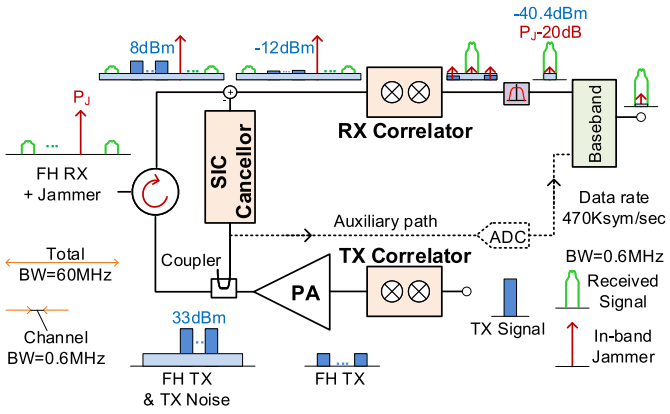


Fig. 2. Receive, self-interference, and jammer signal flows through the system.

frequency domain thus, requiring power hungry spectrum sensing techniques. In addition, these circuits become power hungry and complex with multiple LOs, one for each jammer, when attempting to suppress multiple blockers at the same time. Furthermore, as these filters operate in-band, they need to be very narrow so as to not reduce the usable signal. Narrow-band N-path notch filters require extremely large on-chip area to minimize the bandwidth. In our design, however, utilizing low-power ultra-fast circuit architectures, multiple blockers can be suppressed without any *a priori* knowledge of their frequency content. Like other designs, any out of band blockers can be removed using well-known on/off chip techniques [6].

The ultra-fast front end was presented in [7]. Here, we expand on it and provide additional details. A prior generation was described in [8]. The rest of this paper is organized as follows. Section II discusses the system-level design, Section III provides the circuit details, Section IV provides the measurement results, and conclusions are drawn in Section V.

II. System Design

The architecture for the ultra-fast FH system was shown in Fig. 1. Next, we clarify system operation and provide system specifications, followed by additional details of the receive and transmit correlators, the self-interference cancellation circuit, and the fast-hopping LO generators.

A. Transceiver Specifications

The design specifications for this transceiver are based on the requirements of the DARPA SPAR (Signal Processing at RF) program [9]. However, the design is flexible and easily programmed digitally for different processing gains or different hop rates within circuit limits. In addition, the RF center frequency is programmable via the clock input. The current system is designed to be bolted on to the front of the traditional fixed-frequency RF transceiver. Therefore, the receiver (RX) and transmitter (TX) correlators have both a down-converter and an up-converter. For the design shown in Fig. 1, the fixed-frequency RF transceiver is assumed to be at 300 MHz. However, this frequency is completely flexible. In addition, the system can be redesigned so that the FH RF is converted directly to the RX baseband and the TX baseband is directly up-converted to an FH TX signal. In which case, the second mixer at 300 MHz in Fig. 1 can be eliminated. For the rest of this paper, the architecture in Fig. 1 will be assumed.

The transceiver can operate with a center frequency that ranges between 0.4 and 1.0 GHz. The transceiver operates in a 60 MHz "band," which is divided into 100 "channels" that are each 0.6 MHz wide. The spacing between the channels (channel spacing) is 0.6 MHz. The receiver and the transmitter hop between these channels with a hopping speed of 47 MHop/s, i.e., a hopping time of 21 ns, to enable a maximum symbol rate of 470 KSymbol/s for a processing gain of 20 dB. Both the transmitter and receiver paths operate in this 60 MHz band, but the transmit and receive systems never operate on the same channel to minimize self-interference. The transmitter completes 100 hops for each data symbol, spreading the signal power into the 60 MHz band. This means that the power in each channel is now 20 dB (10log(100)) smaller than the original non-hoped signal, i.e., the processing gain is 20 dB. On the receive side, the signal power from each channel is added back together to recreate the original 0.6 MHz unspread signal.

The overall system operation is best understood with the help of Fig. 2 that shows the signal flow through the system. It is easiest to follow the signal by starting at the transmitter. The modulated TX signal is FH by the fast-hopping TX correlator (blue). This signal is amplified by the 2-W off-chip power amplifier (PA) (33 dBm). The PA adds broadband noise (light blue). A portion of this signal (-25 dB down) couples through the duplexer to the RX (now at $+8$ dBm). The RX sees the FH RX signal (green) plus a narrow-band CW in-band jammer (red). The self-interference cancellation (SIC) block partially cancels (by 20 dB) the FH TX leakage at the receiver (now at -12 dBm). This signal then passes through the RX correlator where the FH RX sees 20 dB of processing gain while the jammer is spread by 20 dB. A filtered version of this signal is sent to the baseband where any residual out of channel signal is removed.

As mentioned earlier, the TX and RX channels are orthogonal, and the amount of the TX channel power that shows up in-band in the receiver channel is a function of the TX and RX channel separation and the filtering capabilities of

the N-path-based correlators. The residual TX signal after the SIC is orthogonal to the RX LO and, hence, gets reduced by the correlator. Due to the ultra-fast hopping speed of the transceiver, the rejection is limited, and a portion of this power shows up in the receiver channel. The sinc filter response caused by the fast hopping has its first null at the hop rate of 47 MHz. Therefore, there is still significant TX energy in the RX channel. The transmitted signal over one symbol can be written as shown in (1), where $P[t]$ is the rectangular pulse, T_h is the hop time, N is the total number of channels, f_{T_i} is the transmit frequency at the ith hop, and $\Phi_T(i)$ is the necessary phase at the ith hop at the transmitter to ensure continuity between the frequency hops

$$x(t) = \sum_{i=1}^{N} P[t - (i-1)T_h]\sin[2\pi f_{T_i} t + \Phi_T(i)]. \quad (1)$$

The signal at the receiver then is given by (2), where f_{R_i} is the receive frequency and $\Phi_R(i)$ is the necessary phase at the ith hop at the receiver to ensure continuity between the frequency hops

$$y(t) = \sum_{i=1}^{N} P[t-(i-1)T_h]\sin[2\pi f_{T_i} t + \Phi_T(i)]e^{j2\pi f_{R_i} t + \Phi_R(i)}. \quad (2)$$

The spectrum at the receiver can be estimated by performing the Fourier transform of (2), which can be written as shown in the equation in the following. Here, we note that the transmitter and receiver channels are distinct and that the final spectrum has a sinc shape that is proportional to the hop-time T_h. This means that even if RX and TX channels are different, there is still going to be spill over from TX to RX. The spacing between TX and RX frequencies alters the phase and the sinc magnitudes of each of the summation terms that fall in-band and changes the self-interference that shows up in the RX band. As the hopping speed increases, T_h decreases, which widens the sinc function that causes more energy to show up in the RX baseband. This problem is normally not seen at lower hopping speeds, as the sinc main lobe is much narrower. We have verified this phenomenon via numerical simulations and also via measurements as discussed later.

$$\begin{aligned} Y(f) = \frac{T_h}{2j} \sum_{i=1}^{N} & e^{-j(2i-1)\pi T_h (f - f_{R_i})} \\ & \times [\mathrm{Sinc}(T_h(f - f_{R_i} - f_{T_i}) \\ & \quad \times e^{j((2i-1)\pi T_h (f_{T_i} - f_{R_i}) + \Phi_T(i) + \Phi_R(i)} \\ & \quad - \mathrm{Sinc}(T_h(f - f_{R_i} + f_{T_i}) \\ & \quad \times e^{-j((2i-1)\pi T_h (f_{T_i} - f_{R_i}) + \Phi_T(i) + \Phi_R(i)}]. \end{aligned}$$

Our measurement results for the transmit signal seen at the RX channel for a ten-channel separation between the TX and RX show a 27 dB suppression of the TX signal. For the 8 dBm TX signal input at the antenna and 20 dB suppression by the SIC, this results in a -40.4 dBm self-interference in the RX channel, as shown in Fig. 2. The broadband TX noise signal can be suppressed in the digital baseband using an axillary path as in [10] and is not included in this prototype. In the case of the PA, the primary limitation is that since the TX correlators are before the PA, the PA needs to be able to pass the fast hopping signal, i.e., it has to be sufficiently broadband. Not surprisingly, broadband PAs are normally less power efficient than high-Q narrow-band PAs.

B. Receive Correlator

The receive correlator consists of two passive four-phase mixers. N-path mixers use passive switches and a 25% duty cycle clock generator (for four-phase). These are "digital-like," in which they do not have any memory and can switch frequencies instantly. The only element that maintains memory is the baseband filter capacitor. As long as the RF and LO frequencies are synchronized, the memory element effectively only sees signals close to dc. The mixer on the left that is synchronized to the received signal de-spreads and down-converts the desired signal to baseband. At the same time, the mixer also spreads out any narrow-band blockers that may exist in-band. The de-spread signal is then filtered out to remove any out of band interference. In our design, the de-spreading/processing gain is 20 dB. The blocker is also reduced by the same amount. The reason for the processing gain is that the receiver only sees the blocker once every 100 times, effectively reducing its power by a 100 times or 20 dB. The same thing happens when there are multiple blockers in-band, i.e., the receiver spreads the blockers such that the sum of the powers of the resulting spectrums that show up in the receive channel is 20 dB down. Note that the spreading and filtering/averaging of the blocker occur in the current domain, which means that large voltage swings due to the interferer are avoided.

The resulting baseband signal is then up-converted to a fixed-frequency RF. As discussed previously, the reason for this up-conversion is that the front end can be added to any commercial off-the-shelf (COTS) transceiver, which also allows us to exploit the excellent noise figure of COTS low noise amplifier (LNA).

C. Transmit Correlator

The transmit correlator down-converts the fixed-frequency transmit signal with the mixer to the right and up-converts it back to RF using the fast-hopping LO signal. Similar to the receive correlator, the double mixer structure makes this correlator suitable for use with COTS transceivers. The fixed-frequency mixers in the receive and transmit correlators may be removed for an integrated solution.

The hopped transmit signal is then amplified using a broadband linear PA. An example broadband PA that meets our specifications is given in [11]. The PA is operated with 5 dB backoff to insure linear operation. The 33 dBm PA output power is fed to the antenna using an off-chip circulator. This output power enables the transceiver to support a range of 1.5 Km for the 3 GPP suburban channel model, assuming that 30 dBm power is radiated from the antenna. The transmit correlator is placed before the PA to relax its power handling requirements. However, this means that a high-Q narrow-band PA may not be used, as it will ring during channel hopping.

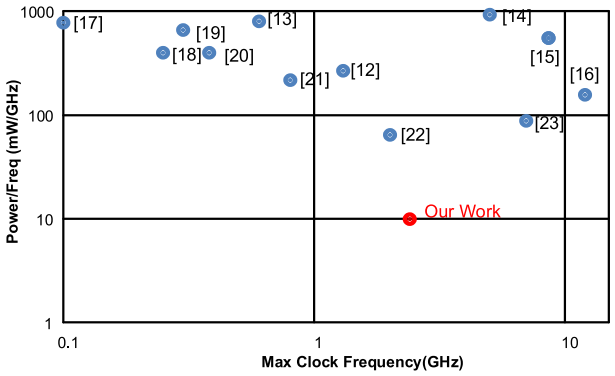


Fig. 3. DDS versus DO power consumption and maximum clock frequency (see [13]–[24]).

D. Self-Interference Cancellation Circuit

Part of the large transmit signal at the PA output leaks into the receiver side due to the finite isolation of the front-end circulator. Assuming 25 dB-isolation [9], the self-interference can be as large as 8 dBm at the input of the receive correlator and limits its linearity. The SIC circuit (SIC canceller) is therefore added to cancel a part of this signal. The circuit is placed after the PA so that any signals due to the PA nonlinearity are also canceled. It does not consume dc power and does not degrade receiver noise performance. The design is based on the same principles as those described in [12] but differs in implementation.

The PA noise is also attenuated by the circulator and shows up in the receive band. The total in-band noise is given by the integration of the attenuated PA noise in a 0.6 MHz band, which is very small in our design and does not limit the performance. For designs where the PA noise is an issue, an extra auxiliary path can be added to cancel the PA noise in the baseband. Previous works have demonstrated 20 dB of cancellation [10].

E. LO Signal Generator

A potential approach to generate the ultra-fast hopping signals is to use a direct digital synthesis (DDS). DDS circuits are designed to generate any custom periodic signal and therein lie its disadvantage. Here, our goal is to generate the LO signal only. The LO signal can be either a sine wave or a square wave (i.e., odd harmonics are not critical). In comparison to our design, DDS circuits consume significantly more power, as shown in Fig. 3. This can be intuitively explained due to the limited function required of the digital oscillator (DO), which generates a sine wave only, while DDSs are able to generate any type of periodic signal. In addition, due to its operational mode, the digital-to-analog converter (DAC) resolution in our signal generator can be of a lower resolution. The power consumption of our prototype in mW/GHz is an order of magnitude smaller than prior DDS designs.

In our design, the programmable LO signal is in the range of $f_{\rm clk}/4$, i.e., the oversampling ratio is only around two. We therefore require a reconstruction filter at the output of the DAC that removes the other unwanted harmonics. The digital

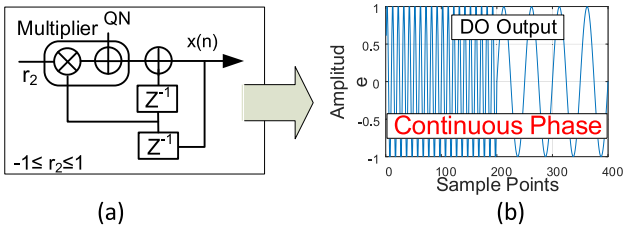


Fig. 4. (a) Structure of the digital oscillator with an additive quantization noise model. (b) DO output with continuous phase between frequency jumps.

oscillator is based on a design presented in [25]. The original design was made to drive a bandpass sigma-delta DAC and was designed for lower speeds. The improved version of the design is shown in Fig. 4 (left). The new design halves the number of multipliers and integrators, allowing it to operate at higher speeds. The center frequency is set by setting the value of r_2 in Fig. 9 (left).

The transfer function from r_2 to the output $x(n)$ for the DO in Fig. 4 is given by (3). Fig. 4 also includes a model for the quantization error in the DO and will be discussed later. The roots of the resulting characteristic equation give us the oscillating frequency. In particular, the input variable r_2 is limited from -2 to 2 to provide real values, and therefore, the poles can be written, as shown in (4). As a result, the precise output frequency can be simplified to (5)

$$x(n-2)+r_2x(n-1)+x(n)=0 \tag{3}$$

$$z_{1,2}=\frac{-r_2}{2}\pm j\sqrt{1-\frac{r_2^2}{4}}=e^{\pm {\rm j}\cos^{-1}(-\frac{r_2}{2})} \tag{4}$$

$$f_{\rm out}=\frac{f_{\rm clk}\cos^{-1}(-\frac{r_2}{2})}{2\pi}. \tag{5}$$

When $r_2=0$, $f_{\rm out}=f_{\rm clk}\cos^{-1}(0)/2\pi=f_{\rm clk}/4$. The output frequency range can be varied from near 0 to $f_{\rm clk}/2$.

1) Frequency Error From Computational Accuracy: The DO output frequency is determined by the value of r_2 and the input clock frequency. The frequency error is determined by the digital computation accuracy. The amplitude of the DO output is solely determined by the initial conditions of the two registers [25]. Next, we discuss the digital computational accuracy needed versus the frequency error of the digital oscillator.

Fig. 4 (right) shows the ideal output when floating-point computation is used. Note that the phase is continuous between frequency hops. Fixed-point computation is more suitable for low-power design, but finite computation resolution is likely to degrade the frequency accuracy. Our design uses 100 channels. Fig. 5 shows the frequency error in Hz for all the 100 channels versus the computation accuracy for a tuning range from $f_{\rm clk}/6$ to $f_{\rm clk}/3$. The computational accuracy is varied between 12 and 20 bits. For 16 bit computational accuracy, the maximum one-sided frequency error is 325 Hz, which corresponds to 0.84 ppm. Most wireless systems allow the crystal oscillator to have a maximum deviation of 10–20 ppm. We wanted to ensure that the DO did not contribute significantly to this. The computational accuracy is a compromise between frequency

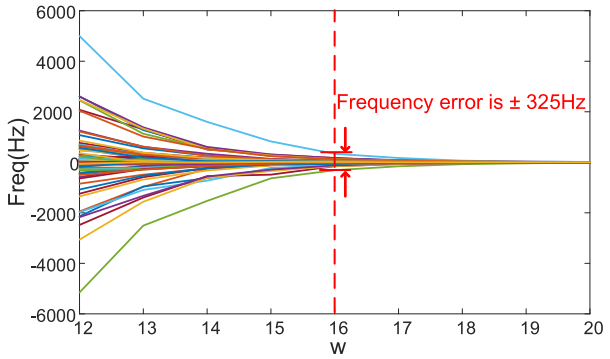


Fig. 5. Frequency deviation from ideal (frequency error) for all 100 channels versus computational accuracy.

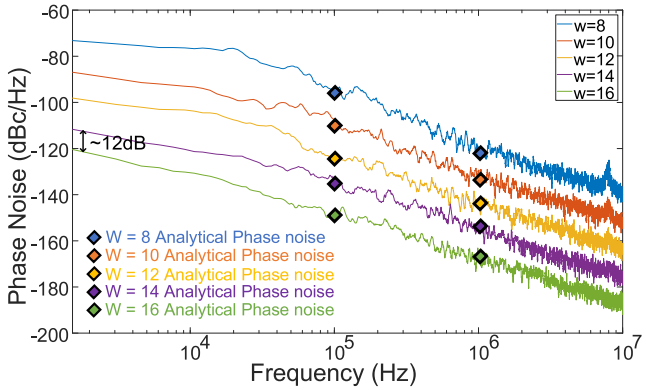


Fig. 6. Analytical model and numerical simulation for the DO phase noise.

error and power. The relationship between the frequency output and the clock frequency given in (5) is nonlinear, and therefore, for simplifying the design of the reconstruction filter and for the modeling of the quantization noise, we limit our r_2 input to lie between -1 and 1. All 100 channels lie within this input range. We maintain the same number of computation bits throughout the digital oscillator, i.e., the number of bits at the output of multiplier is the same as at the input. Therefore, choosing an r_2 value that is bounded by $+1$ and -1 allows us to simplify the design.

2) Phase Noise From Computational and DAC Accuracy: In a transceiver, the phase noise of the LO has significant impact on the error vector magnitude (EVM) and on jammer performance due to reciprocal mixing. The total phase noise will include the contributions from: 1) the input clock; 2) the digital oscillator; and 3) the LO DAC and injection locked oscillator (ILO) and duty cycle generators for the correlators. In this paper, we primarily focus on the contributions of the digital oscillator and DAC, as other contributors are well understood.

The DO model with quantization noise was shown in Fig. 4 (left), where the input coefficient to the DO, r_2, sets the oscillation frequency. Therefore, it stands to reason that the quantization noise due to finite computation accuracy will cause perturbations in the oscillation frequency, i.e., phase noise. The only contributor to quantization noise is the digital multiplier. In general, if two operations of w bits are multiplied, then the resultant can have a maximum of $2w$ bits. However, in our system, the output is also limited to w bits, as r_2 is limited by ± 1, which bounds the quantization noise.

The quantization noise distribution for a multiplier where one of the inputs is a constant is the same as the quantization noise from a regular quantizer (i.e., ADC). Thus, we can simplify our analysis by assuming that the quantization noise can be modeled as an additive white noise [26]. Using phase noise analysis methods similar to continuous-time LC oscillators [27], we developed an analytical model for the phase noise contribution of the computational accuracy of digital oscillators. We used this analytical model to derive the phase noise at 100 KHz and 1 MHz offsets for 8–16 bits of accuracy. These are shown as diamonds in Fig. 6. In Fig. 6, we plot the phase noise contribution of the DO separately by building a bit-accurate model of the DO in MATLAB (lines). For this simulation, we operate the DO with w bit resolution. The output is then down-converted to baseband using an ideal LO, and then, we perform an fast Fourier transform (FFT) on the low-pass filtered signal. We performed these simulations for multiple resolutions between 8 and 16 bits. There is good matching between the analytical model and numerical simulations validating our white noise assumption. Thus, the 16 bit accuracy required from a frequency accuracy perspective results in a DO-only phase noise assuming an ideal input source as -163 dBc/Hz at a 1 MHz offset. This is much lower than the phase noise at the DO output from the input source assuming an infinite accuracy of -144 dBc/Hz at a 1 MHz offset (discussed in Section IV). Thus, 16 bit accuracy was considered to be sufficient from both a frequency accuracy and phase noise perspective. The 16 bit fixed-point digital oscillator was implemented in Verilog and synthesized using a custom standard cell library in Taiwan Semiconductor Manufacturing Company (TSMC's) 65 nm technology.

The DO generates a binary sample-and-hold sinusoidal signal with W bit resolution. The DO output is then converted to the analog domain by a DAC. Because our goal is to hop rapidly between frequencies, we have to use a memoryless DAC, i.e., not a sigma–delta. The output from the M bit DAC is then filtered by an ILO with very high Q to remove the unwanted harmonics. Prior work has shown that ILOs can act as high-Q bandpass filters that can jump frequencies almost instantly [4]. The fast-hopping nature of the DO, the DAC, and the ILO enables the LO frequency to change almost instantaneously. The settling time is primarily limited by the digital circuits that provide the control signals.

III. Circuit Design

Next, we provide the circuit details for the above-discussed system blocks. In particular, we provide circuit details and simulations to validate our design selections for the correlators, the self-interference cancellation circuit, and the LO.

A. Transmit and Receive Correlators

The correlators are implemented as a set of four-phase passive mixers with 25% duty cycle clocks, which is shown in Fig. 7(a). The correlator design is essentially identical to an N-path structure except that the input and output mixers are operated at different frequencies. In an N-Path filter, both

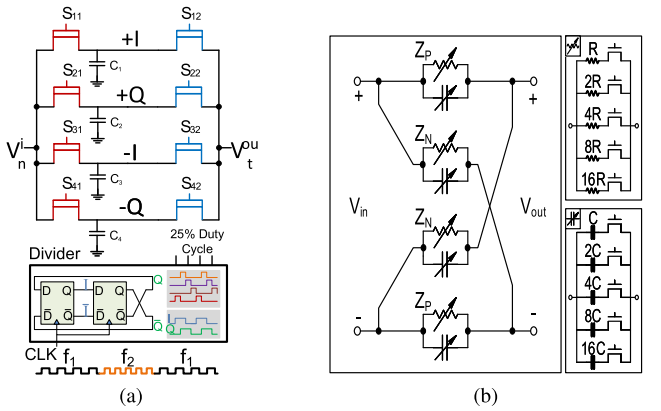


Fig. 7. Circuit details for (a) transmit and receive correlators and (b) self-interference cancellation circuit.

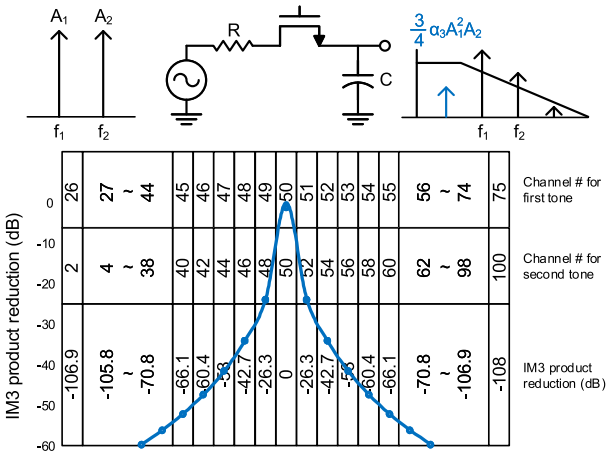


Fig. 8. Out-of-band IM3 product reduction due to baseband filter response.

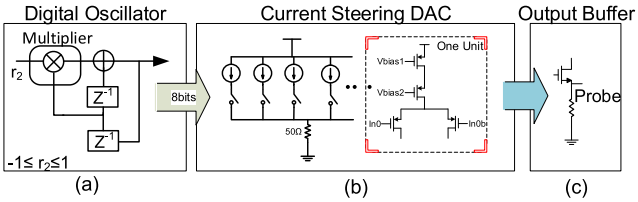


Fig. 9. (a) DO structure. (b) Current-mode 8 bit DAC. (c) Buffer included for testing purposes only.

mixers are operated at the same frequency, and usually, one is removed from the design for improved noise performance. Here, we maintain the dual-mixer format for flexibly and for improved out-of-band performance [5]. For the transmitter, the input mixers are connected to a fixed-frequency LO, and the other one is driven by an ultra-fast FH LO. The input data are down-converted to baseband from a fixed RF center frequency and up-converted back to RF using the fast-hopping LO signal. The same circuit is used for the receiver with opposite directions. When synchronized, the receive correlator down-converts the received hopping signal on the baseband capacitors. The received signal is then up-converted to a fixed frequency and further processed by a COTS receiver. The switches are implemented using 1 V RF nMOS devices, and they have 3 Ω series resistance when they are ON. The baseband capacitors are implemented using only MIM capacitors so that the linearity is only limited by the nMOS switches. The 25% duty cycle clocks are generated using a divide-by-two flip-flop loop and standard logic operations [5].

The correlator is an RF bandpass filter that changes the center frequency according to the LO signal. Hence, if two tones exist in-band, they will generate an third order intermodulation product (IM3) products that may fall in-channel. The low-frequency LTI model for N-path filters was presented and validated in [28]. We use this same model plus insight from [29] to develop an analytical model to evaluate the ratio between in-band third order intercept point (IIP3) and out-of-band IIP3 for our design. The simplified circuit model of a top-plate switch circuit is shown in Fig. 8 (top). The large jammer causes V_{GS} of the switch to vary [29]. As the frequency moves away from the channel center, the capacitor becomes more of a short reducing the signal amplitude of the jammers.

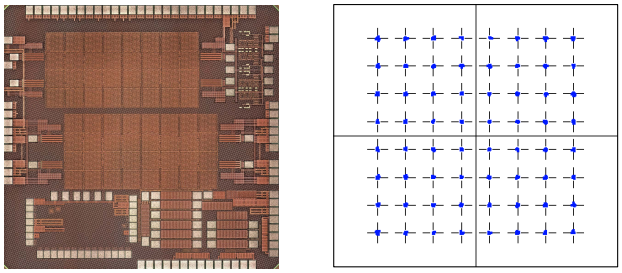
In our system, our channel hops but the jammers are assumed to be stationary. However, for a simpler analysis, we assume that our channel is stationary and the jammers hop. In our case, we have a total of 100 channels but only certain combinations of two tones fall in-band. The cases for which the IM3 products falls in the channel are shown in Fig. 8. The first row shows the channel number in which the first tone exists. The second row shows the second tone channel that results in an IM3 product, which falls in-channel. The suppression of the IM3 product due to the baseband filtering is shown in the third row. The IIP3 improvement compared with the in-band IIP3 is the average value of all the suppression values for the other 99 channels. This results in a 20.1 dB IIP3 improvement for output-of-band IIP3 in comparison with in-band IIP3. The calculations provided here are in reasonable agreement with the previously published results [29].

B. Self-Interference Canceller Circuit

Due to high PA power, the self-interference canceller circuit needs to be very linear suggesting a passive structure. The circuit should also have minimal impact on the noise figure (NF) of the receiver. As shown in Fig. 7(b), the circuit is implemented using resistors, capacitors, and switches and is similar to the design in [12]. The design in [12] uses an R-2R and C-2C ladder networks. We use binary resister and capacitor ratios. Both designs start with the NF consideration first. It can be shown that a 200 Ω resistor only degrades the NF by 0.5 dB when the receiver NF is 1 dB. This means that the smallest combination of the resistors in the circuit needs to be larger than 200 Ωs. The capacitors are then sized accordingly. The switches are located on the receive side where cancellation occurs, as they do not see large voltage swings. The circuit does not consume any DC power. Dynamic power is small due to slow reconfiguration speed which, at maximum, only operates at the hop rate.

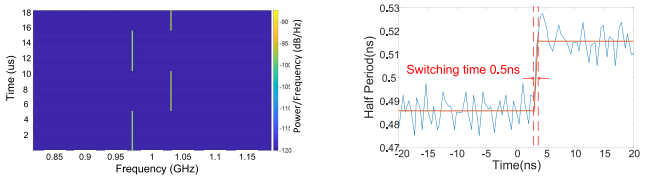
C. Ultra-Fast Hopping Signal Generator

The overall circuit design for LO generation is shown in Fig. 9, and the DO architecture has been discussed earlier. Next, we consider the impact of DAC resolution on



(a) (b)

Fig. 10. (a) Chip microphotograph. (b) Received 64 QAM signal.



(a) (b)

Fig. 11. (a) Frequency-hopping spectrogram used to measure the transient response of the correlator. (b) Measured TX correlator transient response. Only two hopping frequencies are shown here to ease transient response behavior.

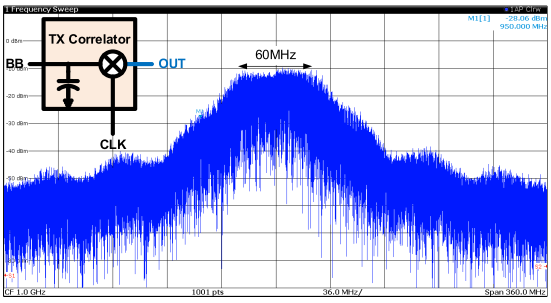


Fig. 12. Transmit correlator output spectrum for random FH LO.

the overall LO phase noise. The current-mode DAC puts out a finite resolution sample-and-hold analog value. Ideally, the finite quantization contributes broadband additive noise but does not directly cause phase noise. However, the broadband quantization at the DAC output can get converted to phase noise due to finite rise and fall times and due to the AM-to-PM conversion of the buffer or ILO that follows the DAC. To evaluate this contribution, we used the same test setup as the DO quantization but with varying DAC resolution. This simulation was done in Cadence using PNOISE where an equivalently shaped Gaussian noise model substitute was used for quantization noise to achieve convergence. The authors are aware that the probability density function of the two noise sources (quantization versus Gaussian) are different but the expected values and frequencies were appropriately adjusted and we expect that this should provide a good approximation. If we assume that the input clock is ideal and that the digital part of the DO generates no phase noise, then the phase noise contribution due to the AM-to-PM conversion of the 8 bit DAC alone at a 1 MHz offset is -136 dBc/Hz. Actual phase noise measurements will be a function of the phase noise from the source, the computational accuracy, and the contributions from the DAC AM-to-PM. The DAC system is being redesigned with a larger number of bits.

IV. Measurement Results

The design was fabricated in the TSMC's 65 nm RF-GP CMOS technology. The active area is 3.1 mm^2. The microphotograph of the fabricated chip is shown in Fig. 10(a). Next, we present measurement results for the various components of the system, i.e., the correlators, the DO, and the DAC. This set of measurements is followed by more system-level measurements, including TX to RX intended signal, TX to RX self-interference, and narrow-band jammer rejection.

A. Component-Level Measurements

First, we provide measurements for the fast-hopping critical components, including the correlator and the LO path.

1) Correlator Measurements: Fig. 11(a) shows a spectrogram of the transmit correlator while hopping between two frequencies centered at 1 GHz. For this and the next measurement, the LO signal that drives the output mixers of the transmit correlator is hopped, and the output of the correlator is measured using a 20 GSa/s R&S oscilloscope. Due to IF bandwidth limitations of our spectrum analyzer, transient response measurements are performed by using the time-domain sampled values of the output using a digital oscilloscope. The data are then taken to MATLAB, interpolated and filtered, and a spectrogram performed on the output. As can be seen, we clearly see the hopping pattern but it is difficult to measure the exact transient response time using the spectrogram.

To better evaluate the transient response, we estimate the instantaneous frequency by looking at the zero crossings of the time-domain signal. Fig. 11(b) shows the transient response of the transmit correlator to an abrupt frequency change in the LO signal. The time resolution using the zero-crossings method is limited to one half period, i.e., 0.5 ns when the output is centered at 1 GHz. The blue line shows the measured signal. The orange line shows the average of 200 data points. The perturbations in the measurement are due to the finite oversampling ($\approx$2) and the practical limitations of the interpolation. The measured settling time is 0.5 ns, which means that the correlator output frequency settles in less than 0.5 ns. This shows that the correlator is able to hop nearly instantly and the settling time is only limited to the fast-hopping LO that drives the correlator.

Fig. 12 shows the transmit output spectrum on a spectrum analyzer centered at 1 GHz. For this measurement, a dc input value was provided at the baseband for a fixed LO. The LO was then hopped randomly across all 100 channels to occupy a bandwidth of 60 MHz. Due to the divide-by-two circuit in the N-path LO generator, the external LO input was centered at 2 GHz and was hopped randomly to cover 120 MHz. In Fig. 12, we see the spreading of the single sinusoidal spread across the 100 channels providing 20 dB of processing gain.

2) DO and DAC Measurements: Next, we evaluate the combined DO and DAC transient performance. Fig. 13(a)

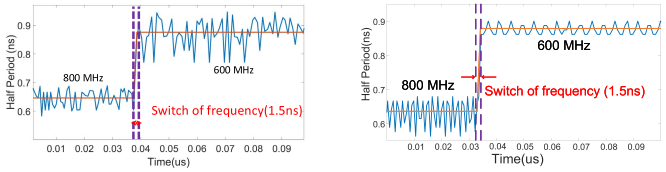


Fig. 13. Measured and simulated DO + DAC hopping speed. Only two hopping frequencies are shown here to ease the transient response behavior.

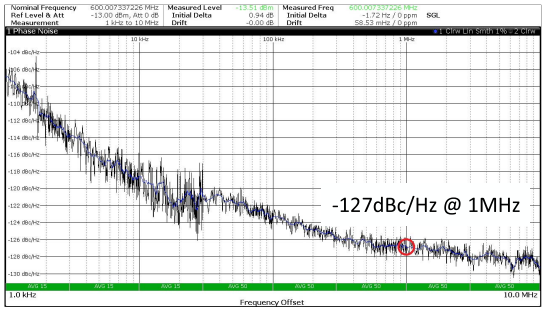


Fig. 14. Measured phase noise of the DO + DAC.

shows transient measurements for the combined DO and DAC. Specifically, Fig. 13(a) shows the hopping speed while hopping from 800 to 600 MHz and operating with a 2.4 GHz clock frequency. The simulated transient response of the DO only is shown in Fig. 13(b) for comparison purposes. To measure the fast-frequency-hopping speed, we sampled the DAC output with an R&S RS-RTO 1044 20 Gsps scope that interpolates the data to 100 Gsps. We used finite impulse response filters (to maintain the linear phase) to low-pass filter with 100 taps in MATLAB at the output of the DAC. As discussed previously, we estimated the frequency of the output by evaluating the zero crossings so the hopping speed resolution is limited by one-half period. The simulated DO output is processed in the same way. The signal is operating around a quarter of clock frequency, so there are only 3–5 data points for each period of the signal. The spline interpolation of the signal is not perfect, so the zero-crossing values are not absolutely accurate. This is the reason that the "half-period" as shown in Fig. 13(b) is not constant. The measured hopping speed matches well with the simulated DO hopping speed, which is 1.5 ns from 800 MHz switch to 600 MHz. This is about 1 clock period within our measurement resolution limits.

The measured power consumption for 1 GHz output from the DO+DAC combination is 6 mW, and the measured frequency accuracy of the output signal is better than 20 ppm, which is limited by the FFT resolution of the R&S RS-RTO 1044. As was shown in Fig. 5, the expected error was 0.84 ppm.

Fig. 14 shows that the measured phase noise for the LO path at a fixed frequency of 600 MHz is −127 dBc/Hz at a 1 MHz offset. The clock source phase used to drive the DO has a phase noise of −132 dBc/Hz at a 1 MHz offset. Since the DO output is roughly at $f_{\mathrm{clk}}/4$, the expected phase noise (for regular frequency divider) would have been 12 dB lower, i.e., −144 dBc/Hz at a 1 MHz offset. Experimental exploration

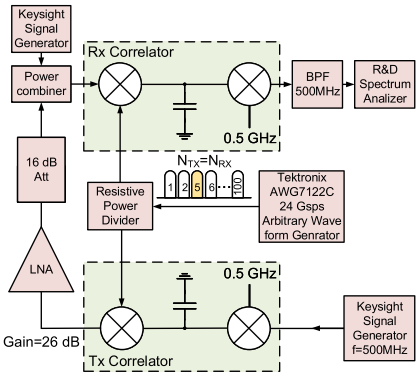


Fig. 15. Measurement setup used for TX → RX intended signal performance and for in-band jammer performance.

suggests that the phase noise deterioration is mainly due to the small-signal swing from the DAC output and due to the AM-to-PM conversion of the buffer that is only included for probing purpose. Specter simulations confirm that the buffer contributes −129 dBc/Hz phase noise at a 1 MHz offset, which is the dominant factor of the phase noise. Both designs are easily updated for improved performance. The 16 bit fixed-point resolution is used for the entire DO to minimize the phase noise and achieve the frequency accuracy, and only the most significant 8 bits are used in the DAC. The DAC resolution affects its tonal behavior, which, combined with quantization noise, is then partially converted to phase noise due to the AM-to-PM conversion of the output buffer.

B. System-Level Measurements

Now, we provide system-level measurements. In particular, we provide TX to RX intended signal performance, TX to RX self-interference rejection, and in-band jammer rejection.

1) TX to RX Intended Signal Performance: We use the same measurement setup for normal operation (TX → RX) and for jammer rejection. This setup is shown in Fig. 15, except that for normal operation, there is no added jammer. We use a signal generator to generate BPSK, QPSK, 16 quadrature amplitude modulation (QAM), and 64 QAM signals centered at 0.5 GHz. This signal goes through the TX correlator, centered at 1 GHz, which spreads the signal by 20 dB. The output of the TX correlator is followed by a 26 dB LNA and a 16 dB attenuator to isolate the TX from the RX. The extra 10 dB of gain compensates for test setup losses so the signal seen at the RX correlator is at −19.5 dBm. The RX correlator is synchronized with the TX correlator. The output of the RX correlator, centered at 0.5 GHz, passes through a 500 MHz bandpass filter with a filter bandwidth of 7 MHz and then demodulates using an R&S FSW 43 spectrum analyzer. The choice of the 0.5 GHz frequency for the fixed TX and RX mixers is due to the availability of the band-pass filter.

The fast-hopping LO is provided by an arbitrary waveform generator (AWG) for two reasons. First, as a mechanism to reduce risk, all the blocks in this chip tapeout were designed to be tested separately. In particular, the signal generator and the correlator were not connected together. Second, due to an

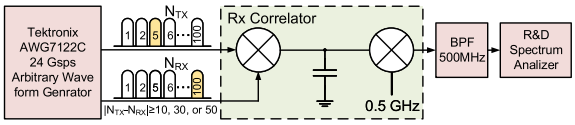


Fig. 16. Self-interference cancellation measurement setup.

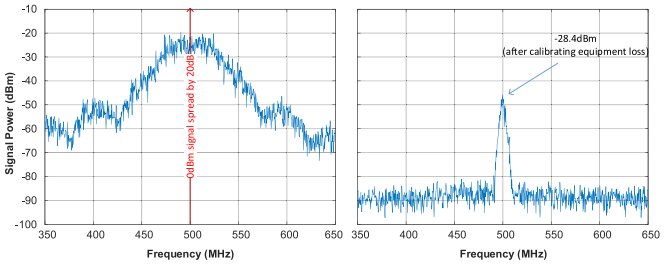


Fig. 17. Self-interference cancellation due to transceiver orthogonal operation.

error in the source follower buffer after the DAC, the output voltage from the buffer was not sufficiently large to run the correlators. Synchronization between the transmitter and the receiver is also important in the system where the problem gets worse with a wireless channel and mobility. This problem is likely to be exasperated with the high hopping speed of this design. The details of synchronization for this architecture are still ongoing research. As mentioned earlier, we are driving the correlators with an external AWG. Since we are assuming perfect synchronization, a single AWG is used for both receive and transmit. In a practical system, however, this correlates the phase noise of the TX and RX, which is unlikely to be correlated in a real system. To make sure that the TX and the RX are synchronized, LO paths were designed symmetrically and were connected together on chip. Also the delay between the TX and the RX was minimized using short cables.

For this measurement, no in-band jammer is added. Due to space limitations, only the 64 QAM signal is shown, here, in Fig. 10(b). The sensitivity measurements for the receive correlator were performed without hopping. The output of the receive correlator was fed directly to an R&S FSW43 spectrum analyzer with a pre-amp option. External input and output baluns were used. There are two differential mixers in the receive correlator. RF data were provided at 401 MHz with a 1 MHz offset to avoid LO feedthrough. The input and output mixers were operated at 400 MHz. The measured sensitivity after de-embedding for the baluns for QPSK signals at a symbol rate of 470 Ksps (600 KHz occupied bandwidth) was -95 dBm. The measured EVM was 6 dB, and assuming a 9 dB NF for the spectrum analyzer (-165 dBm DANL), the effective noise figure for the receive correlator is about 6 dB.

2) TX Signal Rejection in RX Channel: The receive and transmit correlators are operated at different channel frequencies at all times to reduce self-interference. However, due to ultra-fast hopping speed of the correlators in this design, some of the transmit signal shows up in the receive band. Fig. 16 shows the setup that is used to measure the self-interference cancellation. Fig. 17 shows the self-interference cancellation when minimum channel spacing is 30. In this case, the hopping sequence for the receiver is determined randomly using a

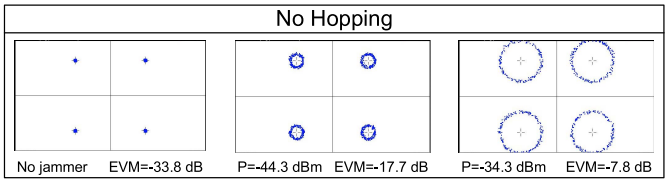


Fig. 18. Received signal constellation versus in-band blocker power when the RX and the TX are not hopping.

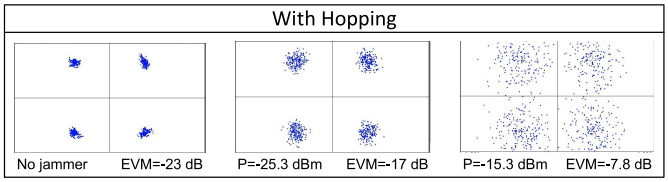


Fig. 19. Received signal constellation versus in-band blocker power when the RX and the TX are hopping. Note that we have attempted to keep the EVMs between the hopping and not hopping cases. Thus, the difference can be seen in the jammer power levels between hopping and not hopping.

TABLE I
POWER BREAK DOWN FOR THE SYSTEM

f_{RF} (GHz)	f_{clk} (GHz)	f_{dac} Output (GHz)	Power (mW)		
			DO+DAC	Correlator	Total
0.4	2.4	0.8	24	1.2	25.2
1	1.6	0.4	16+6(ILO)	2.6	24.6

uniform distribution, and then, another uniformly distributed random function is used to determine the transmitter hopping sequence with the condition that the transmit channel at any given time is at least 30 channels away from the receive channel. In this case, the total measured self-interference cancellation is 28.4 dB. The measured self-interference cancellation is 27.3 dB for ten-channel, 28.4 dB for 30 channel, and 33 dB for 50 channel separations confirming that TX→RX isolation improves only slight, as the channel spacing increases due to the sinc function introduced as a result of ultra-fast hopping. We have numerically calculated the rejection in MATLAB for a 10 MHz bandwidth (consistent with our measurements), which shows -27.7, -33.9, and -37.7 dB rejection for 10, 30, and 50 channel separations, respectively. For this simulation, two 500 MHz signals were generated that are hopped with different TX and RX sequences at 50 MHops/s and are multiplied to get the baseband component of the signal. The filter used in this simulation is an ideal low-pass filter. We think that the discrepancy between the simulated and measured results is likely due to a substrate or supply coupling and/or LO feedthrough that causes a leveling-off in the measurement results.

3) Jammer Behavior: We use the measurement setup in Fig. 15 for this test as well but, except in this case, we add an in-band jammer. The 20 dB processing gain of the receive correlator can also be seen when a narrow-band blocker exists in the receive band. The measured constellation at the receiver is shown in Figs. 18 and 19 versus the in-band blocker power for two cases. The top row shows the constellation versus blocker power when there is no hopping. The bottom row shows the constellation for when the transmitter and

TABLE II
COMPARISON WITH THE STATE OF THE ART

Reference	This work	[3]	[30]	[31]	[32]	[33]	[34]
Method	FHSS	FHSS	FHSS	FHSS	DSSS	DSSS	FHSS
Center frequency (GHz)	0.4-1.0	0.9	0.9	0.12	0.9-1.1	0.3-1.4	2.4
RF processing gain(N=10/100) (dB)[1]	10/19.4	0	0	NA	NA	NA	NA
In-band blocker rejection (N=10/100) (dB)[1]	10/19.4	0	0	NA	NA	NA	NA
NF (dB)[2]	6	NA	NA	NA	4-5	2.5-4	NA
Hop speed (MHops/s)	50	0.08	0.16	0.024	NA	NA	< 0.07
Hops/symbol	100	1	1	< 1	NA	NA	< 1
Power (mW)	24	NA	525	4.6	9.37	35	NA
RF TX SIC (dB)	33	NA	NA	NA	18.6	38.5	NA

[1] The signal power was set to -29dBm and the blocker power was varied from -50dBm to -15.3dBm.
[2] The NF of the correlator was measured without hopping. This measurement does not include the circulator noise.

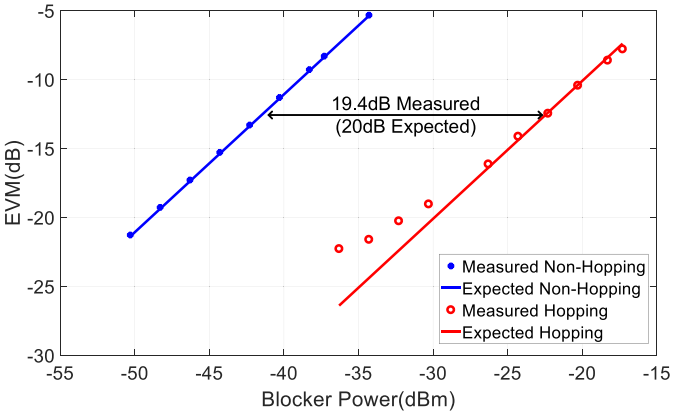


Fig. 20. EVM versus blocker power with 100 channels for two cases, i.e., hopping and not hopping.

the receiver hop with 50 MHop/s. The input signal is at -29 dBm. The EVM with no jammer is at -33.8 and -23 dB, which reduces to -7.8 dB for both cases. The blocker power difference is 19 dB, i.e., processing gain is 19 dB. In this setup, the TX/RX fixed LO is run at 300/500 MHz. This is to avoid influencing the measurements from the substrate and board coupling, which will happen if the TX and the RX have the same frequency. Also the data are fed to the TX at 301 MHz to avoid LO feedthrough and I/Q mismatch.

The EVM versus blocker power is shown in Fig. 20 for the two cases where the transmitter and the receiver are both hopping or both not hopping for the same jammer. The measurement setup is the same as in Fig. 15. The only difference is that the LO frequencies in the baseband side of the TX correlator was set to 0.4 GHz for this measurement. The data were fed to the TX correlator at 401 MHz to avoid LO feedthrough and I/Q mismatch. The red and blue lines show the EVM for hopping and non-hopping cases. As Fig. 20 shows, for the same EVM, blocker handling capability goes up by 19.4 dB. In other words, the blocker is rejected by 19.4 dB. The input power to the receive correlator is set to -29 dBm at each port. We have been also able to measure 20 dB processing gain when the signal is at a 5 MHz offset from the center frequency. The EVM rises linearly with the signal power and can be estimated as $\text{EVM} = 10\log(P_B/P_M)$, where P_B and P_M are the blocker power and the signal power, respectively. The level-off in the red circles in Fig. 20 is due to the limited EVM of the system when there is no blocker present. As was also seen in Figs. 19 and 18, there is an increase in the noise level with hopping. We are still investigating the reasons for this.

The spurs from the DO can also affect the blocker performance. The spurs that are out of band are not problematic since the front-end filter removes any out of band blockers. There is, however, a spur that is 50 MHz away and is due to the hopping of the DO at 50 MHops/s. This spur shows up at 25 MHz away from the LO after down-conversion, which would be in-band and is around -65 dB lower than the LO. Since the spur is much smaller than the LO, it does not affect the blocker performance.

4) Power Consumption: Table I provides details for the power consumption for two specific cases. In case 1, the RF signal is at 0.4 GHz, and the fundamental of the DAC output, at 0.8 GHz, drives the 25% signal generator without an ILO. The total power for TX and RX are 25.2 mW each. In case 2, the RF signal is at 1 GHz, and the first image of the DAC output, at 2 GHz$= f_{\text{clk}} + f_{\text{dac}}$, drives the 25% signal generator with an ILO. The total power for TX and RX are 24.6 mW each. The ILO (not included in this prototype) power is estimated at 6 mW from simulations. All other powers are measured.

C. Measurement Summary

Table II compares our design transceiver with previously published spread spectrum transceiver designs with a focus on FH implementations. Table II shows that our design is the only one that provides processing gain and importantly does this at RF. The processing gain translates into in-band blocker rejection as demonstrated using EVM measurements and as shown in Table II. The hopping speed is more than 312 times higher than the next fastest reported system [30]. Other systems hop at much lower speeds. For instance, [31] and [34] hop at 0.024 and 0.007 Mhops/s, respectively, assuming that the hopping speed is ten times the PLL settling time. This is the first FH system that spreads a single symbol over more than one hop and provides processing gain. In comparison to others, we have increased the number of hops/symbol by 100 times, i.e., 20 dB of processing gain [3], [30]. References [32] and [35] do not report the processing gain but report 18.6 and 38.5 dB of self-interference cancellation

compared with 33 dB for this design. These designs use DSSS techniques, which use the entire frequency band regardless of the specific code used. Because the total bandwidth occupied is large at all instances, DSSS techniques normally use rake receiver architectures to mitigate multipath fading. Rake receivers increase the complexity and power consumption of these architectures. On the other hand, for FHSS receivers, the occupied bandwidth is narrow at each instance simplifying multipath equalization. In addition, FHSS techniques inherit another advantage, i.e., once the jammer location is identified, the jammer frequency location can be avoided entirely [32], [33]. In our design, the random channel hopping behaves like a spectrum sensor where the jammer channel can be identified. The sensitivity of the correlator is −95 dBm, which translates into 6 dB NF for QPSK modulation at 470 KSps.

V. Conclusion

This paper presents the first ultra-fast hopping transceiver front-end architecture that provides 20 dB processing gain at RF. The front end is implemented in a 65 nm CMOS RF GP process and is made possible by two sub-circuits: first, an RF correlator that can change frequency in less than 0.5 ns in response to the LO and second, ultra-fast hopping all-digital signal generator that can hop in less than 1.5 ns. Even better performance is expected for scaled technologies due to the digital nature of the circuits. The 20 dB processing gain is realized by using 100 hopping channels. The processing gain can be increased with the number of channels used. The receiver is able to reject one or more blockers at the same time without any *a priori* knowledge of their frequency. With the jammer frequency information, the performance can be improved further by avoiding the jammer channel completely.

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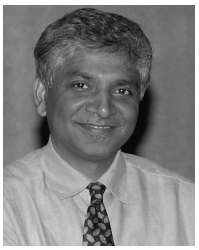

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