--- University of Minnesota ---

Department of Electrical Engineering

EE5333: Analog Integrated Circuit Design Fall 2019

Credits:	3	*Instructor:*	Ramesh Harjani
Time:	08:15 - 09:30 TuTh	*Location:*	Keller Hall 3-125
Office Hours:	09:40 - 10:30 TuTh	*Location:*	4-165 EE/CSci, 625-4032
	Office hour priority (in person, then telephone and then emails)		
Email:	harjani@ece.umn.edu		
Website:	**http://www.umn.edu/~harjani (follow the links on the left for classes)**		
VLSI Lab:	Keller Hall 1-200		

Class video: The class is also taped and available on video. For on campus students you can only view the video after 10 days of the lecture. However, you will have immediate access a week before finals week and a week before mid-terms. UNITE will keep the entire semester on the web and remove it on the day of the final.

Class audio: Same-day access to downloadable audio podcast for the class will be available to on-campus students

All students: those enrolled through UNITE and those enrolled in on-campus sections - will be able to access the audio podcasts and asynch video streams through the UNITE Media Portal at www.unite.umn.edu (they will be prompted for their University of Minnesota Internet ID and password).

Course Description: Design techniques for analog integrated circuits. The primary focus of this course is CMOS. Emphasis will be placed on the design of the fundamental circuits required for analog signal processing. Students will be expected to design and test several design problems. All students are expected to work on a sizeable project that comprises a significant percentage of the final grade. The objective of this course it to provide the basic design concepts and tradeoffs involved in analog integrated circuit design.

	Course outline:	*Book Chapters*	*Lecture Time (weeks)*
I.	Integrated-circuit devices and modelling	(chap 1)	1.0
II.	Processing and layout	(chap 2)	1.0
III.	Basic current mirrors and single-stage amplifiers	(chap 3)	1.0
IV.	Frequency response of electronic circuits	(chap 4)	1.0
V.	Feedback amplifiers	(chap 5)	1.0
VI.	Basic opamp design and compensation	(chap 6)	2.5
VII.	Biasing, references and regulators	(chap 7)	1.5
VIII.	Noise and linearity analysis and modelling	(chap 9)	1.0
IX.	Comparators	(chap 10)	1.0
X.	Discrete-time signals	(chap 13)	1.0
XI.	Switched-capacitor circuits	(chap 14)	2.0

Text: Analog Integrated Circuit Design, 2nd Edition
Tony Chan Carusone, David Johns & Ken Martin
John Wiley & Sons, Inc. 2011, ISBN: 978-0470770108
www.analogicdesign.com (has all the spice models & a long errata)

References: Design of Analog CMOS Integrated Circuits, 2nd Edition
Behzad Razavi
McGraw-Hill, January 2016
ISBN: 0072524936

Used books: http://www.abebooks.com/, www.amazon.com and our book store often has used books.

Homework Assignments:

LATE HOMEWORK WILL NOT BE ACCEPTED! Some of the homework assignments will require circuit simulation on the computer. Students will be expected to design and test one or more design projects. Initial designs will use LTSPICE for simulations. As the course progresses and depending on the progress of students we will move over to Cadence for circuit design and layout (Cadence support will be provided **only** by the TA if there is one). The purpose of the homework is to build upon your understanding of course concepts and to develop analog circuit design skills. The Institute of Technology makes Mathematica available to its students. Please, check http://it.umn.edu for more information.

Projects:

All along the quarter students are expected to work on a project of significant size. You are expected to work on a single project. As these projects make up a significant proportion of your final grade, students are advised to start thinking of topics for their final project immediately. All students have to design an opamp as their first project. You will have to complete circuit design, i.e., everything that is necessary to get your design fabricated at an IC foundry. More details about the project will be provided in a separate handout.

Computer use:

Students are expected to use LTSpice/Cadence for design problems. Directions for accessing LTSpice, Cadence tools & HSPICE are provided on the course website. Example designs are also provided for your convenience. Students are expected to either already know SPICE or are expected to learn SPICE on their own. It will not be explicitly taught in class. So if you do not already know SPICE, start learning it at the earliest. Take a look at the course website for information regarding introductions to SPICE.

Grading policy:

Homework assignments	15%
Midterm I examination	25%
Midterm II examination	25%
Project proposal	5%
Interim project report	10%
Final project report	20%

Exam timings:

Midterm I examination	Tuesday, Oct 29th (in class)
Midterm II	TBD

Project related dates:

Project proposal due	Thursday, September 26th
Interim project report due	Tuesday, November 5th
Final project report due	TBD