EE5940-2: VLSI Data Converter Design Spring 2016

Instructor: Ramesh Harjani
Class Time: 11:15 – 12:30 TuTh
Location: Keller Hall 3-111 (will also be on UNITE)
Office Hours: 1:00pm – 2:00pm TuTh
Prerequisites: EE5333/EE4111 or equivalent or instructor permission
Other information: The course will involve a design project that will require the use of the Cadence design tools or equivalent analog/digital VLSI design software.

This course covers the design of VLSI data converter design. After a brief introduction to sampling theory and quantization noise the course will focus on various Nyquist rate and oversampled converters. In particular, we will discuss flash, pipelined, successive approximation and sigma-delta converters. The course will involve a design project that will require the use of the Cadence design tools or equivalent analog/digital VLSI design software.

Course Outline

1. Introduction to data conversion
    a. Sampling, aliasing, quantization & reconstruction
    b. Data converter performance metrics
2. Sampling circuits & voltage comparators
3. Nyquist rate ADCs
    a. Flash, folding and interleaved converters
    b. Pipelined and algorithmic converters
    c. Successive approximation converters
4. Oversampled ADCs & DACs
    a. First order and higher order sigma-delta converters
    b. Bandpass and multi-bit converters
    c. CT sigma-delta converters
5. ADC power dissipation limits

Intended audience and assumed background

The objective of this course it to provide the basic background to design VLSI analog-to-digital and digital-to-analog converters and special circuit design techniques needed for low power design. This course is intended for practicing engineers and students who are interested in understanding the basics of modern day data converter. It is assumed that the audience will have a basic understanding of *analog CMOS design* and *probability and statistics* at the level of an undergraduate in an engineering or scientific discipline.

Books & References:

There is no required book for this course. However, material for this course will be provided in a reader (slides will be provided online) and selected from publications in IEEE papers and from a number of other reference books. The primary books from which material will be selected include:

1. *The Data Conversion Handbook,* edited by Walt Kester, 2005 (available as a book or online at http://www.analog.com/library/analogDialogue/archives/39-06/data_conversion_handbook.html

2. *Data Converters*, Franco Maloberti, Springer, 2008
   (available via Springerlink- While on campus or logged in via vpn go to www.lib.umn.edu and search for the book. You have online access to the complete book.)
3. *Understanding Delta-Sigma Data Converters*, Schreier & Temes, Wiley IEEE Press 2005 (This is currently the best book for oversampling converters)

Class Video & Audio:

The class is also taped and available on video. For on campus students you can only view the video after 10 days of the lecture. However, you will have immediate access a week before finals week and a week before mid-term exams. UNITE will keep the entire semester on the web and remove it on the day of the final. Same-day access to downloadable audio podcast for the class will be available to on-campus students. All students: those enrolled through UNITE and those enrolled in on-campus sections - will be able to access the audio podcasts and asynch video streams through the UNITE Media Portal at www.unite.umn.edu (they will be prompted for their University of Minnesota Internet ID and password).

Homework:

LATE HOMEWORK WILL NOT BE ACCEPTED! Some of the homework assignments will require circuit simulation on the computer. Students will be expected to design and test one or more design projects. Students are expected to use Cadence for circuit design and layout (No Cadence support will be provided). Some of the hand calculations can get quite complex and so it is recommended that you get hold of some symbolic analysis program on a computer. The purpose of the homework is to build upon your understanding of course concepts and to develop analog circuit design skills. The Institute of Technology makes Mathematica available to its students and those in other colleges that pay the IT Technology Fee. Please, check http://www.oit.umn.edu/utools/ for more information.

Homework:

All along the quarter students are expected to work on a project of significant size. You are expected to work on a single project. As these projects make up a significant proportion of your final grade, students are advised to start thinking of topics for their final project immediately. You will have to complete circuit design and layout, i.e., everything that is necessary to get your design fabricated at an IC foundry. More details about the project will be provided in a separate handout.

Grading:

Midterm I 25%, Final 35%, Homework 10%, Project report 20%, Interim Project Report 10%

Exam Timings:

Midterm I examination	Tuesday, March 22nd
Midterm II / Final examination	TBD