EE8337: Analog Circuits for Wireless Communications

Design Project
Important Dates: Part 1 of the project due date: **March 9th, in class**
Part 2 of the project due date: **Last day of class, Thursday May 4th, 5pm.**

A major portion of your grade in this course will come from your final project. For this course the entire class will work on an RF frontend. The RF frontend will consist of a common gate LNA, a mixer and 1st state of IF.

The design will be done using a 45nm process (or alternate process – please check with me regarding the process you are going to use). Parameters for this process are listed on the website. Models for inductors will be provided soon. Students in class are responsible for only the blocks listed within the red dashed box. The project will be broken up into three parts. For the 1st part of the project everyone will design an LNA. You can assume that a bandgap reference is available for your use.

Part1:

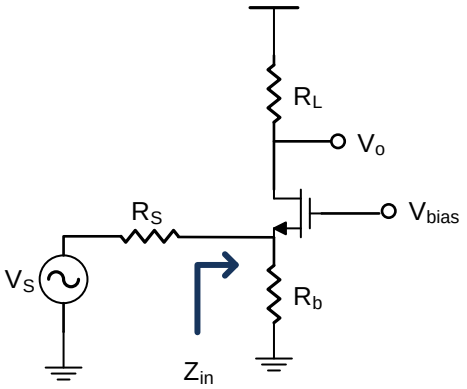
Design the LNA to meet the following specs

- Topology = Common gate LNA
- Differential design
- Vdd = 1.2V
- Zin = 50 ohms, CL=0.2pF (this is the load on the LNA output due to the mixer)
- RF frequency 2.4GHz to meet 802.11g specs
- Power gain = 20dB
- IIP3 = -20dBm (for IIP3 use two tones that are 20MHz apart). IIP2 > +10dBm
- NF max = 1.5dB
- Total DC power < 1.2mW
- Extra credit will be provided for trying new topologies and more aggressive specs

Other parts of the project and specs for them will be updated as the class progresses. Part 1 of the project is due by **the date given above**. You can use either HSPICE or SPECTRE RF for the design of your LNA though SPECTRE RF is preferred. Use an inductor Q=6 for L <10nH and Q=5 for L<20nH. Assume that the capacitor Q=30. Transmission lines have an impedance between 20ohms to 70ohms. Assume a Q=20 for integrated T-Lines. More details models for inductors will be provided later.

Use the book as a good starting point for the project. Sections 5.3.3, 5.3.5, 5.4 should be useful for the project. Start with 5.3.3 for the first part, start with a current bias and a resistive bias. Remember to minimize power. Also remember there is a receiver frontend design in Chapter 13, particularly Section 13.2.1.

a) First design a simple common gate LNA as shown below. The biasing circuit is not shown here. Please, refer to Razavi, Chap 5 for a design example of how to do the biasing. Make sure to include the biasing network as it can affect the NF if not done correctly. Make sure to design a fully differential version of the circuit. Only the single-ended version is shown below.



b) For the second part replace the simple design with a capacitively connect gm-boosted design. Please, refer to the reference below [1] for addition information. The biasing for this design should be very similar to the common-gate LNA described in class. Please, compare the NF, power and IIP3 with the version done in part (a).

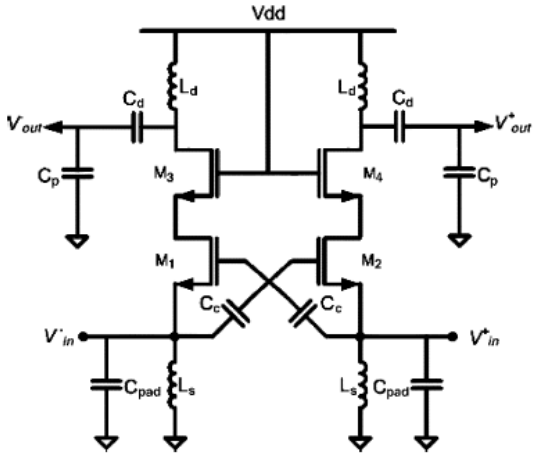


Fig. 5. Complete capacitor cross-coupled differential CGLNA stage.

For your final 6 page report in IEEE conference format please include a table of design specs vs simulated values. Make sure all your figures are clearly visible. All device sizes should be included in your final schematic.

For ideas on how to perform simulation on your LNA in Cadence please search for "LAB-2 (Tutorial) Simulation of LNA (Cadence SpectreRF) Rashad Ramzan" on google

[1] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. Pineda de Gyvez, D. J. Allstot and E. Sanchez-Sinencio, "", IEEE Transactions on Circuits and System II: Express Briefs, Vol 52, No 12, Dec 2005, pp 875-879.