The Impact of Hot Carriers on Timing in Large Circuits

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***Abstract*—This paper focuses on hot carrier (HC) effects in large scale digital circuits and proposes a scalable method for analyzing circuit-level delay degradations. At the transistor level, a multi-mode energy-driven model for nanometer technologies is employed. At the logic cell level, a methodology that captures the aging of a device as a sum of device age gains per signal transition is described, and the age gain is characterized using SPICE simulation. At the circuit level, the cell-level characterizations are used in conjunction with probabilistic methods to perform fast degradation analysis. The proposed analysis method is validated by Monte Carlo simulation on various benchmark circuits, and is proved to be accurate, efficient and scalable.**

I. Introduction

Hot carrier (HC) effects in MOSFETs are caused by the acceleration of carriers (electrons or holes) under lateral electric fields in the channel, to the point where they gain high enough energy and momentum (and hence they are called *hot* carriers) to break the barriers of surrounding dielectric, such as the gate and sidewall oxides [1]. The presence of hot carriers triggers a series of physical processes that affects the device characteristics under normal circuit operation. These effects cumulatively build up over prolonged periods, causing the circuit to age with time, resulting in performance degradations that may eventually lead to circuit failure.

The phenomenon of HC effects is not new: it was a significant reliability issue from the 1970s to the 1990s, when circuits operated under high supply voltages (2.5–5V), which led to a high lateral electric field in the MOSFET channel. The effects of HCs were mitigated by the introduction of special process techniques such as lightly doped drains (LDDs). The traditional theory of HC mechanisms was based on a field-driven model, in which the peak energy of carriers (electrons or holes) is determined by the lateral field of the channel [2]. This was based on the theory of the so-called lucky electron model, capturing the confluence of events due to which an electron is "lucky" enough to do damage – to gain energy from the channel field, to be redirected towards the silicon/oxide interface, and to avoid energy-robbing collisions along the way.

Extrapolating this theory, it was expected that at today's supply voltages, HC effects would almost disappear as carriers cannot gain enough energy when the electric field is reduced to these levels. However, experimental evidence on nanoscale technologies shows that this is not true, and hot carrier degradation remains significant for MOSFETs at lower voltages [3]. Moreover, these issues are projected to get even worse in future generations of devices.

The rate of hot carrier generation increases as $t^{1/2}$. Since the multiplicative constant is relatively small, in the short-term, it is overshadowed by bias temperature instability (BTI) effects, which increase as t^n, for $n \approx 0.1$–0.2, but with a larger constant multiplier. However, in the long term, the $t^{1/2}$ term dominates the t^n term, making HC effects particularly important for devices in the medium to long term. It has been shown in [4], for example, that HC effects contribute to 40-80% of all aging after 10 years of operation. Therefore, HC effects contribute significantly in the short term and are dominant in applications with longer lifetimes, such as embedded/automotive applications and some computing applications.

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Recently, newer energy-driven theories [5]–[7] have been introduced to generalize the ideas of the lucky electron model, and to explain the mechanism of carriers-induced degradation for short-channel devices at low supply voltages. These theories have been experimentally validated on nanometer-scale technologies. The energy-driven framework includes the effects of electrons of various levels of energy, ranging from high-energy *channel hot carriers* (CHCs) to low-energy *channel cold carriers* (CCCs). Under this model, injection is not necessary for the device degradation, and carriers with enough energy can affect the Si–SiO_2 interface directly. However, much of the published circuit-level work on HC effects is based on the lucky electron model, which is effectively obsolete.

Existing work on HC degradation analysis of digital circuits can be divided into to two categories. The first is based on device-level modeling/measurement tied to circuit-level analysis, including [8], commercial software such as Eldo using computationally-intensive simulations, and [4], which predicts the lifetime of a ring oscillator using measured data. While these methods are flexible enough to accept new models, they are not scalable for analyzing large circuits.

Methods in the second category are based on a circuit-level perspective, using statistical information about device operation to estimate the circuit degradation. In [9], a hierarchical analysis method for delay degradation, based on a simple device-level HC model, was proposed. The work in [10] defined a duty factor to capture the effective stress time for HC effects, which assumes constant HC stress during signal transitions and models the duty factor to be proportional to the transition time. The characterization of HC degradation is performed in the device level and only considers the switching transistors, with other transistors in the stack ignored. Then signal probability (SP) and transition density (TD) is utilized for aging analysis. While these works are usually efficient and scalable to large digital circuits, they use over-simplistic models for device aging and cell characterization, and therefore cannot achieve the high accuracy provided by methods in the first category, especially for nanometer-scale technologies. Extending these methods to energy-driven models, including CHC and CCC, is highly nontrivial, and is certainly not a simple extension.

This paper provides a third path for CHC/CCC degradation analysis for large digital circuits, and makes the following contributions:

- Instead of using a simple empirical degradation model [9], or a device model assuming constant stress during transition [10], our method is built upon the newer multi-mode energy-driven degradation model [6], [7].
- It introduces the novel concept of age gain (AG) to capture the amount by which a transistor ages in each signal transition, and develops a quasistatic approach for accurate analysis of AG.
- It performs cell-level characterization of AG, in which the AGs of all transistors in a logic cell corresponding to a signal transition event is computed simultaneously, instead of only considering switching transistors [10].
- It utilizes signal statistics, leveraged from techniques for power estimation, to perform circuit-level degradation analysis. The multilevel hierarchy of modeling and analysis enables both high accuracy and great scalability of the proposed approach.

- It demonstrates that the circuit delay degradation has a slight but negligible deceleration effect due to the degradation of signal transition, in contrast to the significant acceleration effect predicted in [10]. The work in [10] assumes HC aging to be proportional to the transition time, which increases with aging; however, this is incorrect since slower transition times excite fewer energetic carriers and actually cause *less* damage.

Our work bridges the wide chasm between the tremendous advances at the device level with the much simpler models that are currently used at the circuit level. Our approach maintains accuracy and scalability at all levels of design, employing accurate modeling and characterization at the device and cell levels, and a scalable algorithm at the circuit level. At the *transistor level*, we employ the energy-driven model for device aging [6], [7], as outlined in Section II. At the *logic cell level*, we characterize (offline) the device age gain per signal transition for cells within a library using SPICE simulations, as described in Section III. At the *circuit level*, the signal probability and activity factor are utilized to perform fast degradation analysis, based on the cell-level characterization, as explained in Section IV. The proposed analysis method is validated by Monte Carlo simulation on various benchmark circuits, and is demonstrated in Section V to be accurate, efficient and scalable. The paper ends by presenting concluding remarks in Section VI.

As in other work considering hot and cold carriers, we refer to the CHC/CCC problem under all energy modes as "hot carrier"/"HC" degradation, but it is implicit that the CCC case is also included.

II. CHC/CCC Aging: Device Models

A. Traditional Mechanisms

The traditional lucky electron model for HC degradation was based on *direct electron excitation* (DEE), i.e., the theory of impact ionization and interface trap generation due to broken Si–H bonds [1], based on a set of chemical reactions. Let us denote the silicon-hydrogen bonds at the surface as $\equiv \mathrm{Si}_s\mathrm{H}$, where the subscript s denotes the surface, i.e., the oxide-substrate interface, with three other bonds ("$\equiv$") connected to other silicon atoms in the substrate, One of the reactions that causes HC injection involves trap generation by electrons (e^-) that breaks the silicon-hydrogen bond, i.e.,

$$\equiv \mathrm{Si}_s\mathrm{H} + e^- \quad \rightarrow \quad \mathrm{Si}^* + \mathrm{H} \tag{1}$$

Another is related to trap generation by electrons and holes (h^+) as they interact with hydrogen atoms (H) and molecules (H_2), i.e.,

$$\begin{aligned} e^- + h^+ + \mathrm{H}_2 \quad &\rightarrow \quad 2\mathrm{H} \\ \equiv \mathrm{Si}_s\mathrm{H} + \mathrm{H} \quad &\rightarrow \quad \mathrm{Si}^* + \mathrm{H}_2 \end{aligned} \tag{2}$$

It is also possible for holes to break the $\equiv \mathrm{Si}_s - \mathrm{H}$ bound.

B. Energy-driven Mechanisms

From an energy perspective, hot electrons change the distribution of the electron energy distribution function (EEDF). The expression

$$\text{Rate} \; = \int f(E)S(E)dE \tag{3}$$

describes the hot carrier rate, where f, the EEDF, and S, the interaction cross section or scattering rate, are functions of energy E. It has been shown that the dominant energies associated with this integrand are at a set of "knee" points in either f or S. There are four major mechanisms that affect the above rate [5], [6]:

- In the field-driven paradigm of the lucky electron model, f has no significant knee, and the dominant energies are driven by the S function. This is the first mechanism, and its effect is decreasing in nanometer-scale technologies.
- In addition, there are knees in the EEDF beyond the range of the lucky electron model. It has been shown that the EEDF has a significant knee at the point at which there is a steep potential drop at the drain, corresponding to the potential from the drain to the channel pinch-off point, V_{EFF}, and a second knee is seen at about $2V_{EFF}$ due to *electron-electron scattering* (EES).
- The third mechanism, linked to high-energy carriers, is through *single vibrational excitation* (SVE) due to energy transfer to the phonon system, adding to energy from lattice vibrations.
- Finally, there is evidence that the bonds may be broken by *channel cold carrier* (CCC) effects, through a fourth mechanism corresponding to *multiple vibrational excitation* (MVE). This corresponds to direct excitation of the vibrational modes of the bond by multiple carrier impacts, each of which individually have low energy, but which can cumulatively break the bond [11]. MVE degradation is strongly correlated to the current, i.e, the number of electrons "hitting" the bond per second.

The energy-driven theory for HC generation [6] uses quantum-mechanical models to explain the process of carriers gaining energy, through three different mechanisms: (1) *High-energy channel hot carriers* based on direct electron excitation (DEE), consistent with the Lucky Electron Model (LEM), and on the SVE mechanism, (2) *Medium energy electrons* based on the EES mechanism, and (3) *Channel cold carriers* based on the MVE mechanism, which creates lower-energy carriers that cause degradations.

C. Device Aging Model

The degradations of the saturation drain current, $\Delta I_{\text{on}}/I_{\text{on}}$, of a transistor due to HC effects follow a power model [7]:

$$(\Delta I_{\text{on}}/I_{\text{on}})_j = A(\text{age}_j)^n \tag{4}$$

The exponent n is widely accepted to be 0.5 over a range of processes. The value of A can be obtained from device-level experiments, e.g., from the plots in [7]. The age function of a MOSFET is given by

$$\text{age} = t/\tau = R_{\text{it}}t \tag{5}$$

where R_{it} can be interpreted as the *rate of aging* over time, and corresponds to the rate of interface trap generation. The quantity τ is its inverse and is referred to as the device lifetime. Over the years, considerable effort has been expended in characterizing R_{it} at the device level. Under the classical field-driven LEM scenario, this has the form:

$$R_{\text{it(LEM)}} = \frac{1}{\tau} = K\left(\frac{I_{ds}}{W}\right)\left(\frac{I_{bs}}{I_{ds}}\right)^m \tag{6}$$

The more accurate multi-mode energy-driven model for HC degradation for fine-geometry CMOS devices changes this to [7]:

$$\begin{aligned} R_{\text{it}} = \frac{1}{\tau} \quad = \quad & C_1\left(\frac{I_{ds}}{W}\right)\left(\frac{I_{bs}}{I_{ds}}\right)^m + C_2\left(\frac{I_{ds}}{W}\right)^{a_2}\left(\frac{I_{bs}}{I_{ds}}\right)^m \\ & + C_3\, V_{ds}^{\frac{a_3}{2}}\left(\frac{I_{ds}}{W}\right)^{a_3}\exp\left(\frac{-E_{emi}}{k_BT}\right) \end{aligned} \tag{7}$$

The three terms in the expression correspond to degradation in the high-energy mode (corresponding to LEM), the medium-energy mode, and through channel cold carriers, respectively.

The relation between R_{it} and I_{ds}/W in Equation (6) is linear, and experimental data [6], [7] show that this is grossly incorrect. The nonlinear model in Equation (7) shows excellent fits to experimental measurements, and therefore our analysis is based on this model.

HC degradation has positive dependence on temperature, and a corner-based approach with worst-case temperature is used in this work. If more information about thermal characteristics is available, this model can easily be extended.

III. Cell-level Characterization

The device-level models outlined in the previous section provide a means for computing the aging due to CHC/CCC effects. To determine their effects on the circuit, our approach begins by building a cell-level characterization technique for the standard cell library that computes the delay drift over time. The remainder of this section describes the precharacterization method: we begin by determining the aging effect on each transistor of a library cell, and then compute its effect on the cell delay.

A. Transistor Age Gain Per Transition

For most of the time during the operation of a digital circuit, the MOS transistors in the circuit are in off or triode state, where there is minimal HC degradation. The period during which there is a sufficient number of carriers in the channel, with various levels of energy, corresponds to only the active (switching) state, and it is sufficient for only this state to be considered in analyzing HC degradation at the transistor level.

Therefore, HC aging does not occur over all time, and the defect generation rate function in Equation (7) becomes time-varying, and can be written as $R_{\text{it}}(t)$. Fig. 1 shows the $R_{\text{it}}(t)$ of the NMOS transistor in an inverter with a rising input signal: notice that the value is zero outside the transition, and varies over the period of the transition. The active state of a logic cell can be characterized using the input signal transition time and output load capacitance. For example, a faster transition results in higher-energy carriers, while a slower transition to a larger load may result in a larger volume of lower-energy carriers.

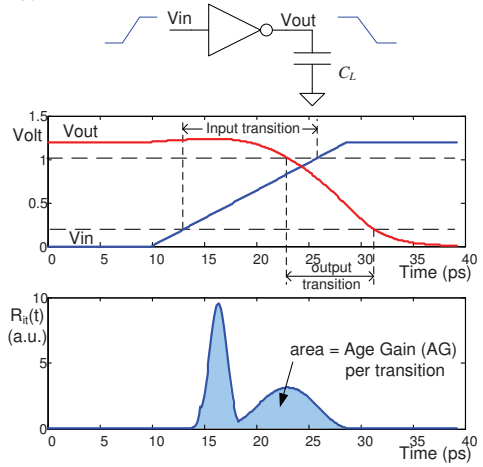

Fig. 1. An example that shows the age function, $R_{\text{it}}(t)$, during a signal transition of an inverter.

It is important to note that, unlike NBTI, HC effects do not experience recovery effects, and the application of HC stress results in monotone aging. We introduce a term, called the age gain (AG) per transition of a MOSFET, to capture the effect of degradation due to HC aging as a result of each transition that the MOSFET undergoes. The age function, which increases monotonically over the life of a device, is the sum of AGs of all transitions:

$$\text{age} = \sum_{\text{all transitions}} \text{AG} \tag{8}$$

We compute the AG using a a quasistatic approach: such methods have been accepted for HC analysis [12]. With this approach, the device AG over each transition period with time-dependent aging rate is computed as the integral of the aging rate function $R_{\text{it}}(t)$, as shown below,

$$\text{AG} = \int_{\text{tran}} R_{\text{it}}(t)\text{dt} \tag{9}$$

Here, tran stands for the interval of a specific transition, and $R_{\text{it}}(t)$ is defined in Equation (7) with time-dependent operation voltages and currents. The integral computes the age gain associated with one specific transition and uses the quasistatic approach to approximate the integral as a finite sum.

B. Library Characterization

For a digital circuit, the AG calculations can be characterized at the cell-level as a part of library characterization. Under a specified input signal type (rise or fall), a transition time, and an output load capacitance, the time-varying voltages and currents of all MOS transistors inside the logic cell can be computed using SPICE transient analysis. The AG of each transistor is computed by the numerical integration of $R_{\text{it}}(t)$ in Equation (7).

Examining the procedure outlined above, it is easy to see that for library-based digital circuits, where all logic cells are from a cell library, the degradation of HC effect can be precharacterized for cells in the library and stored in a look-up table (LUT). Fig. 2 illustrates how a NAND2 cell may be characterized, by enumerating the signal input pin, the signal type, the transition time denoted as tr, and the output load denoted as C_L. Note that a transistor can

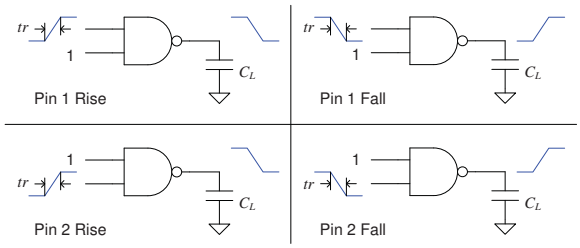

Fig. 2. Characterization of a NAND2 cell. The number of simulations required for characterization is identical to those of timing characterization.

experience age gain even if there is no transition on its gate input: for example, for a two-transistor NMOS pulldown in the NAND2 cell, a transition that turns on the upper input, while the lower input is already on, can cause an increase in AG for the lower transistor. We capture such effects in our model. For example, for each case shown in the figure with specified tr and C_L, the AGs of all four transistors in the NAND2 cell are computed simultaneously.

The LUT of each cell i outputs the AGs of all transistors j inside the cell, and has five input parameters as expressed in Equation (10), where k stands for the input pin with signal transition[1], r/f for the transition type (rise or fall), inp for the input vector of the remaining input pins (if more than one input vector can make pin k critical), tr_k for the input transition time on pin k and C_L for the load capacitance.

$$\left\{\text{AG}_{j,k}^{r/f}\right\}_{j\in\text{cell } i} = \text{LUT}_{\text{AG}}(k, r/f, inp, tr_k, C_L) \tag{10}$$

Characterization cost: The number of simulations required to characterize AG is *identical* to that required for timing characterization: in fact, the same simulations are used, but additional currents/voltages are monitored, followed by a post-processing phase in which mathematical operations (such as numerically integration)

[1]As in static timing analysis, we operate under the single input switching (SIS) assumption, i.e., the signal transition for a logic cell is triggered by one signal. This can be extended to the multiple input switching (MIS) scenario, where more than one signal arrives during the transition using methods similar to those used for timing characterization. However, given that the age function is computed cumulatively over long periods of time and that the probability of MIS is typically much lower than that of SIS, the SIS assumption gives an adequate level of accuracy. Further improvements in accuracy here are likely to be overshadowed by modeling errors at the device level.

are performed on this data to compute AG. Therefore, the number of simulations is $O(N_{\text{cell}})$, where N_{cell} is the number of cells, and so is the storage complexity of the LUT.

The effect of aging on a transistor is to alter its saturation drain current I_{on}. This in turn affects key performance parameters such as the propagation delay and output signal transition time of a logic cell that the transistor lies in. Given that the aging perturbations are small, we use first-order models for these relationships, as is done in other variational methods [13]. The propagation delay d_i and signal transition tr_i of cell i are modeled using the following linear relationship with the $\Delta I_{\text{on}}/I_{\text{on}}$ of transistors j inside cell i:

$$d_i = d_{i0} + \sum_{j \in \text{cell } i} S^d_{ij} (\Delta I_{\text{on}}/I_{\text{on}})_j \quad (11)$$

$$tr_i = tr_{i0} + \sum_{j \in \text{cell } i} S^{tr}_{ij} (\Delta I_{\text{on}}/I_{\text{on}})_j \quad (12)$$

The propagation delay d_i, signal transition time tr_i, and their sensitivities S^d_{ij} and S^{tr}_{ij} to the transistor $\Delta I_{\text{on}}/I_{\text{on}}$ values are calculated using standard techniques. The approximation that mobility degradation $\Delta\mu/\mu = \Delta I_{\text{on}}/I_{\text{on}}$ is used for device model in SPICE analysis. As pointed out earlier, these correspond to the same SPICE simulations that are used for AG characterization, although different results are extracted from the simulations. The results are stored in LUTs, expressed as follows:

$$d_i = \text{LUT}_d(k, r/f, inp, tr_k, C_L) \quad (13)$$

$$\{S^d_{ij}\}_j = \text{LUT}_{S_d}(k, r/f, inp, tr_k, C_L) \quad (14)$$

$$tr_i = \text{LUT}_{tr}(k, r/f, inp, tr_k, C_L) \quad (15)$$

$$\{S^d_{ij}\}_j = \text{LUT}_{S_{tr}}(k, r/f, inp, tr_k, C_L) \quad (16)$$

As stated earlier, the computations of these LUTs has similar complexity as that of AG characterization. Moreover, there are established methods for computing each one of these, as they are used in variational/statistical analysis.

IV. Circuit-Level Analysis

Given a set of precharacterized cells, our task at the circuit level is to efficiently use this information to perform scalable circuit-level analysis using these accurate models. Our analysis consists of four steps, described in this section: first, finding the distribution of the signal transition time at each node; second, calculating the AG for all gates in a circuit, considering their context in the circuit; third, using this information to analyze device aging; and fourth, analyzing the delay degradation of the circuit.

A. Distribution of Signal Transition Time

Due to the discrete nature and finite (but potentially large) number of signal paths in digital circuit, the signal transition time, $tr(q)$, at a certain node q has a discrete probability distribution, $\Pr(tr(q))$, which is nonzero at all values of $tr(q) \in \mathbf{Tr}^{(\mathbf{q})}$, where $\mathbf{Tr}^{(\mathbf{q})}$ stands for the set of all possible tr values of node q.

We assume that the signal transition times of the primary inputs is known (and assumed to be constant). The signal transition distribution of all internal nodes can be calculated either using Monte Carlo simulation, or using a probabilistic method. Here, we ~~use~~ introduce a transition propagation (TP) method to calculate the transition time distribution (rise and fall separately) at each node, which is similar in spirit as static timing analysis (STA), but calculates the complete distribution information of transition time using signal probability (SP) and activity factor (AF), instead of just solving for the longest delay and transition time, as in conventional STA.

As each gate q is processed in topological order, given the distribution of transition times at each input pin of the gate, we use the LUT_{tr} in Equation (15) to compute the distribution of $tr(q)$ at the output. A single transition at the output of q can be triggered under a number of different logical input conditions. We enumerate these conditions for each gate, which correspond to enumerating, for each input pin k, the set of noncontrolling inputs that allow a transition at k to become a transition at q. Under each condition, we compute $tr(q)$ using LUT_{tr}, and $\Pr(tr(q))$ using the activity factor (AF) of the corresponding input transition and the signal probability (SP) of the nontransitioning inputs.

The enumeration over all patterns on a gate is not expensive for a gate with a reasonable number of inputs; however, we must also perform an enumeration over all transition times. In principle, this could lead to state explosion as the number of possible elements of $\mathbf{Tr}^{(\mathbf{q})}$ are enumerated. To control this, we use data binning to reduce the number of data points that represent the distribution by approximating it with a discrete distribution over a smaller number of points, denoted as $\mathbf{Tr_s}$. We find that the error due to this approximation is negligible.

B. Mean AG Calculation in Digital Circuits

As discussed in Section III.A, device aging in a library cell is modeled using age gain per transition $\text{AG}^{r/f}_{j,k}$ and characterized using a quasistatic approach at the cell-level. At the circuit level, since each input pin k of a logic cell i has different probability distribution of transition time $tr_{r/f}$ (r/f for rise and fall), computed using the results of the method in Section IV.A, the age gain from each rise or fall signal on pin k also has a unique distribution.

Unlike the case of static timing analysis (STA) for delay analysis, where the slowest path is concerned, the aging analysis must consider the average operational conditions. Therefore the mean value of the age gain distribution is calculated as shown in Equation (17), where the new term $\text{AG}_{k,j}$ is defined as the mean age gain of transistor j per input signal cycle (including one rise and one fall signal) on pin k.

$$\begin{aligned} \text{AG}_{k,j} &= \text{AG}^r_{k,j} + \text{AG}^f_{k,j} \quad (17) \\ \text{where } \text{AG}^r_{k,j} &= \sum_{tr_r \in \mathbf{Tr_s}} \text{AG}^r_{k,tr_r,j} \cdot \Pr(tr_r) \\ \text{AG}^f_{k,j} &= \sum_{tr_f \in \mathbf{Tr_s}} \text{AG}^f_{k,tr_f,j} \cdot \Pr(tr_f) \end{aligned}$$

where $\mathbf{Tr_s}$ is the approximate discretized version of $\mathbf{Tr}$. Here $\text{AG}_{k,j}$ is calculated as the sum of the mean age gain per rise signal, $\text{AG}^r_{k,j}$, and mean age gain per fall signal $\text{AG}^f_{k,j}$, which are computed separately using age gain per transition under specific transition time tr_r and tr_f from the cell-level AG LUT in Equation (10), and the signal transition time distribution in Section IV.A.

C. Analysis of Device Aging

The circuit-level device aging analysis is performed based on analysis of the device age gain per signal cycle in the above section, and the statistical estimation of signal cycles in a given period of circuit operations. All signal paths (instead of only critical ones in STA) are considered in the device aging analysis, because all signal propagations affect the device aging. If a circuit is V_{dd}-gated or power-gated, the device aging model incorporates this effect using signal statistics, as shown below.

During a time period t of circuit operation, the age of a transistor j in a digital circuit is the accumulation of age gains (AGs) due to signal cycles on its input pins that occurred from time 0 to t. Since we have already obtained the mean AG per signal cycle in Equation (17), the device age function can be written as the number of signal cycles on each pin k times AG per cycle of k, summed

for all input pins of cell i (where transistor j belongs), as follows:

$$\text{age}_j(t) = \sum_{k\in\text{pin}_i} N_k \cdot \text{AG}_{k,j} = \sum_{k\in\text{pin}_i} \eta_k \cdot t \cdot \text{AG}_{k,j} \quad (18)$$

Here $\text{AG}_{k,j}$ stands for the mean age gain of transistor j per cycle of input signal on pin k; N_k stands for the number of signal cycles on pin k during time period of t, and $\eta_k = N_k/t$ is defined as the rate of effective signal cycle on input pin k, that causes cell switching. The value of η_k can be obtained using the statistical information of signal probability (SP) and activity factor (AF) as

$$\eta_k = f_{\text{ref}} \cdot \text{AF}_k \cdot \text{Pr}_{k\ \text{critical}} \quad (19)$$

Here, f_{ref} is the frequency of reference clock, AF_k is the activity factor of the k^{th} input pin of cell i, i.e., the average number of signal transition cycles in a reference clock cycle [14], and $\text{Pr}_{k\ \text{critical}}$ is the critical probability of pin k, i.e., the probability that the cell output is dependent on the input logic of pin k:

$$\text{Pr}_{k\ \text{critical}} = \text{Prob}(\text{output}(\text{pin}_k = 0) \neq \text{output}(\text{pin}_k = 1)) \quad (20)$$

This can easily be calculated using the joint signal probability of the input pins (computed from the Monte Carlo-based SP simulations described in Section V) and the truth table of the logic cell.

D. Analysis of Circuit Delay Degradation

The circuit delay degradation analysis is performed based on the models discussed in the previous sections, and static timing analysis (STA) is used to calculate the delay of the fresh and the aged circuits.

HC effects can slow down the signal transition during the aging process, which in turn reduces the age gain per transition, further slowing down HC-based circuit aging. Therefore, in principle, the circuit delay degradation is generally a *decelerating* process, as will be pointed out in Section V, and it may need iterations for accurate analysis that recalculate the slowdown in signal transition times in multiple steps and update the the age gains. Our experimental results in Section V explore a *one-step* method (where the signal transition times at $t = 0$ are used throughout the simulation) with a *64-step* method (where the transition times are updated 64 times through the life of the circuit). The results demonstrate that in practice this deceleration effect of aging is quite insignificant and can safely be ignored, so that the degradation analysis can be performed efficiently without iterations[2].

The degraded critical path delay D in a digital circuit is given by

$$D = \sum_{i\in\text{path}} d_{i0} + \sum_{i\in\text{path}} \Delta d_i = D_0 + \Delta D \quad (21)$$

The cell-level delay degradation Δd_i, which is modeled as a linear function of all transistor degradation $\Delta I_{\text{on}}/I_{\text{on}}$ in Equation (11), can be derived as following using the models of $\Delta I_{\text{on}}/I_{\text{on}}$ and $\text{AG}_{k,j}$ in Equation (4) and (17).

$$\Delta d_i = \sum_{j\in\text{cell}\ i} S_{ij}^d \cdot A \cdot (\text{AR}_j^{(i)} \cdot t)^n \quad (22)$$

$$\text{where} \quad \text{AR}_j^{(i)} = \sum_{k\in\text{pin}_i} \eta_k^{(i)} \text{AG}_{k,j}^{(i)}$$

Therefore the critical path delay degradation is

$$\Delta D = At^n \sum_{i\in\text{path}} \sum_{j\in\text{cell}\ i} S_{ij}^d \cdot (\text{AR}_j^{(i)})^n \quad (23)$$

[2]Other authors [10] have found nontrivial *acceleration* effects of HC degradation, mainly due to the inaccuracy of their model assumption of constant HC stress during signal transitions (in contrast to our time-varying model illustrated in Fig. 1).

Equation (23) indicates that the path delay degradation of digital circuits has a power function versus time, with the same exponent n as the power model of device degradation in Equation (4). However, since devices on different paths have different rate of aging, the longest-delay path may change after a period of degradation.

V. Experimental Results

The proposed method for delay degradation analysis of digital circuit is applied to the ISCAS85 and ITC99 benchmark circuits for testing. The circuits were synthesized by ABC [15] using a subset of the Nangate 45nm open cell library [16]. The cell-level library characterization was performed using HSPICE simulation and 45nm PTM model [17]. The circuit-level analysis was implemented in C++ and run on a Linux PC with 3GHz CPU and 2GB RAM. The parameters a_2, a_3 and m of the device-level HC model in Equation (7) is from [7]. The coefficients C_1, C_2 and C_3 for different energy-driven modes have arbitrary units (a.u.) and are selected empirically according to the τ vs I_{ds}/W plot in [7]. The parameter A in Equation (4) also has a.u..

The cell-level characterization of transistor age gain, as well as the degradation of cell delay and output transition is performed using HSPICE simulation with the enumeration of all signal input cases for each cell. The characterization of the library which contains 34 logic cells takes 1 hour and 52 minutes of runtime and 8.4MB of hard drive storage (in ASCII format). This is $1.87\times$ runtime and $5.94\times$ storage overhead compared with timing characterization (Equations (13–16)), which is well within reasonable range.

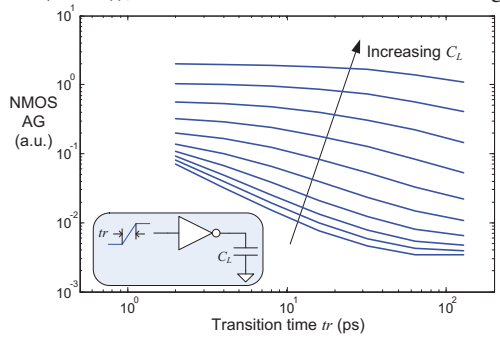

Fig. 3. Age gain versus signal transition time and load capacitance.

Fig. 3 plots the curves of the NMOS transistor age gain (AG) versus the input signal transition tr of an inverter with a rising input signal, under different load capacitance C_L. The figure indicates that the input signal transition generally causes more damage to the transistor (larger AG) when the load C_L is large, or when the transition tr is small. This is explained by the fact that HC degradations are caused by the charge carriers flowing through the channel, and larger load C_L requires more charge to be moved, while smaller transition tr makes the carriers moving faster, thus causing more damage. This result is consistent with the data presented in [8]. In other transition cases, with different cells and input signals, the AG vs. tr and C_L plots may be slightly different, but all have a trend similar to Fig. 3. Specifically, for the small range in which the transition time increases as a result of aging ($<2\%$), the AG generally reduces slightly, i.e., aging slightly decelerates with time.

The results of our method for circuit degradation analysis under HC effects are shown in Table I for different benchmark circuits. The sizes of the circuits range from 221 cells (c432) to 20407 cells (b17). Three methods are implemented and applied on each benchmark: the first is a Monte Carlo (MC) simulation with 10000 random input signal transitions for the circuit the second is the proposed analysis approach using one-step approximation that ignores the deceleration of aging, and the third incorporates deceleration, updating the aged

transition times at 64 time points over the life of the circuit (see Section IV.D for details). The signal probability (SP) and activity factor (AF) data for the latter two methods is obtained using Monte Carlo method with 10000 random input transition samples. The circuit degradations are calculated at t=5000 a.u. with reference clock f_{ref}=1GHz, input SP=0.5 and AF=0.05.

TABLE I
RUNTIME AND DEGRADATION COMPARISON FOR DIFFERENT METHODS

Circuit Name	SP/AF	Monte Carlo		1-step Analysis		64-step Analysis		DF
	T_{exe}	T_{exe}	ΔD	T_{exe}	ΔD	T_{exe}	ΔD	ΔD_{err}
c432	.57s	3.3s	9.46%	.03s	9.60%	1.5s	9.55%	-41%
c880	1.1s	5.9s	3.54%	.04s	3.39%	2.6s	3.37%	42%
c1908	1.4s	8.9s	3.69%	0.1s	3.76%	3.3s	3.75%	54%
c2670	1.9s	11s	6.02%	0.1s	6.16%	5.6s	6.14%	-22%
c3540	3.8s	21s	8.35%	0.2s	8.46%	9.6s	8.44%	11%
c5315	5.1s	31s	16.8%	0.2s	16.3%	11s	16.2%	-38%
c6288	29s	109s	6.38%	0.5s	6.65%	27s	6.61%	27%
c7552	10s	50s	17.2%	0.3s	16.9%	15s	16.8%	58%
b14	61s	153s	9.04%	0.7s	9.16%	43s	9.13%	-12%
b15	89s	205s	6.81%	1.0s	6.54%	60s	6.49%	32%
b17	327s	675s	3.97%	3.2s	4.10%	190s	4.05%	48%
b20	166s	369s	4.82%	1.5s	5.00%	94s	4.94%	32%
b21	164s	362s	3.93%	1.5s	4.15%	89s	4.12%	35%
b22	227s	495s	3.51%	2.0s	3.63%	120s	3.60%	53%

In Table I, the first column lists the benchmark circuit name, the second column lists the runtime of SP and AF calculation, and the remaining columns show the runtime and circuit delay degradation obtained using the three methods. The results show that the one-step analysis and 64-step analysis yield very close results ($<$1% relative error), demonstrating that the one-step method is an accurate approximation. The error between one-step analysis and MC is small (2.5% relative error), showing the proposed analysis method is efficient and accurate compared with Monte Carlo simulation.

The last column shows a comparison with a simple duty-factor based scheme, similar to [10]. Note that in contrast with this method, our approach performs quasistatic analysis with newer energy-driven model, which captures the time-varying HC stress, and indicates that the transistor AG decreases when signal transition slows down (Fig. 3). In addition, [10] uses an empirical device HC model which only considers the switching transistors and ignores the other transistors in the stack which also experience current stress. Our approach perform the device degradation analysis in the cell level, and the AG of all transistors in a logic cell is computed simultaneously. The results in the last column assume constant HC stress through signal transitions, ignores non-switching transistor degradation, and uses worst-case transition time. Experimental results of all tested benchmarks show errors of -41% to $+58\%$ for this method. It is clear that the use of such simplifying assumptions, commonplace in all prior work on large-scale circuits, results in serious errors.

It is important to note that the SP and AF analysis take more time than the HC degradation calculation; however a) this computation is a common overhead shared by other circuit analyses, such as power estimation, oxide reliability, BTI degradation, etc., and should not be counted solely towards the proposed approach, and b) our implementation uses Monte Carlo simulation to generate these probabilities; faster graph traversal based methods may also be used.

Fig. 4 shows the circuit delay degradation versus time on a logarithm scale for benchmark c1908 using both the proposed analysis method (one-step) and MC simulation. The results from these two approaches match well with each other, and the delay degradation is a power function of time with exponent 0.5 before t=10000. After that the delay degradation is no longer a power function and increases at a faster rate since the critical path may change, as discussed in Section IV.D.

An examination of the degradation of $\Delta tr/tr_0$ in c7552 confirms that the effects of aging deceleration are negligible, e.g., at t=5000,

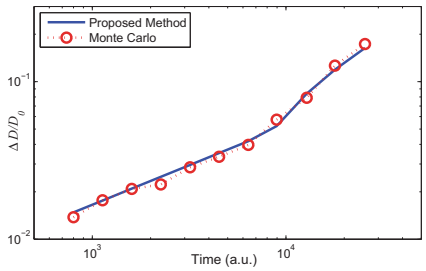

Fig. 4. Circuit delay degradation versus time.

when the circuit has 17% delay increase, the average $\Delta tr/tr_0$ is only 1.8% which leaves AG per transition virtually unaffected, according to the AG/tr curves in Fig. 3. In contrast, the duty factor model [10] assumes constant HC stress in the off-to-on transition, leading to the result that the transition time degradation elevates the duty factor and accelerate circuit degradation, which is incorrect.

VI. Conclusion

This paper focuses on the HC effect in large scale digital circuits, and proposes a scalable method for analyzing CHC/CCC-induced delay degradation, with innovations in analysis at the transistor, cell, and circuit levels. The method is validated by Monte Carlo simulation on benchmark circuits and is shown to be accurate.

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