Ring Oscillator Clocks and Margins

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***Abstract*—How much margin do we have to add to the delay lines of a bundled-data circuit? This paper is an attempt to give a methodical answer to this question, taking into account all sources of variability and the existing EDA machinery for timing analysis and sign-off. The paper is based on the study of the margins of a ring oscillator that substitutes a PLL as clock generator. A timing model is proposed that shows that a 12% margin for delay lines can be sufficient to cover variability in a 65nm technology. In a typical scenario, performance and energy improvements between 15% and 35% can be obtained by using a ring oscillator instead of a PLL. The paper concludes that a synchronous circuit with a ring oscillator clock shows similar benefits in performance and energy as those of bundled-data asynchronous circuits.**

I. Introduction

Asynchronous bundled-data circuits offer an attractive trade-off between synchronous and quasi delay-insensitive (QDI) circuits in terms of area, performance, and power. QDI provides highly robust solutions at the expense of an important cost in area and power for the use of delay-insensitive encoding techniques (e.g., dual rail). On the other hand, synchronous circuits are based on the generation of high-quality clock signals that provide reliable timing references. Phase-locked loops (PLLs) are commonly used to generate low-jitter clocks that are agnostic to the variability experienced by the circuit at runtime.

The way variability is handled in synchronous circuits is by adding guardband margins to the clock period that can accommodate the static and dynamic delay fluctuations. Static timing analysis (STA) with different process, voltage, and temperature (PVT) corners and on-chip variability (OCV) derating factors are typically used to estimate conservative bounds on delay variability [1].

The datapath of a bundled-data circuit is similar to the one of a synchronous circuit (see Fig. 1). The main difference lies on the clock signal generated by a set of distributed oscillators implemented as delay lines (e.g., chains of inverters) and synchronized with other oscillators via handshake controllers (req/ack signals), such as the ones presented in [2]. If a clock domain requires a totally independent clock generator (i.e., no handshaking with other domains), the controller disappears and the delay line becomes a simple ring oscillator (RO).

Fig. 2 depicts a system with two independent clock domains. One clock is generated by an RO and the other by a PLL. From the functionality point of view, both generators are interchangeable. It is even possible to design a system in which each clock domain can dynamically select (via multiplexers) which clock generator must be used at each time instant.

In the last few years, we have observed a proliferation of proposals for clock generation based on ROs [3]–[7]. The main motivation is the capability of tracking PVT variability, thus reducing the guardband margins and providing tangible improvements in power and performance. Bundled-data circuits also share the same motivation given that the role of the ROs and the delay lines is similar. The question we would like to answer in this paper is:

Which are the benefits of using an RO clock instead of a PLL?

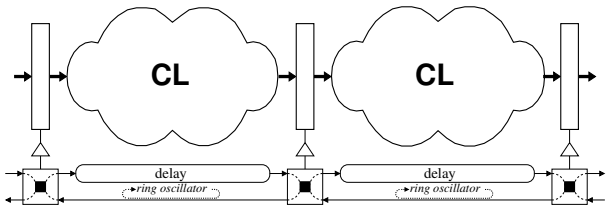


Fig. 1: Bundled-data asynchronous pipeline

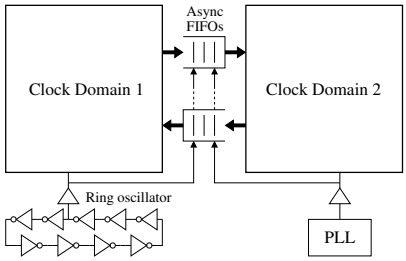


Fig. 2: GALS system with two clock domains.

The answer to this question will implicitly give an estimation of the margins that must be applied to delay lines in bundled-data circuits.

The paper concludes that substituting PLLs by ROs is a practical alternative that inherits most of the benefits of asynchronous bundled-data circuits in terms of tolerance to variability. Moreover, the actual commercial EDA tools for STA can be used in RO clocks with minimum changes on the scripts required for sign-off.

II. Why Ring Oscillator Clocks?

Designers usually advocate for robust timing references during STA. Low-jitter clocks and near-zero-skew clock trees are mechanisms that contribute to reduce the guardband margins required to achieve a target performance. For this reason, ROs have been generally disregarded as clock sources because of their jitter instability under the presence of variations, thus making STA either difficult or over-conservative (adding margins to cover a large clock jitter).

But looking at this problem from another angle, we can observe that the jitter generated by an RO is highly correlated with delay variability of the circuit [7].

This phenomenon is illustrated in Fig. 3. The horizontal bars represent delays. The critical paths of the circuit and the RO (or delay line in a bundled-data circuit) are competing paths. At different time instants (t_1, t_2, and t_3) the paths may experiment different delays due to the operating conditions (e.g., voltage and temperature fluctuations). However, and given that all paths are in the same neighbourhood, their delays are highly correlated. Therefore, the margins required for the RO clock only have to protect its *differential variability* with regard to the critical paths of the circuit (represented as Δd in the picture).

If we would use a PLL (agnostic to variability), the margins for timing correctness should cover the full variability range of the

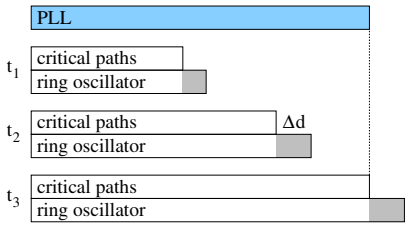


Fig. 3: Guardband margins for a PLL and an RO clock.

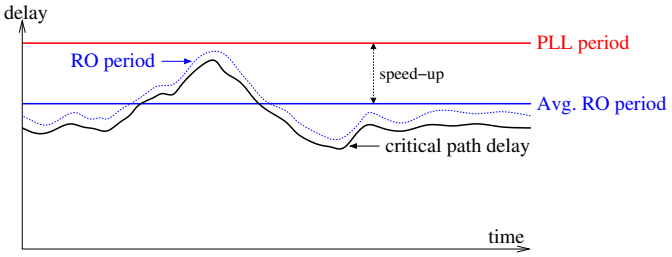


Fig. 4: Period for a PLL and an RO with varying operating conditions.

critical paths. In conclusion, the main differences between a clock signal generated by a PLL or by an RO clock are:

- The margins for an RO clock are smaller and only have to cover the differential variability with regard to the critical paths.
- An RO clock generates a high-jitter clock whose average frequency is better than the one generated by a PLL.

Fig. 4 emphasizes the potential benefits of using an RO as a clock source. The period generated by a PLL must conservatively account for all possible (global and local) variations produced by the fluctuating operating conditions of the circuit, whereas an RO must only account for local variations. Overall, the average period of the RO is smaller than the one required for a PLL.

A key aspect of the RO is that it can *instantaneously* adapt the cycle period to dynamic variations (e.g., unexpected voltage droops). This particular aspect is crucial to save margins and bring significant improvements in power and performance. This immediate reaction allows the RO clock to outperform other techniques as dynamic voltage and frequency scaling [7] which reaction time is typically a few or hundred clock cycles [8].

The purpose of this paper is to quantify the benefits of RO clocks and define a methodology for their timing sign-off.

III. Static Timing Analysis for a Ring Oscillator Clock

The purpose of Static Timing Analysis (STA) is to check whether the circuit meets a set of timing constraints that guarantee a proper propagation of data across the sequential elements. Two timing constraints are usually checked: setup and hold. The setup constraint is the one that determines the period of the clock and will be the center of our attention.

A timing constraint is specified as an inequality of two competing paths: the *launch* and the *capture* paths. For a setup constraint, the launch path usually starts at the clock generator, goes through the clock tree, the launch flip-flop, the critical path and ends at the capture flip-flop (red path in Fig. 5). The capture path (blue) starts from the clock generator, and ends at the capture flip-flop. It is important to note that the launching and capturing clock pulses are separated by

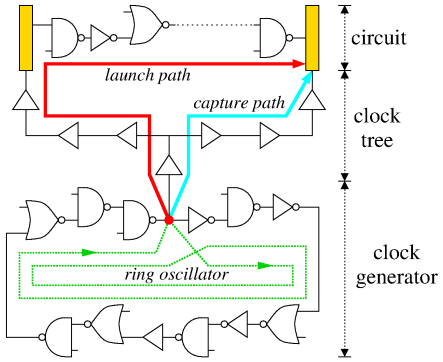


Fig. 5: Paths involved in a setup constraint with an RO clock.

a clock period. Thus, the setup constraint can be defined as[1]:

$$LaunchPath < CapturePath + Period \tag{1}$$

The previous inequality must also take into account variability. Given that timing analysis cannot be performed under all possible operating conditions, the conventional approach for modern STA is to analyze the circuit in a discrete set of corners. Each corner defines the values for a set of parameters that model process and environmental variations (voltage and temperature).

For a given subset of global PVT operating conditions, the components of the circuit also suffer local (within-die, on-chip) variations. To cover on-chip variations, corner-based sign-off applies some derating factors to the timing paths of the circuit that scale the delays with regard to other competing paths in the timing constraints.

Finally, clock jitter and any pessimism derived from the inaccuracies and uncertainties of STA must also be modeled. Typically, they are modeled as a fixed margin in the timing constraints.

In summary, in modern STA, variability is modeled using the following mechanisms:

- **library corners** to model global variability.
- **derating factors** to model on-chip variability.
- **clock uncertainty** to model clock jitter and other inaccuracies.

Timing constraints must hold for all paths and corners under consideration. Given a library corner, the derating factors and clock uncertainty must be incorporated in the setup constraint:

$$\delta_L \cdot LaunchPath < \delta_C \cdot CapturePath + Period - Jitter \tag{2}$$

where $\delta_L \geq 1$ and $\delta_C \leq 1$ are the derating factors applied to the launch and capture paths, respectively. Clock jitter must be conservatively subtracted from the period.

A simplification of the model consists of making the derating factors symmetric and reducing the analysis to a parameter ϵ in such a way that:

$$\delta_L = 1 + \epsilon, \qquad \delta_C = 1 - \epsilon. \tag{3}$$

The accuracy on how these derating factors model on-chip variability is crucial. Foundries usually provide conservative values. However, more aggressive values can be used if designers have additional knowledge about the behavior and operating conditions of the circuit.

[1]For simplicity, we assume the setup time of the capturing flip-flop to be included in the delay of the launch path.

A. Timing sign-off for a ring oscillator clock

When using an RO as clock generator, the term $Period - Jitter$ must be substituted by the delay of the RO in constraint (2):

$$\delta'_L \cdot LaunchPath < \delta'_C \cdot (CapturePath + RO) \quad (4)$$

with $\delta'_L = 1 + \epsilon'$ and $\delta'_C = 1 - \epsilon'$ being new derating factors.

Notice that the derating factor δ'_C is also applied to the delay of the RO (green path in Fig. 5). This is because the RO must be treated as a conventional timing path that experiments the same sources of variability as the remaining components of the circuit.

The derating factors in (2) can be different from those in (4) since δ'_C and δ'_L must also take into account the spatial correlation between the critical paths and the RO.

The key question is: which is the main difference between (2) and (4)? The answer is that these inequalities must hold for all PVT conditions (corners). While the PLL-based period is fixed for all conditions, the RO adapts its period "on-the-fly" and instantaneously, thus reducing the required guardband margins.

For simplicity, and without loss of generality, we will consider that the launch and capture paths are disjoint. In general, they share some part of the clock tree for which no derating factors should be applied. The technique of not applying derating factors for common paths is called *Common Path Pessimism Removal* (CPPR) [1]. In this paper we will assume that the common paths have already been cancelled out in the timing constraints.

In the next sections, we will present a simple model to quantify the benefits of using an RO clock.

B. Multicorner static timing analysis

When performing timing closure on a circuit, STA is performed on multiple corners in order to determine the behavior of critical paths under different PVT conditions. In circuits that operate with PLLs, the clock period is set to that speed that guarantees that the circuit runs properly under most of all the PVT conditions.

However, most of dies may run faster than the specified clock period after fabrication, as PLL sign-off is very conservative. To avoid die underutilization, a process known as binning classifies final products in such a way that each die could run at its maximum speed. Unfortunately, binning is a complex and expensive technique which is not always affordable.

Nevertheless, the RO clock period is determined by the PVT conditions that each die experiments at a given point in time, which in practice is similar to performing binning if the RO is properly designed [7]. In this scenario, multicorner STA is necessary to guarantee the correct functionality of the RO at any available corner.

IV. Defining Margins and Derating Factors in a Ring Oscillator Clock

This section presents a statistical model for PVT variations using an RO as a clock source. To ease comprehension, some of the details are presented in the appendix.

A. Static and dynamic on-chip variability

Process, voltage, and temperature are the main sources of on-chip variability. We can classify variability sources depending on their behavior. On the one hand, *static* process (P) variability does not fluctuate along time, and it is caused by the uncertainties of manufacturing. Process variations are mainly due to voltage threshold variations, which can be accommodated in statistical models. In this paper, we assume that cell delays follow a normal distribution due to random process variations on cell voltage threshold [9], [10].

On the other hand, voltage and temperature (VT) variations are *dynamic*. Unflattened thermal distribution, unbalances in IR droops, computational activity, and floorplan power density are examples of VT variability [11]–[13]. As a result, VT changes locally in time depending on the chip activity and the fluctuations of the voltage source. The local component of dynamic variability can be quantified or bounded with enough detail by analyzing the target circuit with EDA tools. Note that local dynamic variability is usually marginal. Moreover, on-chip voltage has a large global component which is more pronounced when cells are close—more on this in Section VI.

Let us now model the delay of a path π, i.e., D_π:

$$D_\pi(t) = D^0_\pi + D^P + D^V(t) + D^T(t)$$

where D^0_π is the nominal critical path delay in a given corner, and D^P, $D^V(t)$, $D^T(t)$, represent the delay variation due to process, voltage, and temperature, respectively[2]. There exist other sources of variability as aging. In this paper we omit any other variability sources except PVT as there is no consensus in the community on how they can be quantified. Process delay variation is modeled as a normal distribution. Hence, D^P will be also modeled as a normal distribution. Let us define $D^P \sim N(0, \sigma_\pi)$, $D_\pi(t)$, then,

$$D_\pi(t) \sim N(D^0_\pi + D^V(t) + D^T(t), \sigma^2_\pi) \quad (5)$$

Simplifying, let us represent the delay of path π at time t as:

$$D_\pi(t) \sim N(D^0_\pi + D^{VT}_\pi(t), \sigma^2_\pi)$$

where D^0_π is the nominal delay in a specific corner, $D^{VT}_\pi(t)$ accounts for the dynamic variability produced by the fluctuations of voltage and temperature, and σ_π models the static (process) variations affecting the critical path.

B. On-chip margins in a PLL clock

Let $D_L(t)$ and $D_C(t)$ be the delay of the launch and capture paths at time t, respectively. Both delays follow a normal distribution as defined in (5). That is, $D_L(t) \sim N(D^0_L + D^{VT}_L(t), \sigma^2_L)$ and $D_C(t) \sim N(D^0_C + D^{VT}_C(t), \sigma^2_C)$. Let P and J be the clock period and jitter of a rigid clock such as the PLL. The setup constraint (2) can be defined as:

$$P - J + D_C(t) - D_L(t) > 0,$$

that results in:

$$P > (D^0_L - D^0_C) + J + M_{PLL} \quad (6)$$

where $(D^0_L - D^0_C)$ is its nominal corner value and M_{PLL} is the guardband margin required to cover on-chip variations. M_{PLL} can be decomposed into two different terms: a margin due to P (M^P_{pll}) variations and a margin due to VT (M^{VT}_{pll}) variations. Both margins are defined as

$$M^P_{pll} = \Psi \cdot \sigma_{PLL}; \qquad M^{VT}_{pll} = \max|_t \big(D^{VT}_L(t) - D^{VT}_C(t)\big) \quad (7)$$

where Ψ is a constant that depends on the number of critical paths and the desired yield (see (17) in the appendix), and $\sigma^2_{PLL} = \sigma^2_L + \sigma^2_C$. Note that the maximum difference along time between $D^{VT}_L(t)$ and $D^{VT}_C(t)$ is required to obtain a conservative of the clock period.

[2]Note that D_P models static variability and does not depend on t.

C. Guardband margins in a ring oscillator clock

Similar to the previous analyses, it is possible to estimate the margin required by an RO clock. Let $D_{RO}(t)$ be the delay of the RO defined as in (5), i.e., $D_{RO}(t) \sim N(D^0_{RO} + D^{VT}_{RO}(t), \sigma^2_{RO})$. Here, the setup constraint (4) for any timing path can be defined as:

$$D_{RO}(t) + D_C(t) - D_L(t) > 0,$$

and by developing the previous expression, we can obtain:

$$D^0_{RO} \geq (D^0_L - D^0_C) + M_{RO} \tag{8}$$

where $(D^0_L - D^0_C)$ is its nominal value and M_{RO} is the margin required to absorb local PVT variations. As in the previous section, M_{RO} can be decomposed into a margin to cover P variations (M^P_{RO}) and a margin to cover VT variations (M^{VT}_{RO}). Both margins are defined as:

$$M^P_{RO} = \Psi \cdot \sigma_R; \qquad M^{VT}_{RO} = \max|_t \big(D^{VT}_L(t) - D^{VT}_{RO}(t) - D^{VT}_C(t)\big)$$

where $\sigma^2_R = \sigma^2_{RO} + \sigma^2_L + \sigma^2_C$. It is important to highlight that σ_R is larger than σ_{PLL} as it needs to account for the on-chip process variability suffered at the RO, represented by σ^2_{RO}.

D. Comparing PLL and RO on-chip variability margins

There exist some differences between the guardband margins used to deal with on-chip variability when comparing PLL with RO clocks. First, RO clocks do not consider any jitter margin. In addition, as σ_R is larger than σ_{PLL}, M^P_{RO} margin is larger than M^P_{pll}. This is not surprising as the RO, like any other element in the circuit, suffers process variability. In contrast, PLL is agnostic to such variability. Nonetheless, M^{VT}_{RO} is typically smaller than M^{VT}_{pll}. This is a consequence of the correlation between the RO and critical paths when referring to voltage and temperature.

Considering all sources of on-chip variability, the RO guardband margin should be larger the PLL on-chip margin for normal PVT and jitter values.

In the example shown in Section VI, the RO and PLL on-chip margins are 11.7% and 9.4% of the nominal delay at the worst-case corner. Nonetheless, the RO clock does not require additional margins to handle global PVT variability, being more effective than PLLs in the typical and average case.

Fig. 6 shows the amount of voltage received in the RO when a voltage droop periodically occurs because of circuit activity. The RO has been designed with an on-chip margin of 158ps, whereas the PLL introduces an on-chip margin of 120ps. In practice, that means that PLL period is 1515ps, as it needs to cover the worst-case scenario all the time. In contrast, the RO period fluctuates along time, being 1553ps in the worst-case scenario. As it can be seen in the figure, voltage fluctuates from 0.860mV up to 0.985mV in the RO. Consequently, the RO period varies when voltage changes, ranging from 1553ps (worst-case) to 1130ps (best-case), without causing a timing failure. In average, the RO period is 1260ps, which is an 18% faster than the PLL.

E. Applying derating factors in PLL and RO clocks

Derating factors are used to define the limits of guardband on-chip margins. It is possible to measure the PLL derating factor by rewriting (2):

$$P \geq (D^0_L - D^0_C) + J + \epsilon(D^0_L + D^0_C) \tag{9}$$

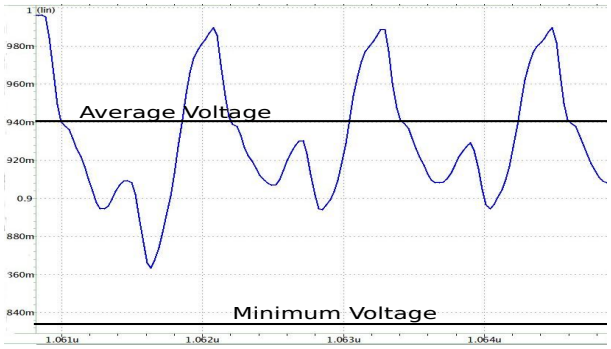


Fig. 6: Amount of voltage received in the ring oscillator.

TABLE I: RO and PLL margins and derating factors.

	Worst	Typical	Best
CP delay (ps)	1427	794	562
RO OCV Margin (ps)	162	73	47
PLL OCV Margin (ps)	155	69	44
$\epsilon(\%)$	10.8	8.7	7.8
ϵ' (%)	5.4	4.2	3.8

Note that it is possible to associate the on-chip margin M_{PLL} with the PLL derating factor ϵ by introducing (6) in (9). Thus, the derating factor ϵ for a PLL can be expressed as:

$$\epsilon = \frac{M_{PLL}}{D^0_L + D^0_C}$$

Similarly, we could define ϵ' as the derating factor required when performing timing sign-off in an RO clock. By introducing (8) in (4), we can obtain:

$$\epsilon' = \frac{M_{RO}}{2D^0_L + M_{RO}}$$

Table I shows the on-chip margins and derating factors used in the circuit implemented in Section VI. As it can be seen, the RO margin is larger for any corner than the PLL on-chip margin, but the derating factors applied at RO timing sign-off are smaller than the ones required by the PLL. Note that the PLL derating factors are different from those used in RO timing closure, as RO clocks are more sensitive to on-chip variability. Because of that, they require a throughout analysis at timing sign-off of the circuit. Nonetheless, if it is not possible at design time to perform such analysis, it is valid to apply the PLL derating factors that are provided by the foundry, as they are conservative from RO's point of view.

V. Experimental Methodology

In order to validate the timing models presented in previous sections, we have analyzed the variability of a digital circuit using commercial EDA tools. Our experimental circuit comprises 10 instances of an AES encryption module [14]. The AES encryptors were synthesized, placed, and routed using the Synopsys Design Compiler®, the Synopsys IC Compiler®, and a 65nm commercial library. Additional logic has been introduced to enable independently each individual AES encryptor. Fig. 7 shows the layout of the digital circuit evaluated in this analysis. The AES encryptors were organized in a 5×2 matrix. Each AES encryptor occupied 350x350um^2, requiring the circuit a total die area of 2488x1285um^2.

Metal layers ranging from 2 to 6 were used for routing purposes, while metal layers 9 and 10 distributed power and ground. The power delivery network was designed to keep the IR drop below a 5% of the nominal voltage. To this end, ten power pads and ten ground

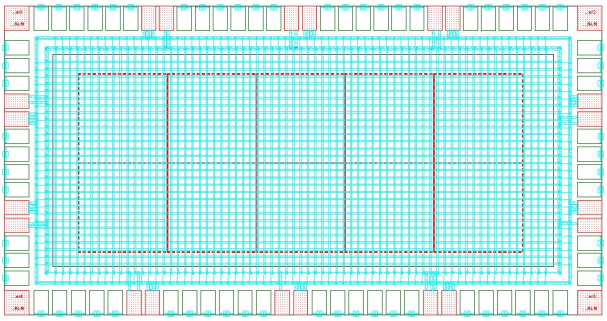


Fig. 7: Schematic floorplan of 10 AES.

pads (dotted IO pads) were equidistantly placed through the IO ring. Current flip chips allow IO pads to be placed across the die, and thus, flip chip voltage droops are more uniform than the ones presented in this paper. Despite some of the results enclosed in this paper are related to the usage of peripheral IO pads, we believe that the main conclusions of this study are still valid.

Synopsys VCS® was used to run multiple simulations and extract the switching activity of each standard cell of the circuit. Simulations covered different scenarios in which one or several AES encryptors computed in isolation, or other scenarios where all instances operated at the same time.

Synopsys Primerail® was used to perform static and dynamic IR drop analysis. The switching activity obtained from simulations allowed to estimate the voltage at any power/ground pin of the standard cells. For a complete voltage noise analysis, package [15] and voltage source models were incorporated for simulation. Voltage source variability has been set to 3% of its nominal value.

Performing an accurate temperature analysis is a difficult task and requires the usage of technological parameters that are typically not available at design time. In [16], [17] the temperature difference between any pair of nodes was quantified in real silicon for 65 and 32nm technologies, respectively. A maximum temperature gradient of 4°C and 50°C were obtained, respectively. Due to the technology proximity, we took 4°C as a reference—the same difference reported in [16][3]. Finally, we also assumed that the maximum temperature reachable in our circuit was 125°C (i.e., the maximum temperature at the worst corner).

We performed SPICE simulations over the most representative critical paths of the circuit using Synopsys HSIM®. The critical paths were extracted using Synopsys Primetime®. The parameters of the transistors of each logic gate were modified to model random process variations by adding a random component to the nominal value, according to a Gaussian distribution and using linear interpolation between the values of the parameters at different library corners ($\pm 3\sigma$ was assumed for the best/worst corners).

A. Generating a ring oscillator clock

Our evaluation methodology replaces a conventional clock source with an RO implemented according to the teachings described in [7]. The design process consists of extracting the delays of the circuit's critical path in all the available corners using static sign-off tools (in our development framework, Synopsys Primetime®). These delays feed a path synthesizer tool that produces a single chain of gates that generates an oscillating signal. The delay of the RO almost fits the delay of the circuit's critical path in all the analyzed corners, although it is a bit slower. The generated RO comprises an additional margin which goal is to avoid timing violations when the circuit operates in conditions not covered by the corners provided in commercial libraries. The more corners a library provides, the smaller this margin can be, making the RO more precise.

In our analysis the RO is connected to the 10-instance AES encryption module, and it is used as a clock source. Unlike other clock sources such as the PLLs, the clock signal delivered by the RO is strongly correlated with the global and local PVT variability that takes place in the circuit. The aim of the next section is to quantify the effects of such correlation, and to asses whether RO clocks are feasible, beneficial, and robust.

[3]The delay impact of temperature is usually smaller than other components such as voltage or process. For the commercial 65nm library used in this study, the maximum temperature difference barely affects the results presented in the paper.

TABLE II: Characterizing on-chip voltage variations

Nominal *Vdd*	Static IR drop	Max. *Vdd* droop	Avg. *Vdd*
1V	0.044V	0.168V	0.940V

VI. Variability Analysis in Ring Oscillator Clocks

A. Adaptability to voltage noise

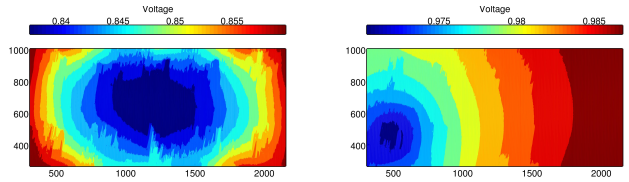
Voltage noise has two main components: global and local. Global fluctuations affect uniformly the whole die (or clock domain), whereas local fluctuations affect small regions. We will show that, despite voltage droops are highly dependent on switching activity, the global component dominates over the local, favoring the argument that ROs are in a privileged position when used as a clock source.

In this characterization, voltage noise has been divided into two components: static and dynamic. Static voltage droops are caused by energy losses in resistors when no circuit activity exists. On the contrary, dynamic voltage droops are produced when circuit current fluctuates due to switching activity and voltage source ripple. Hence, dynamic voltage droops depend on circuit resistance (dynamic IR drop) and inductance (Ldi/dt) [18], [19]. Commonly, the maximum voltage droop is used as a measure to determine the margin required in PLLs to cover voltage variability (see Sect. IV-D).

Table II summarizes the behavior of the voltage droop in the evaluated circuit. The largest component of the voltage droop is caused by dynamic variations produced by the switching activity and the voltage source ripple. Moreover, the maximum voltage droop occurs at the center of the die when all AES modules are active. However, in this scenario, the average voltage supply along time is 940mV. This value is important as it determines the average RO performance.

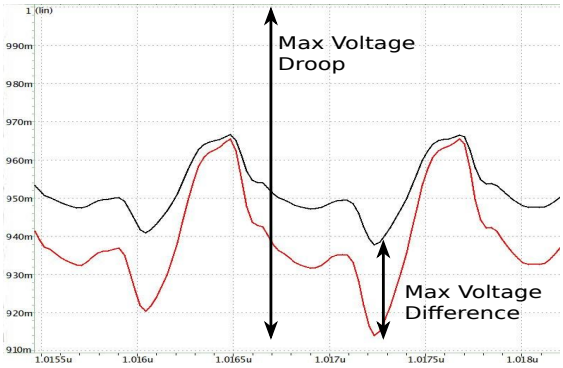
The next figures map the voltage of the circuit in two different situations. On the one hand, Fig. 8a shows the maximum voltage droop achieved at any cell of the circuit when all AES encryptors are active. The voltage droop is more pronounced for the cells that are far away from the IO pins, reaching the highest rates at the center of the die. On the other hand, Fig. 8b shows an extreme case where the switching activity is strongly localized. In that occasion, only the left-bottom AES encryptor is working. However, the maximum droop is much lower than in Fig. 8a, since the total switching activity is minimized. In particular, the maximum droop is reduced from 168mV (all encryptors active) to 59mV (a single AES encryptor active).

Unlike PLLs, RO clocks do not measure the maximum voltage droop to determine the required voltage margin. Instead, they compute the maximum voltage difference between the RO cells and any other cell in the clock domain. Fig. 9a depicts the voltage fluctuations of the two cells of the die that show the largest voltage difference during the experimental simulations. It can be observed that the

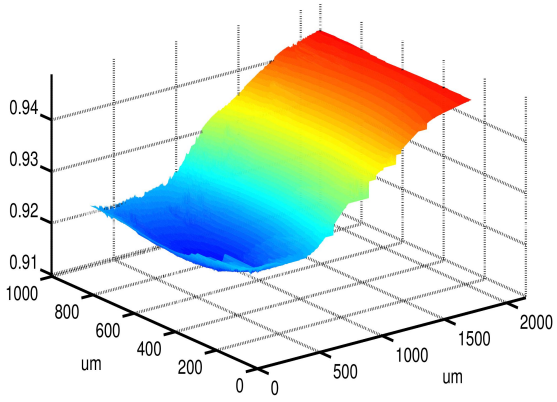


(a) All (10) AES modules active. (b) Bottom-left AES module active.

Fig. 8: Die voltage map: two different scenarios.



(a) Voltage difference between two cells.



(b) Die voltage map,

Fig. 9: Analysis of the maximum voltage difference.

maximum difference is smaller than the maximum voltage droop. Fig. 9b shows a voltage map of the die at the instant that the voltage difference between cells is the largest (i.e., 29mV).

It is important to understand that the maximum voltage droop does not necessarily generate the maximum difference between cells, given that the voltage droop has a large global component. Note that the power delivery network propagates voltage droops across the die independently from the switching activity.

Table III shows the maximum voltage difference between any two cells in three complementary scenarios: (a) when all AES encryptors are active, (b) when only the bottom-left AES encryptor is active, and (c) when all the AES encryptors placed at the left half of the die are active. These three scenarios are a good representation of extreme situations that the circuit may experiment. For instance, the maximum voltage happens when all the AES encryptors are active. In that situation, the maximum droop is 168mV, but the maximum difference between circuit cells is 25mV. Nonetheless, the maximum

TABLE III: Voltage droop analysis in three situations.

Scenario	Max V droop	Max. V Diff. between cells
All active	168mV	25mV
Bottom-left active	59mV	18mV
Half active	85mV	29mV

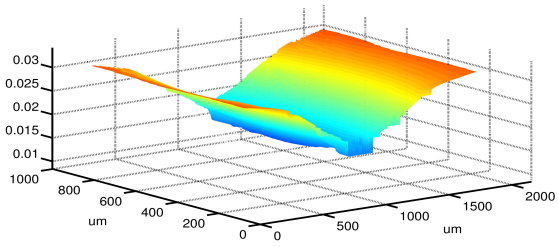


Fig. 10: Maximum voltage difference for each location of the die.

difference between circuit cells (29mV) occurs when half of the AES encryptors are active. In that scenario, the maximum voltage droop is only 85mV.

B. Finding the best location for an RO clock

The previous voltage analyses and the die voltage maps should help designers to locate a good region to place the RO clock. A near-optimal location (x, y) would be the one that minimizes the maximum difference of voltage along cells and time, i.e.,

$$\min_{(x,y)}[\max_{g,t}\left(V_{x,y}(t) - V_g(t)\right)] \tag{10}$$

where g ranges over all cells of the circuit and t ranges over time, respectively. In other words, the best location to fit the RO clock would be the one that maintains the voltage of the RO cells as similar as any other cell of the circuit.

Theoretically, the optimal point to place the RO is usually close to the point that experiments the maximum voltage droop. At that location, the RO cells experiment a larger delay, increasing the clock period. This guarantees enough time slack for all critical paths. The simulations performed are aligned with the previous hypothesis, as they indicate that best location for the RO is the center of the die because it is the place that suffers the worst voltage droop in most scenarios.

Fig. 10 plots the maximum voltage difference for each location of the die according to (10). The figure shows that the best location is around the center of the die, where the maximum voltage difference between a cell placed in the center and any other cell is 14mV.

C. Validating margins for ring oscillator clocks

Table IV reports the critical path delays of our circuit at three different corners: worst, typical, and best. The analysis assumes no on-chip variability. The table also reports the margins introduced when designing the RO and their percentage with respect to each critical path delay.

To estimate the impact of variability on the yield, a set of SPICE simulations with the most significant critical paths of the circuit have

TABLE IV: Critical path delays and RO margins.

	Worst SS/0.9V/125^{o}C	Typical TT/1.0V/25^{o}C	Best FF/1.1V/0^{o}C
CP delay (ps)	1427	794	562
RO margin (ps)	162	73	47
% margin	11.4%	9.2%	8.4%

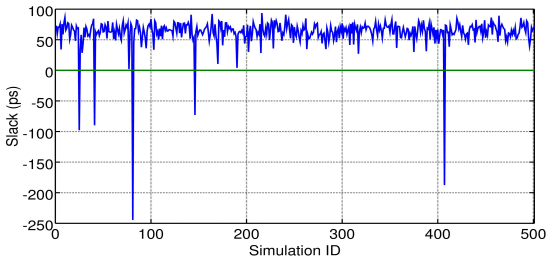


Fig. 11: Critical path slack with an RO clock source.

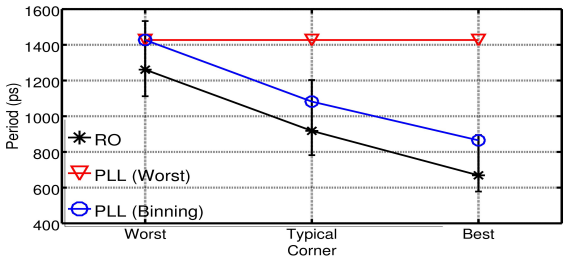


Fig. 12: PLL vs. RO performance.

been executed. On-chip variability has been modeled with different PVT parameters. For process variability, transistor models have been randomly generated with a probability distribution of V_{th} following a normal distribution $N(V_{\text{th}}, \sigma^2_{V_{\text{th}}})$, where $3\sigma_{V_{\text{th}}} = 0.4V_{\text{th}}$ (ITRS [20]). The maximum temperature difference with respect to the RO has been set to 4°C as in [16] and the maximum voltage difference between the RO and other circuit cells has been set to 14mV, as estimated in Section VI-A. The margin of the RO clock has been calculated for a yield of 97% (see (13) in appendix) and set to 162ps.

Fig. 11 shows the minimum time slack when the circuit is driven by the RO clock. From a total of 500 different circuit configurations and simulations (each one with its own global and local PVT conditions), failures (negative slack) have only been produced in five of them. Note that the number of failing simulations is less than the desired yield, a result that validates our timing model.

D. PLL vs RO clock performance

Fig. 12 shows the performance of circuit when the clock is driven by a PLL or by an RO clock. Two cases are considered when defining the PLL frequency: worst-case sign-off and speed binning. For worst-case sign-off, the frequency determined by the worst corner is assigned to all dies. For speed binning, each die is assigned the best possible frequency according to its process parameters (this is an optimistic assumption for binning).

Three process corners (best, typical, and worst) have been analyzed. When analyzing the PLL, worst local process variation has been assumed on each cell in order to determine the clock period. Similarly, voltage and temperature have been set to their worst value, which is determined by the library. Temperature is set to 125°C and voltage is set to 832mV, which is the minimum achievable voltage (considering global and local variations).

The RO clock period has been measured for the same three process corners. For each process corner, the average RO clock period is shown. To compute the average RO clock period, temperature has been set to 75°C, as it is the average estimated temperature along time. The voltage is set to 940mV, as it has been measured in Sec. VI-A to be the average voltage of the circuit when all AES modules are active.

Fig. 12 also shows the interval between the minimum and maximum RO achievable clock period. These values represent the theoretical minimum and maximum RO clock period if worst/best local PVT conditions remain unalterable along time. The maximum RO clock period is computed when the RO temperature and voltage are at 125°C and 832mV, respectively, and all the cells of the RO suffer the worst on-chip process variation. On the contrary, the minimum RO clock period is achieved when temperature and voltage are at 25°C and 1V (nominal voltage), and all cells of the RO have the best on-chip process variation.

Results show that the RO clearly outperforms PLL in all the analyzed corners. When no binning is applied, RO performance is 11.63%, 35.67%, and 53.12% larger than PLL for the worst, typical, and best corners, respectively. If perfect binning takes place for the PLL, the RO still outperforms the PLL. In this case, conservative improvements of 11.63%, 15.16%, and 22.66% are achieved. These benefits would be improved if realistic binning procedures are assumed.

VII. Conclusions

Guardband margins for covering static and dynamic variability have a significant impact on power and performance. This paper has presented a statistical analysis on the margins required for delay lines when used either for asynchronous circuits with bundled data or synchronous circuits with ring oscillator clocks.

In the future we envision more efforts towards techniques that can instantaneously adapt to dynamic variations at the expense of using clock generators with fluctuating frequencies that can better explore power/performance trade-offs at runtime.

Appendix

A. Introducing on-chip variability in a timing model

Given a PVT corner, the delay D of a gate can be modeled by a well-accepted expression:

$$D \propto \frac{V}{\mu(T)(V - V_{\text{th}_0})^{\alpha}} \tag{11}$$

where V, μ, V_{th_0}, and T, represent the supply voltage, carrier mobility, voltage threshold, and temperature, respectively, at a given corner [21], [22]. α ($\in [1, 2]$) is a technological parameter related to transistor velocity saturation.

When considering on-chip variability, the delay of a gate at time t, denoted as $D(t)$, can be decomposed as follows:

$$D(t) = D^0 + D_{\text{ocv}}(t)$$

where $D_{\text{ocv}}(t)$ represents the on-chip variations. $D_{\text{ocv}}(t)$ can be decomposed into three different terms representing the PVT variations:

$$D_{\text{ocv}}(t) = D^P + D^V(t) + D^T(t)$$

Each source of variability can be approximated linearly using a first-order Taylor expansion around the nominal value of the corner:

$$\begin{aligned} D^P &= \left.\frac{\partial D}{\partial V_{\text{th}}}\right|_0 (V_{\text{th}} - V_{\text{th}_0}) \\ D^V(t) &= \left.\frac{\partial D}{\partial V}\right|_0 (V(t) - V) \\ D^T(t) &= \left.\frac{\partial D}{\partial T}\right|_0 (T(t) - T) \end{aligned}$$

where $\frac{\partial D}{\partial X}\big|_0$ represents the first derivative of the delay (11) with respect to parameter X, measured at the nominal value of the corner.

Under the assumption that V_{th} is a statistical random variable that follows a Gaussian distribution $N(V_{\text{th}_0}, \sigma^2_{V_{\text{th}}})$, D_P can be modeled as another Gaussian distribution $N(0, \sigma^2_P)$, where

$$\sigma_P = \frac{\partial D}{\partial V_{\text{th}}}\bigg|_0 \sigma_{V_{\text{th}}}.$$

B. Defining margins for a rigid clock

Let's define $D_{L_i}(t)$, $D_{C_i}(t)$ as the delay of the launching and capturing paths of the ith critical path with L and C gates, respectively. Both delays follows a normal distribution as defined in (5). That is, $D_L(t) \sim N(D^0_L + D^{VT}_L(t), \sigma^2_L)$ and $D_C(t) \sim N(D^0_C + D^{VT}_C(t), \sigma^2_C)$. We assume that capturing and launching paths have a similar variance-to-mean ratio (index of dispersion). Then:

$$\frac{\sigma^2_L}{D_L} \approx \frac{\sigma^2_C}{D_C} \tag{12}$$

Let's define P and J as the PLL clock period and its jitter. In this case, the setup constraint for a critical path at a given corner is defined as:

$$S_i = P - J + D_{C_i}(t) - D_{L_i}(t) > 0$$

Given the statistical nature of launching and capturing paths, circuit timing correctness is achieved when the clock period is larger than any critical path delay with a probability Y (yield). In a circuit with N critical paths,

$$P(\cap_{i=1}^{N} S_i > 0) \geq Y$$

Assuming that the N critical paths are identical ($S = S_i, \forall i$) and uncorrelated[4], we could redefine the previous expression as:

$$P(S > 0)^N = \Big(1 - P(S < 0)\Big)^N \geq Y \tag{13}$$

where $P(S \leq 0)$ is the well-known cumulative distribution function (CDF) of the normal distribution $S \equiv N(\mu_{PLL}, \sigma^2_{PLL})$ such as:

$$\mu_{PLL} = P - J + D^0_C + D^{VT}_C(t) - D^0_L + D^{VT}_L(t) \tag{14}$$

Using (12), we can quantify σ^2_{PLL} as:

$$\sigma^2_{PLL} = \sigma^2_L + \sigma^2_C = \left(1 + \frac{D^0_C}{D^0_L}\right)\sigma^2_L \tag{15}$$

After introducing the normal distribution CDF into (13):

$$\left(1 - \frac{1}{2}\big(1 + \text{erf}(\frac{-\mu_{PLL}}{\sqrt{2}\sigma_{PLL}})\big)\right)^N \geq Y.$$

where erf is the error function (and its complementary is erfc). Last expression can be reordered as:

$$\mu_{PLL} \geq \Psi\sigma_{PLL} \tag{16}$$

where Ψ is a design parameter that depends on the number of critical paths and the desired yield (Y):

$$\Psi = \sqrt{2} \cdot \text{erfc}(2(1 - Y^{1/N})) \tag{17}$$

When introducing (14) and (15) into (16), we obtain the PLL clock period accounting for on-chip variability:

$$P \geq (D^0_L - D^0_C) + J + \Psi\sigma_{PLL} + D^{VT}_L(t) - D^{VT}_C(t)$$

[4]This assumption is not completely true as part of the OCV is common to all critical paths. However, this assumption is conservative as it generates an upperbound for the clock source period

As it can be seen, the clock period of the PLL can be defined as its nominal period in a given corner ($D^0_L - D^0_C$) plus some additional margins to cover on-chip PVT and jitter variations.

C. Defining margins for an RO clock

Similar to previous analyses, it is possible to compute the required RO clock period to cover on-chip variations. Let's define $D_{RO}(t)$ as the delay of the RO defined as in (5). That is, $D_{RO}(t) \sim N(D^0_{RO} + D^{VT}_{RO}(t), \sigma^2_{RO})$. In this case, the setup constraint for any critical path at a given corner is:

$$R_i = D_{RO}(t) + D_{C_i}(t) - D_{L_i}(t) > 0 \tag{18}$$

Analogous to the PLL, we can assume that all critical paths are identical and independent ($R = R_i, \forall i$). Thus, we can define R as a normal distribution $R \sim N(\mu_R, \sigma^2_R)$, where:

$$\mu_R = D^0_{RO} + D^{VT}_{RO}(t) + D^0_C + D^{VT}_C(t) - D^0_L - D^{VT}_L(t) \tag{19}$$

Using (12), we can quantify σ^2_R as:

$$\sigma^2_R = \sigma^2_L + \sigma^2_C + \sigma^2_{RO} = \left(1 + \frac{D^0_C}{D^0_L} + \frac{D^0_{RO}}{D^0_L}\right)\sigma^2_L \tag{20}$$

Performing the same mathematical analysis as in the PLL approach, we can obtain the RO clock period considering on-chip variations:

$$D^0_{RO} \geq (D^0_L - D^0_C) + \Psi\sigma_R + D^{VT}_L(t) - D^{VT}_{RO}(t) - D^{VT}_C(t) \tag{21}$$

Like in PLLs, the RO clock period can be defined as its nominal period in a given corner ($D^0_L - D^0_C$) plus some additional margins to only cover PVT variations.

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