

On the Selection of On-Chip Inductors for the Optimal VCO Design

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Abstract—The selection of on-chip inductors is crucial to the design of low phase noise voltage controlled oscillators (VCO's). In this paper, we study the effect of substrate on the inductor selection criterion for the VCO circuit and resolve the long lasting argument among circuit designers about whether large or small inductors should be used to reduce the phase noise of VCO's. Several substrate types including CMOS, SOI, and substrates with patterned ground shields (PGS's) are compared, and we demonstrate that the substrate resistivity plays a key role in determining the selection criterion of the optimal on-chip inductors for VCO design.

I. INTRODUCTION

The voltage controlled oscillator is a key component in many modern communication circuits where up and down frequency conversion is needed to effectively transmit the signal. Due to its good phase noise performance and relative ease of implementation, the LC-VCO has attracted much research interest in the past few years. The most basic form of an LC-VCO, as shown in Fig. 1, consists of an LC tank with two pairs of cross-coupled MOS transistors used to replenish the energy dissipated by the parasitic conductance of the tank. Despite the simplicity of the architecture, the integration of the LC-VCO into Si CMOS technology has posed many challenges to circuit designers due to the semiconducting nature of the silicon substrate, which severely limits the quality factor Q of the tank. Since the on-chip inductor is usually the most lossy component in the circuit, and thus one of the most significant determining factors of the phase noise, many designers have chosen to take an inductor centered design strategy where the best inductor is first selected within the design constraints and then other circuit components are sized and optimized assuming the design of the inductor does not change.

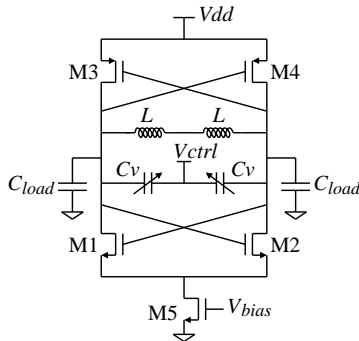


Fig. 1. Schematic of an LC-VCO.

In the literature, we can find two conflicting arguments about how inductors should be selected to effectively reduce the phase noise of VCO's. Some authors have proposed that the inductors in the LC tank should be made as large as possible without violating the tuning range constraints [1][2] while others believe that small inductors should be used instead, provided that the tank amplitude constraint and the startup condition are satisfied [3]. In this paper, we extend the

physical model of on-chip inductors proposed in [4] by incorporating the well known proximity effect and demonstrate that the variation of phase noise with inductance L depends critically on the resistivity of the substrate over which the inductor is fabricated. Thus, both previous arguments about how the optimal inductors should be selected are valid but *only* apply to some specific fabrication technologies. We have studied the inductor selection criterion for a broad range of substrate types, including CMOS, SOI, and substrates with patterned ground shields (PGS's) [5], and we show that although for high resistivity substrates, such as SOI, larger inductors are always better to reducing the phase noise, the opposite may be true as the substrate resistivity becomes smaller. To the best of our knowledge, this is the first systematic study of the substrate effect on the inductor selection criterion in LC-VCO design.

II. MODELING OF THE ON-CHIP INDUCTOR

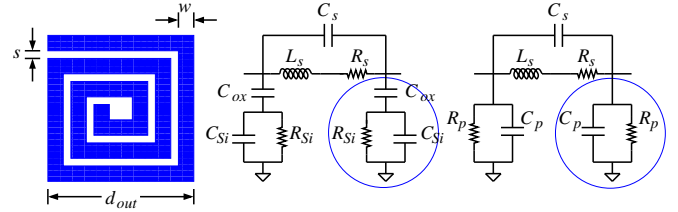


Fig. 2. (a) Schematic of a 3 turn on-chip square spiral inductor. (b) Physical model of the on-chip spiral inductor. (c) Inductor model with the parallel equivalent substrate network. The circled sub-circuits are equivalent to each other at the oscillation frequency of the VCO.

On-chip inductors are usually implemented by spiral structures fabricated on top metal layers. They can have different shapes such as square and octagonal; they can be either symmetric or nonsymmetric; and they can be implemented using either a single metal layer or multiple metal layers. The analysis of inductors with different geometries are similar although the equations used to calculate the inductance values may be different. To keep the computation simple and to be consistent with the structures studied in [3], which will be used in the paper for comparison purposes, we have only considered the square spiral inductors here. Fig. 2(a) and (b) show the schematic of a square spiral inductor and its physical model as proposed in [4], respectively. The spiral inductor is characterized by the number of turns n , the outer length d_{out} , the metal width w , and the metal spacing s . The DC inductance L_s can be computed accurately using Grover's formula [6] and Greenhouse's method [7]. However, in this work, we adopt a well verified simple expression [8] to compute L_s which gives

$$L_s = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5} \quad (1)$$

where $d_{avg} = 0.5(d_{out} + d_{in})$, $\beta = 1.66 \cdot 10^{-3}$, $\alpha_1 = -1.33$, $\alpha_2 = -0.125$, $\alpha_3 = 2.50$, $\alpha_4 = 1.83$ and $\alpha_5 = -0.022$. Here, the number of turns n is assumed to be an integer such that the inner diameter of the spiral d_{in} is well defined.

The lumped circuit elements C_s , C_{ox} , R_{Si} and C_{Si} model the capacitance between the spiral and the underpass, the oxide capacitance, and the parasitic resistance and capacitance of the substrate, respectively. They can be computed using

$$C_s = \epsilon_{ox} n w^2 / t_{su} \quad (2)$$

$$C_{ox} = \epsilon_{ox} l w / t_{ox} \quad (3)$$

$$R_{Si} = 2 / (G_{sub} l w) \quad (4)$$

$$C_{Si} = (C_{sub} l w) / 2 \quad (5)$$

where ϵ_{ox} is the dielectric permittivity of the oxide, t_{su} is the thickness of the oxide between the spiral and the underpass, t_{ox} is the thickness of the oxide between the spiral and the substrate, l is the total length of the spiral, and G_{sub} and C_{sub} are the conductance and capacitance per unit area of the substrate, respectively [4].

The computation of R_s deserves some more consideration because of the skin effect and proximity effect that occur at RF frequency range. Both effects tend to re-distribute the current and result in a reduction in the effective cross-sectional area through which the current can flow. Thus, R_s will increase as the operating frequency of the inductor increases. The following expression was used in [3] and [4]

$$R_s = l / (\sigma w \delta (1 - e^{-t_{metal}/\delta})) \quad (6)$$

where σ and t_{metal} are the conductivity and thickness of the metal layer respectively, and $\delta = \sqrt{2 / (\omega \mu_0 \sigma)}$. Here $\omega = 2\pi f$ where f is the frequency, and μ_0 is the magnetic permeability of free space. Equation (6) takes into account the skin effect only. However, as shown in [9], the proximity effect comes into play even earlier than the skin effect, becoming significant in increasing the effective resistance of the inductor at frequencies as low as a few hundred MHz. As a result, it is crucial to incorporate the proximity effect into the inductor model in order to correctly evaluate the performance of the device.

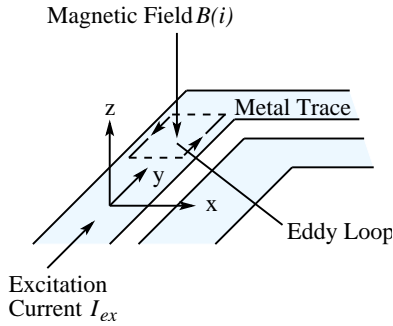


Fig. 3. Eddy current loop in a metal trace due to proximity effect.

Let $B(i)$ be the magnetic field at the i^{th} turn of the spiral as shown in Fig. 3. If we assume that the excitation current I_{ex} passing through the inductor is sinusoidal, then the induced eddy current density at distance x from the center axis of the i^{th} turn due to proximity effect is given by

$$J_{eddy}(x) = \sigma w B(i) x \quad (7)$$

Thus, the power dissipated in the i^{th} turn due to eddy current can be computed as

$$P_{eddy}(i) = \int_{-\frac{w}{2}}^{\frac{w}{2}} R_{\square} \frac{l_i}{dx} (\sigma w B(i) x \cdot t_{metal} dx)^2 \quad (8)$$

where R_{\square} is the sheet resistance of the metal layer and l_i is the total length of the i^{th} turn. The integral in (8) is obtained by meshing the metal trace into filaments with width dx each and summing the

power consumed by all the filaments due to eddy current. Let $B(i) = K(i) I_{ex}$ where the computation of $K(i)$ is given in [10], and recall that $R_{\square} = \frac{1}{\sigma t_{metal}}$. Then $P_{eddy}(i)$ becomes

$$P_{eddy}(i) = \frac{l_i \omega^2 [K(i)]^2 w^3}{12 R_{\square}} I_{ex}^2 \quad (9)$$

This is equivalent to an added series resistance of $\frac{l_i \omega^2 [K(i)]^2 w^3}{12 R_{\square}}$. Thus, the total R_s including both skin effect and proximity effect is given by

$$R_s = \frac{l}{\sigma w \delta (1 - e^{-t_{metal}/\delta})} + \sum_{i=1}^n \frac{l_i \omega^2 [K(i)]^2 w^3}{12 R_{\square}} \quad (10)$$

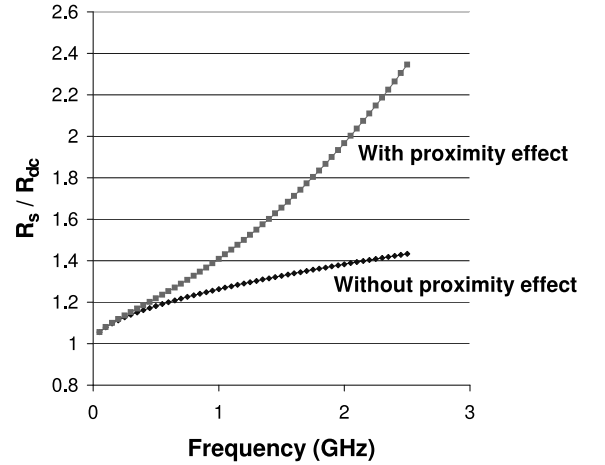


Fig. 4. Series resistance R_s versus frequency.

The significance of including the proximity effect into the model can be clearly seen in Fig. 4 where a 3 turn inductor with $d_{out} = 300 \mu\text{m}$, $w = 20 \mu\text{m}$ and $s = 10 \mu\text{m}$ is simulated. The sheet resistance and the metal thickness are assumed to be $20 \text{ m}\Omega/\square$ and $1.2 \mu\text{m}$, respectively. The inductor is $5 \mu\text{m}$ above the substrate and the substrate resistivity is chosen to be $10 \Omega\text{-cm}$. The DC inductance is found to be $L_s = 2.95 \text{ nH}$, and the effective series resistance R_s , measured in terms of the DC series resistance R_{dc} , is plotted against the operating frequency of the inductor. Without the proximity effect, R_s is approximately proportional to the square root of the frequency, which is a characteristic of the skin effect. When the proximity effect is included, however, it dominates the skin effect, and the growth of R_s with frequency becomes almost quadratic. This is consistent with the analysis and observation given in [9] and [10]. We also used ASITIC [11] to find the self-resonant frequency of the inductor, which is approximately 6GHz. Thus, we conclude that the proximity effect becomes much more significant than the skin effect well before the self-resonance of the inductor is reached and it must be considered in any RF circuit design.

III. MINIMIZATION OF THE PHASE NOISE

We assume that the VCO works in the current-limited regime because a voltage limited VCO will either result in a waste of inductance or a waste of power [3]. It is shown in [3] that in the current-limited regime, the phase noise $\mathcal{L}\{f_{off}\}$ of the LC-VCO shown in Fig. 1 is proportional to $L_{tank}^2 g_{tank}^2$ for a specific I_{bias} , where L_{tank} and g_{tank} are the equivalent tank inductance and conductance, respectively.

To assist the circuit analysis, it is advantageous to transform the substrate circuit in Fig. 2(b) to its equivalent parallel form in Fig. 2(c). The shunt resistance R_p and the shunt capacitance C_p are given by

$$R_p = \frac{1 + [\omega R_{Si}(C_{Si} + C_{ox})]^2}{\omega^2 R_{Si} C_{ox}^2} \quad (11)$$

$$C_p = \frac{C_{ox} + \omega^2 R_{Si}^2 (C_{Si} + C_{ox}) C_{Si} C_{ox}}{1 + [\omega R_{Si}(C_{Si} + C_{ox})]^2} \quad (12)$$

Hence for the VCO circuit in Fig. 1, the tank inductance and conductance can be computed using

$$L_{tank} = 2L_s + \frac{(2R_s)^2}{2\omega^2 L_s} \quad (13)$$

$$g_{tank} \approx g_L = \frac{1}{2R_p} + \frac{1}{2R_s + \omega^2(2L_s)^2/(2R_s)} \quad (14)$$

where, as in [3], we have assumed that the tank loss is primarily due to the inductor.

Since the phase noise is proportional to $L_{tank}^2 g_{tank}^2$, we formulate the following optimization problem

$$\begin{aligned} \text{minimize} \quad & N_{vco}(n, d_{out}, w, s) = L_{tank}^2 g_{tank}^2 \quad (15) \\ \text{subject to} \quad & 2nw + 2(n-1)s < d_{out} \\ & 0 < d_{out} \leq d_{max} \\ & n, w, s > 0, \quad n \text{ is an integer} \end{aligned}$$

where d_{max} is the maximum allowed outer length of the inductor. Here, the first constraint is to ensure that the sum of metal widths and spacings does not exceed the outer length of the inductor. For each inductance value L_s ranging from 1nH to 8nH with an increment of 0.25nH per step, we perform the optimization to obtain the minimum N_{vco} . Then we plot the minimum N_{vco} against L_s to see whether larger inductors or smaller inductors are better to reducing the phase noise. In this work, the minimum N_{vco} at each L_s is obtained through enumeration, where we loop through n , d_{out} , w , and s , pick out all the designs whose DC inductance is within 5% error of the expected L_s , and find the one that has the minimum N_{vco} .

IV. EXPERIMENTAL RESULTS

The inductor is assumed to be fabricated using a metal layer with sheet resistance $R_\square = 20m\Omega/\square$ and rests $5\mu\text{m}$ above the substrate. Three types of substrates with different resistivities are studied in this work:

- 10 Ω -cm (lightly doped CMOS and BiCMOS)
- 200 Ω -cm (SOI)
- 10 Ω -cm with PGS

The effect of the PGS is to eliminate the electric coupling from the inductor to the substrate and it will make R_p go to infinity in the ideal situation. According to [9], the eddy current loss in the substrate can be safely ignored for resistivities above 10 Ω -cm.

Fig. 5(a) and (b) show the minimum $L_{tank}^2 g_{tank}^2$, obtained from solving the optimization problem, versus the series inductance L_s of each spiral at the intended oscillation frequency of 2.4GHz and 5GHz, respectively. Note that for any particular L_s , the optimal design at the 2.4GHz frequency may be different from that at the 5GHz one. In the optimization loop, d_{max} is set to 300 μm , and n , D , w , s are incremented by 1 turn,¹ 1 μm , 0.5 μm , 0.5 μm each step, respectively. Recall that $L_{tank}^2 g_{tank}^2$ is proportional to the phase noise, we can see that when the substrate resistivity is 10 Ω -cm, the minimum phase noise increases with L_s as a general trend, which suggests that the use of small inductors in the design provides the best solution. However, when the substrate resistivity is 200 Ω -cm or when a PGS is inserted between the inductor and the substrate with a resistivity of 10 Ω -cm, the minimum phase noise decreases with L_s , which makes the large inductors the preferred choices. The minimum $L_{tank}^2 g_{tank}^2$ versus L_s curve is not very smooth because the number of turns n of the spiral is assumed to take only discrete values as pointed out above, and whenever one more turn is needed to realize a specific L_s value,

¹This choice is made because the d_{avg} term in the approximate inductance formula shown in Equation (1) is well defined only for integer number of turns.

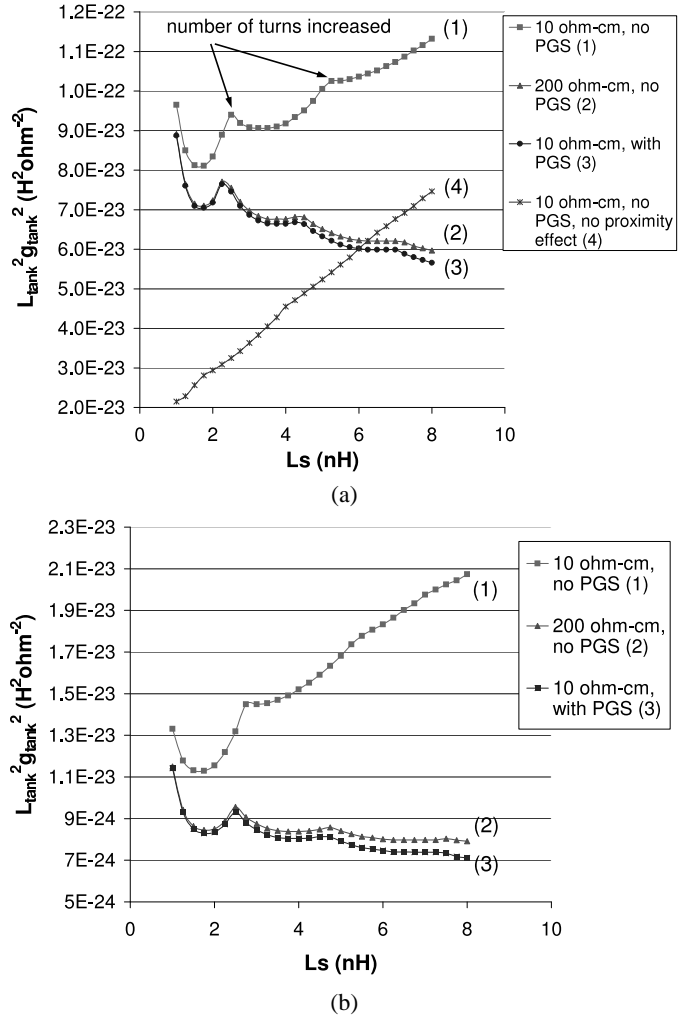


Fig. 5. $L_{tank}^2 g_{tank}^2$ versus L_s with different substrate resistivities and oscillation frequencies (a) 2.4GHz (b) 5GHz.

there is a discontinuous change in the effective series resistance R_s of the spiral due to the proximity effect. However, these kinks are relatively minor and the overall trend is easily visible on each curve.

An explanation of why the selection criterion of the optimal inductors should depend on the substrate resistivity is as follows:

- When a PGS is inserted between the inductor and the substrate, R_p goes to infinity in the ideal situation. Thus, for an inductor with reasonable Q , we have $L_{tank} \approx 2L_s$ and $g_{tank} \approx \frac{2R_s}{\omega^2(2L_s)^2}$, which implies that $L_{tank}^2 g_{tank}^2$ is proportional to $(R_s/L_s)^2$. Although larger L_s usually results in larger R_s , R_s does not increase as fast as L_s . Hence, the overall phase noise of the circuit will decrease as L_s increases, which is shown by the curves marked (3) in Fig. 5.
- When the substrate is involved, $1/(2R_p)$ will be added to g_{tank} . The substrate resistance R_p will generally decrease as L_s increases because a larger inductor implies a larger overlap area between the metal winding and the substrate. As a result, R_p tends to increase g_{tank} as L_s increases. When the substrate resistivity is very high (200 Ω -cm), R_p will be very large. This can be seen from (11), where R_p tends to infinity as R_{Si} tends to infinity. In this case, g_{tank} is completely dominated by the term involving R_s and we will observe the same trend as when the PGS is present, i.e., the phase noise decreases as L_s increases (curves marked (2) in Fig. 5).
- When the substrate resistivity is 10 Ω -cm, however, the effect of R_p can no longer be ignored. Although the overall g_{tank}

still decreases as L_s increases, it decreases at a slower rate. Thus, the overall phase noise increases as L_s increases (curves marked (1) in Fig. 5).

- The phase noise is lower when the VCO is designed to oscillate at 5GHz rather than 2.4GHz because g_{tank} , which is approximately given by $\frac{1}{2R_p} + \frac{2R_s}{\omega^2(2L_s)^2}$, decreases as the frequency increases. This is in agreement with the result obtained in [11].

As a comparison, we also show in Fig. 5(a) the simulation result using the model proposed in [4] and used by [3], which does not include the proximity effect in the spiral. It can be clearly seen that using this simplified model, the phase noise is severely underestimated while the advantage of using small inductors is significantly overestimated, i.e., a more than three times reduction in phase noise when L_s changes from 8nH to 1nH. Both of these two observations can be explained by the fact that the series resistance R_s is underestimated if the proximity effect is ignored, which leads to an underestimation of the $\frac{1}{2R_s + \omega^2(2L_s)^2/(2R_s)} \approx \frac{2R_s}{\omega^2(2L_s)^2}$ term in the expression of g_{tank} . Since the significance of the proximity effect has been well demonstrated in the literature, we believe that our work provides a more accurate guidance for the selection of inductors in an LC-VCO design.

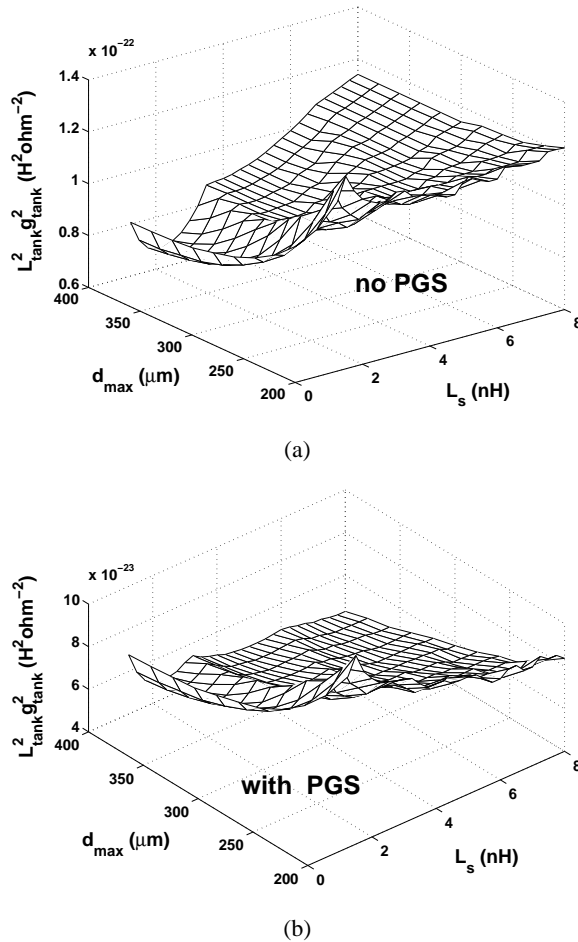


Fig. 6. 3D plot of $L_{tank}^2 g_{tank}^2$ versus L_s and d_{max} at 2.4GHz. The substrate resistivity is $10\Omega\cdot\text{cm}$. (a) no PGS is used (b) PGS is inserted between the inductor and the substrate.

Fig. 5 was obtained by setting d_{max} to $300\mu\text{m}$ in the optimization problem, where d_{max} is the maximum allowed outer length of the inductor. In our experiment, we also varied d_{max} to see its effect on phase noise. Fig. 6 shows a 3D plot of $L_{tank}^2 g_{tank}^2$ versus L_s and d_{max} for the substrate resistivity of $10\Omega\cdot\text{cm}$ and oscillation frequency

of 2.4GHz. A slicing of Fig. 6 at $d_{max} = 300\mu\text{m}$ and parallel to the L_s axis will give the curves marked (1) and (3) in Fig. 5(a). It can be seen that although d_{max} has some effect on $L_{tank}^2 g_{tank}^2$, the basic trend of the minimum phase noise versus L_s is maintained regardless of the choice of d_{max} . Specifically, in Fig. 6(a), the general trend of phase noise increases with L_s for any particular d_{max} , while in Fig. 6(b), it reduces as L_s increases.

To summarize, the answer to the question of whether large or small inductors should be used in VCO design depends on the substrate property and many other factors in the design and fabrication technology. A general rule of thumb is that when g_{tank} is dominated by R_s , large inductors are usually preferred, while when the effect of R_p starts to become significant, small inductors may be used. Thus, before a designer can select the inductors for the VCO, a simulation/optimization run similar to that shown in this paper will be very helpful.

V. CONCLUSION

In this paper, we first extended the physical model of on-chip inductors proposed in [4] by including the important proximity effect. Then we used the enhanced model to study the selection criterion of on-chip inductors for the optimal LC-VCO design. We resolved the long lasting question among circuit designers about whether large or small inductors should be used to minimize the phase noise of VCO by showing that the selection of optimal inductors depends critically on the substrate resistivity and whether a PGS is used in the design.

As a future work, we will study the optimal selection criterion for inductors fabricated over low resistivity substrates, which typically have a resistivity in the order of $0.01\Omega\cdot\text{cm}$ to $1\Omega\cdot\text{cm}$. One complication that may arise in this situation is that the substrate eddy current loss can no longer be ignored, which will affect both the effective L_{tank} and g_{tank} . The modeling of substrate eddy current has been discussed in [11] and [12], and it will be used in our study of the low resistivity substrates.

REFERENCES

- [1] B. Razavi, "A 1.8GHz CMOS Voltage-Controlled Oscillator," *Digest of Technical Papers, IEEE International Solid-State Circuit Conference*, pp. 388-389, Feb. 1997.
- [2] J. Kim *et al.* "A Power-Optimized Widely-Tunable 5-GHz Monolithic VCO in a Digital SOI CMOS Technology on High Resistivity Substrate," *Proceedings of the 2003 International Symposium on Low Power Electronics Design*, pp. 434-439, Aug. 2003.
- [3] D. Ham and A. Hajimiri, "Concepts and Methods in Optimization of Integrated LC VCOs," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 896-909, Jun. 2001.
- [4] C. P. Yue and S. S. Wong, "Physical Modeling of Spiral Inductors on Silicon," *IEEE Transactions on Electron Devices*, vol. 47, no. 3, pp. 560-568, Mar. 2000.
- [5] C. P. Yue and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp. 743-752, May 1998.
- [6] F. W. Grover, *Inductance Calculations*, Van Nostrand, New York, NY, 1962.
- [7] H. M. Greenhouse, "Design of Planar Rectangular Microelectronic Inductors," *IEEE Transactions on Parts, Hybrids, and Packaging*, vol. 10, no. 2, pp. 101-109, Jun. 1974.
- [8] S.S. Mohan *et al.*, "Simple Accurate Expressions for Planar Spiral Inductances," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 10, pp. 1419-1424, Oct. 1999.
- [9] W. B. Kuhn and N. M. Ibrahim, "Analysis of Current Crowding Effects in Multiturn Spiral Inductors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 1, pp. 31-38, Jan. 2001.
- [10] J. M. Lopez-Villegas *et al.*, "Improvement of the Quality Factor of RF Integrated Inductors by Layout Optimization," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 1, pp. 76-83, Jan. 2000.
- [11] A. M. Niknejad, "Analysis, Simulation, and Applications of Passive Devices on Conductive Substrate," Ph. D. Thesis, UC Berkeley, CA, Spring, 2000.
- [12] W. B. Kuhn and N. K. Yanduru, "Spiral Inductor Substrate Loss Modeling in Silicon RFICs," *Microwave Journal*, pp. 66-81, Mar. 1999.