# Aging of Current DACs and its Impact in Equalizer Circuits

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***Abstract*—This paper illustrates the impact of temporal degradations due to aging on current digital-to-analog converters (IDACs) within the context of a feed-forward equalizer (FFE) that is used in high-speed links. Aging causes mismatch in the current mirror, a matching-critical building block of IDACs, which degrades IDAC performance. The work analyzes and models the effect of mismatch over IDAC performance metrics and demonstrates how this affects FFE behavior. Finally, a novel scheme for FFE recalibration to recover from this degradation is presented.**

## I. Introduction

Current-mode digital-to-analog converters (IDACs) are widely used in analog design. Their fast response times makes them well suited for use in high-speed link (HSL) circuits such as feed-forward equalizers [1], decision feedback equalizers [2], and linear equalizers [3]. Due to the high data rates and high activity in HSL circuits, IDACs in HSLs carry high currents and are subject to performance shifts due to aging. These performance shifts can induce non-linearities in an IDAC over time and non-monotonicity in the worst case.

In this work, we perform a detailed modeling study to analyze aging-induced temporal performance degradation of two IDAC topologies. We show how aging induces mismatch over time in matched transistors, and the induced mismatch affects IDAC behavior over time. We study the impact of aging within the context of an HSL circuit, a feed-forward equalizer (FFE), and propose a method to mitigate these effects. In contrast, prior studies on IDAC aging [4], [5] have examined aging in standalone current-steering DACs. We perform an application-driven analysis, examining the impact of IDAC aging in the context of the FFE circuit, and present a mitigation method to optimize the performance of the FFE. Our analysis incorporates the use of calibration methods used in analog systems to recover from performance drifts.

## II. Analysis of IDACs

### A. IDACs: Operating Principles

Two common configurations of an IDAC are the *current-steering* and *current-switching* DAC (Fig. 1). Both configurations use a current-mirror (CM) to convert an analog input current, $I_{in}$, to a scaled analog output current, $I_{out}$, using an $N$-bit coefficient, $(c_{N-1}c_{N-2}\cdots c_0)$, with decimal value $c$ as:

$$I_{out} = \left(\sum_i c_i \cdot \mathcal{R}_i\right) I_{in} \tag{1}$$

where $\mathcal{R}_i$ is the transfer ratio between the input current and the current through schematic transistor $M_i$, and is implemented by appropriately sizing the transistor ratios. In Fig. 1, this is achieved by binary-weighted sizing of the transistors in the CM, where each transistor in the schematic is sized at $2^i\times$ relative to $M_{ref}$. In FinFET technologies, each sized schematic transistor is implemented using multiple discrete FinFETs,

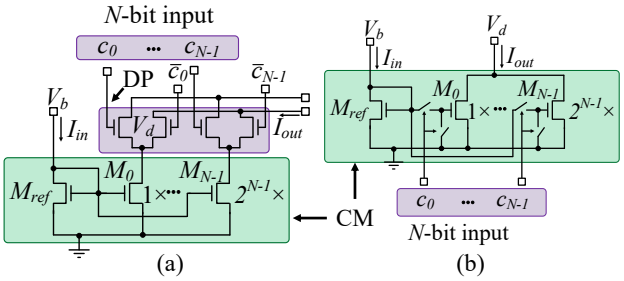


**Fig. 1.** Schematic of a (a) current-steering DAC, (b) current-switching DAC.

e.g., a $4\times$ transistor is implemented as four FinFETs.[1] The current-steering DAC also includes a set of differential pairs (DPs), which function in "digital mode" with input values at logic 1 or logic 0. For the DP, aging only affects the settling time of the output, and its impact can be minimized with wider transistors. On the other hand, as we will show, IDAC performance is very susceptible to CM aging.

**Notation:** We use the following notations:

- $M_i$: the $i^{\text{th}}$ transistor in the schematic ($0 \le i < N$).
- $M_{i,j}$: the $j^{\text{th}}$ FinFET in $M_i$ ($0 \le j < 2^i$).
- $\mathcal{R}_{i,j}$: FinFET transfer ratio, $(I_{M_{i,j}}/I_{M_{ref}})$ from the reference transistor current to the current in FinFET $M_{i,j}$.
- $\mathcal{R}_i$: transfer ratio of bit $i$, $(I_{M_i}/I_{M_{ref}})$ from the reference transistor current to the current in schematic transistor $M_i$.
- $\Delta[M_{ref}, M_{i,j}] = \Delta V_{th,M_{ref}} - \Delta V_{th,M_{i,j}}$: threshold voltage mismatch between FinFETs $M_{i,j}$ and $M_{ref}$.

The current through $M_i$ can be written as:

$$I_{M_i} = c_i \cdot \mathcal{R}_i = \textstyle\sum_j (c_i \cdot \mathcal{R}_{i,j})\, I_{in} \tag{2}$$

The total $I_{out}$ is the sum of currents through all $M_i$:

$$I_{out} = \left[\textstyle\sum_i (c_i \mathcal{R}_i)\right] I_{in} = \left[\textstyle\sum_i \sum_j (c_i \cdot \mathcal{R}_{i,j})\right] I_{in} \tag{3}$$

We use $V_{GS,M_{i,j}}$ and $V_{DS,M_{i,j}}$ to denote the gate-to-source and drain-to-source voltages, respectively, of $M_{i,j}$. In both IDAC configurations, $M_{ref}$ is a diode-connected transistor that converts an input current, $I_{in}$, to a voltage, $V_b$. Hence,

$$V_{GS,M_{ref}} = V_{DS,M_{ref}} = V_b \tag{4}$$

In the current-steering DAC, the gate node of each FinFET in $M_i, 0 \le i < N$, is always connected to $V_b$. In the current-switching DAC, the gate of $M_i$ is connected to $V_b$ if $c_i = 1$ (i.e., $V_{GS,M_i} = V_b$), or to ground if $c_i = 0$ (i.e., $V_{GS,M_i} = 0$).

In the ideal circuit, all FinFETs have identical threshold voltage, $V_{th,\mu}$. Process variations are nullified using larger transistor sizes and using layout techniques such as common-centroid. If $V_{GS,M_{i,j}} = V_b$, then for all FinFETs $M_{i,j}$ of $M_i$,

$$V_{DS,M_{i,j}} = V_d \approx V_b - V_{th,\mu} \tag{5}$$

[1] $M_{ref}$ could be implemented using $f$ FinFETs; if so, the other transistor sizes and indices could be scaled up by $f$. For ease of exposition, we assume a unit-sized $M_{ref}$.

These transistors are placed in saturation to maximize output current, and $V_d$ is chosen to maximize output swing.

The transfer ratio, $\mathcal{R}_{i,j} = I_{M_{i,j}}/I_{M_{ref}}$ for FinFET $M_{i,j}$ can be represented using the alpha-power law [6] as:

$$\mathcal{R}_{i,j} = \left[\frac{V_{GS,M_{i,j}} - V_{th,M_{i,j}}}{V_{GS,M_{ref}} - V_{th,M_{ref}}}\right]^{\alpha} \left[\frac{1+\lambda V_{DS,M_{i,j}}}{1+\lambda V_{DS,M_{ref}}}\right] \quad (6)$$

### B. Performance for the Ideal Case

Ideally, $V_{GS} = V_b$ and $V_{th} = V_{th,\mu}$, the nominal value, for all transistors. The circuit performance parameters are:

*FinFET transfer ratio:* For each FinFET $M_{i,j}$,

$$\mathcal{R}_{i,j} = \left[\frac{V_b - V_{th,\mu}}{V_b - V_{th,\mu}}\right]^{\alpha} \left[\frac{1+\lambda V_d}{1+\lambda V_b}\right] = \frac{1+\lambda V_d}{1+\lambda V_b} \triangleq r \quad (7)$$

*Transfer ratio of bit i:* The transfer ratio $\mathcal{R}_i$ for $M_i$ is:

$$\mathcal{R}_i = \textstyle\sum_{j=0}^{2^i-1} \mathcal{R}_{i,j} = 2^i \cdot r \quad (8)$$

*Finding $I_{out}$:* We combine Eqs. (1) and (8) to obtain:

$$I_{out} = \left[\textstyle\sum_i c_i \cdot 2^i \cdot r\right] I_{in} = c \cdot r \cdot I_{in} \quad (9)$$

*Gain:* Given the full-scale current, $I_{FS}$ ($c_i = 1\ \forall\ i$, i.e., $c = 2^N - 1$), the gain, $G = I_{FS}/(2^N - 1)$. Thus,

$$G = \frac{\sum_{i=0}^{N-1} \mathcal{R}_i I_{in}}{2^N - 1} = \frac{(2^N-1)\cdot r \cdot I_{in}}{2^N - 1} = r \cdot I_{in} \quad (10)$$

*DNL:* To compute DNL, we determine the step size, $I_{\Delta c}$, in the output current in moving from input word $c-1$ to $c$, and compare it with the ideal *Gain* for a single step (Eq. (10)):

$$\text{DNL}_c = (I_c - I_{c-1}) - r \cdot I_{in} \quad (11)$$

In the ideal case, $I_c - I_{c-1} = c\cdot r\cdot I_{in} - (c-1)\cdot r\cdot I_{in} = r\cdot I_{in}$, (from Eq. (9)). Hence, $\text{DNL}_c = 0$ for all $c$.

*INL:* The INL is the difference between actual output and ideal output for the input $c$, and can be represented as:

$$\text{INL}_c = I_c - c \cdot r \cdot I_{in} \quad (12)$$

For the ideal case, from Eq. (9), $\text{INL}_c = 0$ for all $c$.

## III. Aging Effects in IDACs

### A. Aging Model

We consider the impact of aging on FinFET-based IDAC circuits with n-type FinFETs. We focus on hot carrier degradaton (HCD) induced aging and ignore smaller PBTI shifts [7]. We extend the model in [8] to incorporate dependency of the threshold voltage shift to channel length using data from [9].

The impact of aging at time $t$ is modeled as:

$$\Delta V_{th} = V_{th}\left(1 - \exp\left[-\left(\beta \cdot t/\tau_L\right)^n\right]\right) \quad (13)$$

$$\begin{aligned} \text{where } \tau &= \frac{A}{\exp[\Gamma_{A2}(V_{DS})]} \exp\left[\Gamma_{A1}(V_{DS} - \gamma V_{GS})\right] \\ \tau_L &= \tau \exp\left[s\left(L - L_0\right)\right] \\ n &= n_0 \exp\left[-\left(\beta \cdot t/\tau_n\right)^{\kappa}\right] \\ A &= A_1 \exp\left[-E_a/(kT)\right] \end{aligned}$$

Here, $k$ is Boltzmann's constant; $L$ is the gate length; $\beta$ is the activity factor; the temperature $T = T_0 + T_{SH}$ where $T_0$ is the base temperature and $T_{SH}$ is the local temperature rise due to device self-heating. We incorporate self-heating using the equations in [8]. Other model parameters are: $\Gamma_{A1} = 3.85\text{V}^{-1}$, $\Gamma_{A2} = 9.40\text{V}^{-1}$, $\gamma = 5.2$, $s$ = 0.045s/nm, $L_0 = 14$nm, $n_0 = 0.8$, $\tau_n$ = $10^5$s, $\kappa = 0.036$, $A_1 = 6\times10^{13}$s, $E_a = -0.58\text{eV}^{-1}$.

### B. Performance Shifts due to Aging

A transistor only ages at the active state when it carries current. During normal operation, the $M_{ref}$ transistor is always active. In the current steering DAC, FinFETs $M_{i,j}$ in the CM are also always active, but in the current switching DAC, $M_{i,j}$ may be active or inactive, depending on $c_i$. Even if $M_{i,j}$ is active, from Eq. (5), $V_{DS,M_{i,j}} < V_{DS,M_{ref}}$.

Moreover, in a diode-connected configuration, at a constant current $I_{in}$, $V_{th}$ degradation in $M_{ref}$ implies that $V_{GS,M_{ref}}$ increases over time to maintain the $I_{in}$. This causes $V_{DS,M_{ref}}$ = $V_{GS,M_{ref}}$ to rise [10], further worsening the gap between $M_{ref}$ and $M_{i,j}$. Therefore, $M_{ref}$ typically undergoes more HCD aging than FinFETs $M_{i,j}$. The imbalance in aging rates leads to *mismatch* between transistors, quantified as:

$$\Delta[M_{ref}, M_{i,j}] = \Delta V_{th,M_{ref}} - \Delta V_{th,M_{i,j}} \quad (14)$$

The aging equation (13) models this mismatch, based on factors such as time, activity factor, and applied voltage.

We present expressions that quantify the impact of aging-induced shifts on IDAC performance parameters. Proofs for these expressions are provided in Appendix A.

*FinFET transfer ratio:*

$$\Delta\mathcal{R}'_{i,j} = \frac{\alpha \cdot r}{(V_b - V_{th,\mu})} \cdot \Delta[M_{ref}, M_{i,j}] \quad (15)$$

*Transfer ratio of bit i:*

$$\Delta\mathcal{R}'_i = \frac{\alpha \cdot r}{(V_b - V_{th,\mu})} \textstyle\sum_{j=0}^{2^i-1} \Delta[M_{ref}, M_{i,j}] \quad (16)$$

$$\textit{I}_{out}\textit{:} \quad \Delta I_{out} = I_{in} \textstyle\sum_{i=0}^{N-1} c_i \Delta\mathcal{R}'_i \quad (17)$$

$$\textit{Gain:} \quad \Delta G = \frac{I_{in}}{2^N - 1} \textstyle\sum_{i=0}^{N-1} \Delta\mathcal{R}'_i \quad (18)$$

$$\textit{DNL:} \quad \text{DNL}_c = I_{in} \textstyle\sum_{i=0}^{N-1} \left[c_i - (c-1)_i\right] \Delta\mathcal{R}'_i \quad (19)$$

$$\textit{INL:} \quad \text{INL}_c = I_{in} \textstyle\sum_{i=0}^{N-1} c_i \Delta\mathcal{R}'_i \quad (20)$$

Note that all terms depend on the mismatch, $\Delta[M_{ref}, M_{i,j}]$.

## IV. FFE Circuit Structure

The FFE is a multi-tap multi-level transmit equalizer that reduces inter-symbol interference (ISI) when data is transmitted through a wired channel. The transmitted data bounces between two voltage levels, $V_{Tx}^{max}$, and $V_{Tx}^{min}$. The channel is band-limited and attenuates the high-frequency contents of the Tx pulse, causing its energy to be dispersed over adjacent pulse positions, potentially resulting in Rx side errors. This issue is countered by shaping the pulse, transmitting a weighted sum of past, present, and future pulse(s) (with negative weights for adjacent pulses). The weights are regulated by coefficients that can be adjusted adaptively (e.g., during each power-up) using an up-channel link protocol [11]. An automatic level control algorithm is used on the Tx side to maintain a fixed peak-to-peak output, $V_{Tx}^{max}$ to $V_{Tx}^{min}$, as coefficients change. Figs. 2(a) and (b) show an example of equalized pulse and its pulse

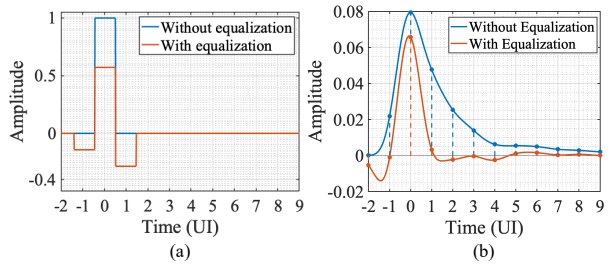


**Fig. 2.** An unequalized pulse with its precursor and postcursor, and its equalized output. The signal is sampled at integer multiples of the unit interval (UI), and the equalized signal provides low ISI at $t \leq -1$ and $t \geq 1$.

response, respectively. The narrower spread of the equalized pulse avoids ISI. The core of the FFE (Fig. 3) consists of:

**Taps** The FFE has $(p+q+1)$ taps: the main tap coefficient controls the weight of the main cursor, which is the message pulse to be transmitted, while a set of $p$ and $q$ taps control weights of precursors and postcursors, respectively.

**Delay Units (DUs)** The input bit stream propagates through a set of DUs that ensure that the precursor(s), main cursor, and postcursor(s) are fed to the FFE at the right time.

**Differential Pairs (DPs)** A set of DPs are used for each precursor, main cursor, and postcursor, to propagate each input bit to the channel using two complementary signals.

**IDACs** The IDACs convert each tap coefficient to an appropriately weighted multiple of a reference bias current, $I_{bias}$. The weights determine the relative importance of the main cursor, precursor(s), and postcursor(s).

**Resistive load** ($R_{load}$) The load terminates the transmission line at the transmitter side and corresponds to the characteristic impedance of the channel. The differential voltage drop across the resistive loads is the transmitted signal, $D_{Tx}$.

**XOR gates** Depending on the sign of the coefficient, detected using the sgn(.) function, an XOR gate sends data to DP for the pre/main/postcursors in either true or complemented form.

The DP is driven by two complementary digital inputs. It is relatively insensitive to aging, and only requires transistors to remain in the linear region even after aging. It is easy to ensure this. On the other hand, the IDACs, which translate the coefficient weights into precise analog currents, are very analog in nature, and undergo significant aging effects.

The current steering DAC is aging-resilient, as illustrated in Section VII, but, it can consume extra voltage headroom to accomodate DPs. This limits the output voltage swing [12], making it more susceptible to noise and perturbation. Hence, current switching DAC and circuits with similar topology, e.g., current-mode logic driver, are prevalent in HSLs. We will consider an FFE with a current-switching DAC, quantifying the impact of aging on FFE performance in Section V, and

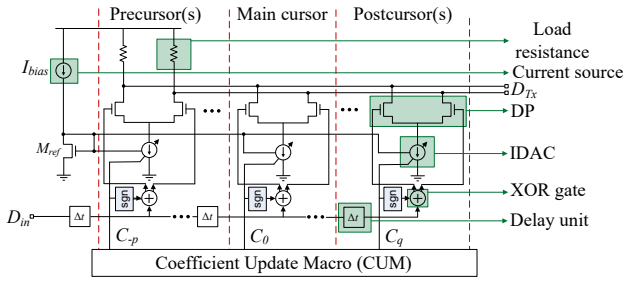


**Fig. 3.** Schematic of a feed-forward equalizer (FFE) architecture.

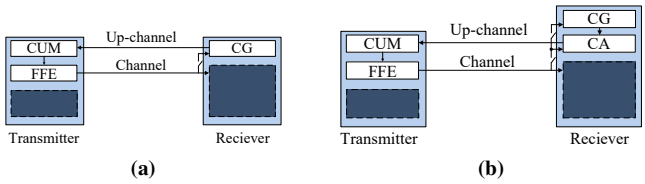


**Fig. 4.** (a) Conventional communication between Tx and Rx for the FFE. (b) Aging mitigation scheme with CA unit on the Rx side.

presenting a mitigation scheme for recalibration in Section VI.

## V. FFE Performance Analysis

### A. Operation under Nominal Conditions

A simplified diagram of a high-speed link, focusing on the parts that pertain to the equalizer, is shown in Fig. 4a: parts unassociated with the equalization process are encapsulated in black boxes. The process of equalization of the data to be transmitted consists of three steps:

**Step 1:** The FFE generates a pulse, $D_{Tx}$, at the operating frequency with an amplitude of $V_{Tx}^{max}$ on system power-up:

$$D_{Tx}(t) = V_{Tx}^{max} \cdot [u(t) - u(t-T)] \tag{21}$$

Here, $u(t)$ indicates unit step function and $T$ is the pulse width.

**Step 2:** The signal propagates through the channel, whose impulse response is $h(t)$, and creates a response at the receiver:

$$D_{Rx}(t) = (V_{Tx}^{max} \cdot [u(t) - u(t-T)]) * h(t) \tag{22}$$

**Step 3:** At the Rx end, the coefficient generator (CG) (Fig. 4a) samples the received signal, $D_{Rx}$. Under a fixed equalization scheme with a given number of $p$ past pulses (precursors) and $q$ future pulses (postcursors) to be used, along with the current pulse (main cursor), for equalization, the CG generates $(p+q+1)$ tap coefficients from $D_{Rx}$. The CG also requires the tap adjustment range of the main cursor. A tap adaptation algorithm, e.g., zero force (ZF) or minimum mean square error (MMSE) [13], is used to generate the FFE coefficients:

$$\mathbf{C} = \left[c^{-p}, \cdots, c^{0}, \cdots, c^{q}\right] \text{ where } \textstyle\sum_{j=-p}^{q} |c^{j}| = C^{tot} \tag{23}$$

As we will see in Eq. (26), the latter condition maintains a constant amplitude for the equalized signal.

**Step 4**: The computed coefficients are sent back by the CG module to the Tx side using an up-channel protocol, and the coefficient update macro (CUM), shown in Fig. 4a. The CUM stores and applies these coefficients to control the strength of each drivers, assembled using IDACs, and to appropriately emphasize or demphasize the precursor(s), main cursor, and postcursor(s) to generate the signal that is to be transmitted. The IDACs use the tap coefficients received from the CUM in binary form and use them to generate the weighted currents, using Eq. (2). These are represented by the weight vector:

$$\mathbf{W} = [I_{-p}, \cdots, I_0, \cdots, I_q] = I_{bias} \cdot r \cdot \left[c^{-p}, \cdots, c^{0}, \cdots, c^{q}\right]$$

Since in the ideal case, for tap $\tau$, $I_\tau = c^\tau \cdot r \cdot I_{bias}$ (Eq. (9)),

$$c^{-p} : \cdots : c^{0} : \cdots : c^{q} = I_{-p} : \cdots : I_0 : \cdots : I_q \tag{24}$$

$$I_{tot} = \textstyle\sum_{j=-p}^{q} |I_j| = C^{tot} \cdot r \cdot I_{bias} \tag{25}$$

With $(p+q+1)$ weights in the vector $\mathbf{W}$, the amplitude of equalized signal of FFE can be represented as follows:

$$V_{Tx}^{max} = I_{tot} \cdot R_{load} = (C^{tot} \cdot r \cdot I_{bias}) \cdot R_{load} \tag{26}$$

**Algorithm 1** Algorithm for obtaining coefficient vector $\mathbf{C}'$

**Input:** $I_i^\tau \ \forall\ 1 \le i \le N, -p \le \tau \le q$;
**Output:** Updated coefficient vector, $\mathbf{C}'$
**for** $\tau = -p : q : 1$ **do**
  **for** $i = N-1 : 0 : -1$ **do**
    $\xi_i^\tau = 0$;
    **if** $(I_{out}^\tau - I_i^\tau) \ge 0$ **then**
      $I_{out}^\tau = I_{out}^\tau - I_i^\tau$; $\xi_i^\tau = 1$;
    **end if**
  **end for**
**end for**

### B. Impact of Aging on the FFE

As explained in Section III, the transfer ratios of each branch of an IDAC may depart from ideal behavior under variations, shifting the weight vector $\mathbf{W}$ of the FFE to:

$$\mathbf{W}'(t) = \left[I'_{-p}(t), \cdots, I'_0(t), \cdots, I'_q(t)\right] \tag{27}$$

As the IDAC transistors age over time, they do not maintain Eq. (25) as the IDAC output currents change (Eq. (17)). Moreover, each IDAC is stressed with different coefficients, due to which transfer ratio of the IDAC can change. Hence,

$$I'_{-p}(t) : \cdots : I'_q(t) \neq I_{-p} : \cdots : I_q \quad ; \quad \sum_{j=-p}^{q} |I'_j(t)| \neq I_{tot}$$

## VI. Mitigating FFE Aging

In order to achieve correct equalization under aging, we must return the circuit to the original weight vector, $\mathbf{W}$. To achieve this, we dynamically adapt the coefficients $\mathbf{C}$ to a new set,

$$\mathbf{C}' = \left[\xi^{-p}, \cdots, \xi^0, \cdots, \xi^q\right] \tag{28}$$

where the coefficient vector for tap $\tau$ is $\xi^\tau = [\xi_1^\tau, \cdots, \xi_{N_\tau}^\tau]^T$.

Note that while $I_{bias}$ can be used as a knob to control $I_{tot}$, but is not effective against differential aging in each bit position as it cannot control each IDAC block individually, and the transfer ratio remains unchanged even if $I_{bias}$ is adjusted.

We propose a scheme to recalibrate the FFE after aging. Our proposed modification to the FFE architecture is shown in Fig. 4b. We add a coefficient adapter (CA) unit on the Rx side that maps coefficients $\mathbf{C}$ to $\mathbf{C}'$ before transmitting them to the CUM. The CA sits on the Rx side in order to incorporate the impact of the channel.

A key observation is that this recalibration is performed very seldom, while the equalizer is on during the entire operation of the circuit. Therefore, recalibrating circuitry can be assumed to be unaffected by aging shifts. The updated coefficients in $\mathbf{C}'$ are determined in four steps as follows:

**Step 1**: A pulse of amplitude $V_{max}^{Tx}$ at the operating frequency is propagated through the channel. The detected amplitude of the received signal is denoted as $V_{max}^{Rx}$. Since the transmitted pulse drives the same load, $R_{load}$, on the Tx side, the current through the $R_{load}$ is $I_{tot}$, i.e.,

$$V_{max}^{Tx} = I_{tot} \cdot R_{load} \tag{29}$$

**Step 2:** The Tx side sends a set of one-hot-encoded input signals for each FFE tap, also at the operating frequency. For each tap $\tau$, each input bit in $(c_{N_\tau-1}^\tau, \cdots, c_0^\tau)$ of tap $\tau$ of an FFE is set to 1 in turn; all other tap coefficients are set to 0. On the Rx side, the amplitude of the response to each signal is recorded. We denote the amplitude for the $i^{th}$ bit of tap $\tau$ as $\mathcal{V}_{i,\tau}^{Tx} = I_i^\tau R_{load}$, and that of the pulse response as $\mathcal{V}_{i,\tau}^{Rx}$.

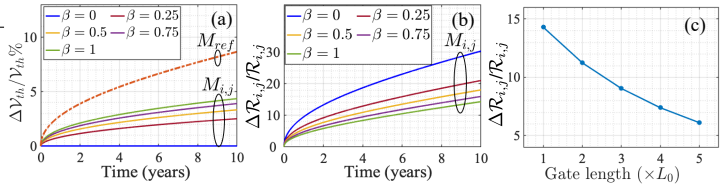


**Fig. 5.** (a) $V_{th}$ degradation of $M_{ref}$ and $M_{i,j}$ due to aging with varying $\beta$. (b) Change in transfer ratio of $M_{i,j}$ due to aging with varying $\beta$. (c) Change in transfer ratio of $M_{i,j}$ with varying gate length, $L$.

**Step 3:** Using the pulse response amplitudes in Steps 1 and 2, the CA calculates $I_i^\tau$ for the $i^{\text{th}}$ bit of tap $\tau$. Since the channel is a linear system, the ratio of the transmitted signal to the response for a fixed pulse shape is identical. Combining this observation with Eq. (29),

$$\frac{\mathcal{V}_{max}^{Tx}}{\mathcal{V}_{max}^{Rx}} = \frac{\mathcal{V}_{i,\tau}^{Tx}}{\mathcal{V}_{i,\tau}^{Rx}} \implies \frac{\mathcal{V}_{i,\tau}^{Rx}}{\mathcal{V}_{max}^{Rx}} = \frac{\mathcal{V}_{i,\tau}^{Tx}}{\mathcal{V}_{max}^{Tx}} = \frac{(I_i^\tau \cdot R_{load})}{(I_{tot} \cdot R_{load})}$$

$$\text{i.e., } I_i^\tau = \left(\mathcal{V}_{i,\tau}^{Rx} / \mathcal{V}_{max}^{Rx}\right) \cdot I_{tot} \tag{30}$$

**Step 4:** For each tap $\tau$, the current corresponding to the $i^{\text{th}}$ bit flows through transistor $M_i^\tau$ in Fig. 1. From (3), the output current of tap $\tau$ under the aged coefficient vector $\mathbf{C}'$ is:

$$I_{out}^\tau = \textstyle\sum_{i=0}^{N-1} \xi_i^\tau \cdot \mathcal{R}'_i \cdot I_{bias} = \sum_{i=0}^{N-1} \xi_i^\tau \cdot I_i^\tau \tag{31}$$

where $I_i^\tau = \mathcal{R}'_i \cdot I_{bias}$ is the current that $M_i^\tau$ can deliver.

The CA then calculates the required weights for equalization. The required current, $I_{out}^\tau$ for each tap $\tau$ is determined, given $I_i^\tau, \forall\{i,\tau\}$ derived in Eq. (30). The pseudocode for this purpose is shown in Algorithm 1 and is easily implemented in the CA at the Rx end for dynamic adaptation.

## VII. Results

We apply our models to the IDACs and FFE and illustrate the impact of aging on performance. We also demonstrate how our mitigation strategy can be used to ensure correct FFE behavior over its lifetime. Our results are based on simulations on a commercial 12nm FinFET technology, incorporating device-level aging models from Section III into HSPICE.

**IDAC Analysis:** Fig. 5(a) compares the $V_{th}$ degradation of $M_{ref}$ and FinFETs $M_{i,j}$ for the current-switching DAC, for various values of $\beta$. For the current-steering DAC, the gate of $M_{i,j}$ is always at $V_b$, i.e., $\beta = 1$. The mismatch induces an increase in the transfer ratio, $\Delta\mathcal{R}_{i,j}/\mathcal{R}_{i,j}$, of $M_{i,j}$ over time, as shown in Fig. 5(b) over a sweep of $\beta$. The mismatch is lowest for $\beta = 1$; hence, the current-steering DAC is more aging-resilient than the current-switching DAC. Aging-induced mismatch and the change in transfer ratio can be reduced by using higher gate-length: Fig. 5(c) shows that a gate length of $5L_0$, instead of $L_0$, reduces $\Delta\mathcal{R}_{i,j}$ by 57%.

As $\Delta\mathcal{R}_i$ increases over time, the IDAC gain $G$ also increases (Equation (18)). For a 6-bit current switching DAC, in 10 years of continuous aging, $\Delta G$ can drift by 14% (maximum stress: $c_i = 1 \forall 0 \le i < N$) to 29% (minimum stress: $c_i = 0 \forall 0 \le i < N$). As all CM transistors in a current-steering DAC are always active, the cumulative mismatch in transistors of current-steering DAC is the lowest. In the absence of any

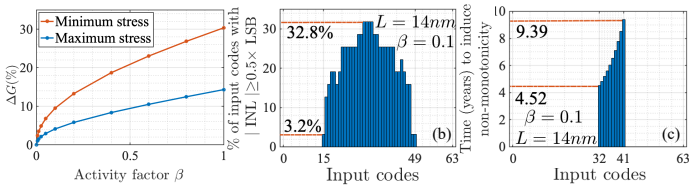


**Fig. 6.** Aging effects on 6-bit IDAC. Aging can (a) increase gain error, (b) increase INL, (c) induce non-monotonicity.

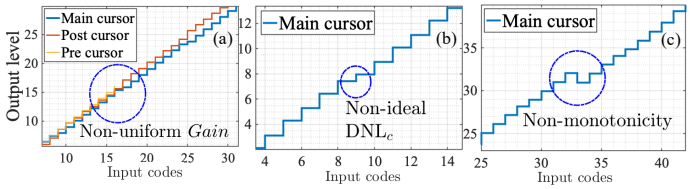


**Fig. 8.** Segments of the transfer curves that illustrate (a) non-idealities in Gain $G$, (b) non-idealities in DNL, and (c) nonmonotonicity.

recalibration of the IDAC, the integral nonlinearity (INL) and differential nonlinearity (DNL) also increase over time (Equation (19) and (20)). The maximum allowable |INL| and minimum allowable DNL are $\frac{1}{2}$LSB and $-1$LSB, respectively.

In modern chips, $\Delta G$ can be recalibrated to zero in IDACs by varying $I_{in}$. In a current-steering IDAC, such recalibration also minimizes DNL and INL, explained in Appendix B. However, in a current-switching DAC, recalibrating $\Delta G$ to zero by varying $I_{in}$ can induce non-monotonicity in the worst case. Our analysis shows that with zero $\Delta G$ and an activity factor, $\beta$, of 0.1, a fixed input code between 15 to 49 will induce an |INL| $>$ $\frac{1}{2}$LSB in 3.2% to 32.8% of the input codes in 10 years (Fig. 6(b)). If the input codes are evenly distributed between 15 to 49, there will be no INL violation, but for evenly distributed input codes between 15 to 31 and 32 to 49, which are probable cases for the IDACs of FFE, the INL specification may be violated in 16% and 4% input codes, respectively, after 10 years. In addition, in less than 10 years, any input code between 32 to 41 can cause non-monotonicity, a highly undesirable property in control loops in the IDAC (Fig. 6(c)). For input codes distributed between 32 to 41, non-monotonicity is induced in the IDAC in 5.82 years. Hence, the impact of aging on performance degradation of a current-switching DAC is very sensitive to its operating region.

**FFE Analysis:** We use current-switching DACs in a 3-tap FFE with a precursor, a main cursor, and a postcursor, where the tap adaptation range of precursor, main cursor and the postcursor are 16, 64, and 32, respectively (i.e., the coefficients have 4, 6, and 5 bits, respectively). The channel is modeled as a 12" desktop backplane [14]. The tap coefficients, $\mathbf{C}$ (Eq. (23)) are generated using the MMSE algorithm by the CG module on the Rx side. The CUM receives $\mathbf{C}$ for all taps from the Rx side and sets these as the IDAC input codes.

Our SPICE simulations show that if the main cursor is stressed with equalization coefficients of 15 GHz frequency with 15% variation, an |INL| $\geq$ $\frac{1}{2}$LSB is induced in 10 years (Fig. 7(a)), and DNL drift over time can lead to non-monotonicity (Fig. 7(b)). During operation, each tap of the FFE is stressed differently as it operates with a different coefficient, with the main cursor carrying most of the current. Hence, the impact of aging varies across taps. Fig. 8 illustrates

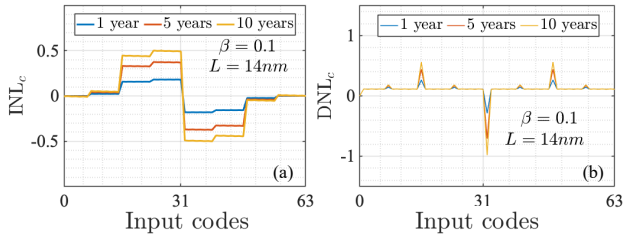


**Fig. 7.** Impact of aging on the main cursor of the FFE: (a) INL, (b) DNL.

aging effects on the IDACs in the 3-tap FFE after 10 years. Aging can cause (a) non-uniform gain among the IDACs of FFE (Fig. 8(a)) that can change effective equalization, (b) non-ideal DNL in the IDAC (Fig. 8(b)) that can result in large quantization error for some input codes, (c) non-monotonicity in the IDAC of main cursor (Fig. 8(c)) in the worst case that will hamper adaptive equalization scheme of the FFE.

Fig. 9 shows the impact of aging in IDACs of FFE on the eye-diagram of 15 GHz frequency. Due to the stress caused by different tap-coefficients, the transfer curve of each tap moves away from the ideal by different levels and with some nonlinearity, as illustrated in Fig. 8(a). As a consequence, quality of equalization for 15 GHz frequency degrades over time (Fig. 9(b)) causing 30% vertical eye width degradation, and 17% horizontal eye width degradation.

Our mitigation scheme is effective in countering FFE aging. The eye diagram (Fig. 9(c)) shows the eye to be as wide as the unaged circuit, and the bathtub curve (Fig. 9(d)) shows that after calibration, the BER improves back to the $t = 0$ level.

## VIII. Conclusion

This paper has presented an approach for modeling and analyzing the impact of mismatch in IDACs, and demonstrates its application to the analysis of aging in an FFE. A recalibration approach for aging is proposed, and is shown to enable recovery from aging-induced degradations in the eye diagram.

## Appendix

### A. Proofs of FFE Degradation Results

**Impact of Mismatch on Circuit Voltages** We first analyze the impact of aging-induced mismatch on IDAC performance. For a FinFET $M_{i,j}$, we denote the shift in threshold voltage due to time-dependent aging as $\Delta V_{th,M_{i,j}}$; similarly we define $\Delta V_{th,M_{ref}}$ for the reference transistor, $M_{ref}$. Thus, for any transistor $M_x$,

$$\Delta V_{th,M_x} = V_{th,M_x} - V_{th,\mu} \tag{32}$$

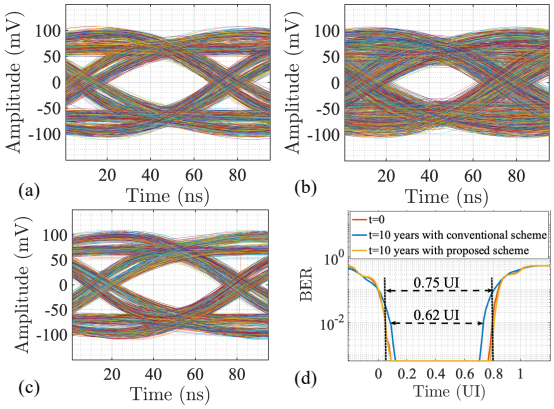


**Fig. 9.** Aging effects on eye diagram of HSLs: (a) at $t = 0$, (b) at $t = 10$ years with the conventional scheme, (c) at $t = 10$ years with the proposed scheme, (d) bathtub curve comparison in unit interval (UI).

where $V_{th,\mu}$ was defined earlier as the nominal threshold voltage. For a fixed $I_{in}$, as the diode-connected $M_{ref}$ is in saturation, any change in $V_{th}$ results in an equal rise in $V_b$:

$$V_{GS,M_{ref}} = V_{DS,M_{ref}} = V_b + \Delta V_{th,M_{ref}} \tag{33}$$

Combining this with Eq. (32), we have:

$$V_{GS,M_{ref}} - V_{th,M_{ref}} = V_b - V_{th,\mu} \tag{34}$$

For all FinFETs of an ON transistor $M_i$ (with $c_i = 1$),

$$V_{GS,M_{i,j}} = V_{GS,M_{ref}} \text{ and } V_{DS,M_{i,j}} = V_d \tag{35}$$

The latter relation arises because these FinFETs operate in the linear region, and $V_{th}$ shift has a negligible effect on the drain voltage. From Eqs. (32), (33), and (35),

$$\begin{aligned} V_{GS,M_{i,j}} - V_{th,M_{i,j}} &= (V_b + \Delta V_{th,M_{ref}}) - (V_{th,\mu} + \Delta V_{th,M_{i,j}}) \\ &= (V_b - V_{th,\mu}) + \Delta[M_{ref}, M_{i,j}] \end{aligned} \tag{36}$$

where $\Delta[M_{ref}, M_{i,j}]$ is the $V_{th}$ mismatch, as defined earlier.
Building upon the above ideas, we now present proofs of the results shown in Section III-B.

**FinFET transfer ratio:** When the FinFETs age nonuniformly, we combine Eqs. (6), (33), (34), (35), and (36), to obtain the the transfer ratio for FinFET $M_{i,j}$ as:

$$\mathcal{R}'_{i,j} = \left[1 + \frac{\Delta[M_{ref}, M_{i,j}]}{(V_b - V_{th,\mu})}\right]^{\alpha} \left[\frac{1 + \lambda V_d}{1 + \lambda(V_b + \Delta V_{th,M_{ref}})}\right]$$

Rearranging this and, for small perturbations, using a Taylor series approximation for the first term,

$$\mathcal{R}'_{i,j} = (1 + \alpha K_1 \Delta[M_{ref}, M_{i,j}]) \left[\frac{r}{1 + K_2 \Delta V_{th,M_{ref}}}\right] \tag{37}$$

$$\approx r\,(1 + \alpha K_1 \Delta[M_{ref}, M_{i,j}]) \tag{38}$$

Here, $r$ is as defined in Eq. (7), $K_1 = 1/(V_b - V_{th,\mu})$, $K_2 = \lambda/(1 + \lambda V_b)$, The last approximation arises by setting $r' = r/(1 + K_2 \Delta V_{th,M_{ref}}) \approx r$ because both $K_2$ and $\Delta V_{th,M_{ref}}$ are small. For a representative technology, $\lambda \approx 0.3$, $V_{th,\mu} \approx 0.35$, $V_b - V_{th}$ is 100mV$\sim$200mV, $\Delta V_{th} \sim$ 100mV. Thus, $K_2 \Delta V_{th,M_{ref}} \sim 0.026 \ll 1$.

From Eq. (7), $\Delta \mathcal{R}'_{i,j} = \alpha K_1 r \Delta[M_{ref}, M_{i,j}]$.

**Transfer ratio of bit $i$:** This is calculated as:

$$\begin{aligned} \mathcal{R}'_i &= \textstyle\sum_{j=0}^{2^i-1} \mathcal{R}'_{ij} = r \sum_{j=0}^{2^i-1} (1 + \alpha K_1 \Delta[M_{ref}, M_{i,j}]) \\ &= 2^i \cdot r + \alpha K_1 r \textstyle\sum_{j=0}^{2^i-1} \Delta[M_{ref}, M_{i,j}] \end{aligned} \tag{39}$$

Together with Eq. (8) for the ideal case, we obtain Eq. (16).

**Finding $I_{out}$:** From Eq. (1),

$$I'_{out} = I_{in} \textstyle\sum_{i=0}^{N-1} c_i \mathcal{R}'_i \tag{40}$$

Together with Eq. (9), we get Eq. (17). From Eq. (39), $I'_{out}$ is

$$\begin{aligned} &I_{in} \left(\textstyle\sum_{i=0}^{N-1} c_i 2^i r + \alpha K_1 \sum_{i=0}^{N-1} c_i r \sum_{j=0}^{2^i-1} \Delta[M_{ref}, M_{i,j}]\right) \\ &= I_{in} \left(c \cdot r + \alpha K_1 r \textstyle\sum_{i=0}^{N-1} c_i \sum_{j=0}^{2^i-1} \Delta[M_{ref}, M_{i,j}]\right) \end{aligned} \tag{41}$$

**Gain:** We set $c_i = 1\ \forall\ i$ in (40) to obtain the gain as:

$$G' = \frac{I_{FS}}{2^N - 1} = \frac{I_{in}}{2^N - 1} \textstyle\sum_{i=0}^{N-1} \mathcal{R}'_i \tag{42}$$

Combined with Eq. (10), we obtain Eq. (18).

**DNL:** Under variations, from Eqs. (11) and (41):

$$\begin{aligned} \text{DNL}_c &= (I_c - I_{c-1}) - r \cdot I_{in} \\ &= \alpha K_1 r I_{in} \left(\textstyle\sum_{i=0}^{N-1} c_i \sum_{j=0}^{2^i-1} \Delta[M_{ref}, M_{i,j}] - \right. \\ &\qquad \left. \textstyle\sum_{i=0}^{N-1} (c-1)_i \sum_{j=0}^{2^i-1} \Delta[M_{ref}, M_{i,j}]\right) \end{aligned} \tag{43}$$

$$= I_{in} \textstyle\sum_{i=0}^{N-1} [c_i - (c-1)_i]\, \Delta \mathcal{R}'_i \tag{44}$$

**INL:** Using Eqs. (12) and (41):

$$\begin{aligned} \text{INL}_c &= I_c - c \cdot r \cdot I_{in} \\ &= \alpha K_1 r I_{in} \left(\textstyle\sum_{i=0}^{N-1} c_i \sum_{j=0}^{2^i-1} \Delta[M_{ref}, M_{i,j}]\right) \end{aligned} \tag{45}$$

$$= I_{in} \textstyle\sum_{i=0}^{N-1} c_i \Delta \mathcal{R}'_i \tag{46}$$

### *B. Calibrating Gain of IDAC*

Comparing Eq. (42) with (10), $G' > G$ as $\mathcal{R}'_i > \mathcal{R}_i$. In this case, $\Delta G$, DNL$_c$, and INL$_c$ can be calculated using Eq. (18), (19), and (20) respectively. To set $G' = G$, $I_{in}$ can be calibrated to $I'_{in}$ such that:

$$\sum_{i=0}^{N-1} I'_{in} \mathcal{R}'_i = \sum_{i=0}^{N-1} I_{in} \mathcal{R}_i \Longrightarrow \frac{I'_{in}}{I_{in}} = \frac{\sum_{i=0}^{N-1} \mathcal{R}_i}{\sum_{i=0}^{N-1} \mathcal{R}'_i} \tag{47}$$

For a current-steering DAC, all $M_{i,j}$ face identical stress condition: $V_{GS,M_{i,j}} = V_b$, and $V_{DS,M_{i,j}} = V_d$. This causes an identical mismatch, $\Delta[M_{ref}, M_{i,j}]$, hence identical $\mathcal{R}'_{i,j}$ as a consequence (Eq. 38) in all $M_{i,j} \forall 0 \le i < N, 0 \le j < 2^i$. From Eq. (47), $G'$ can be set to $G$ in a current-steering DAC by recalibrating $I'_{in}$ as following:

$$\frac{I'_{in}}{I_{in}} = \frac{(2^N - 1) \cdot \mathcal{R}_{i,j}}{(2^N - 1) \cdot \mathcal{R}'_{i,j}} \Longrightarrow I'_{in} = \frac{r \cdot I_{in}}{\mathcal{R}'_{i,j}} \tag{48}$$

After such recalibration in a current-steering DAC, DNL$_c$ and INL$_c$ for any $c$ also go to zero:

$$\begin{aligned} \text{DNL}_c &= (I_c - I_{c-1}) - r \cdot I_{in} = \mathcal{R}'_{i,j}.I'_{in} - r \cdot I_{in} = 0 \\ \text{INL}_c &= I_c - c \cdot r \cdot I_{in} = c \cdot \mathcal{R}'_{i,j}.I'_{in} - c \cdot r \cdot I_{in} = 0 \end{aligned}$$

In a current-switching DAC, stress condition of each $M_i$ varies depending on $c_i$ (Section II). Hence, $\mathcal{R}'_{i,j}$ corresponding to each $M_i, 0 \le i < N$ can be different. As a consequence, tuning $I_{in}$ to $I'_{in}$ to set $G' = G$ in a current-switching DAC may not set DNL$_c$ and INL$_c$ to zero for all $c$.

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