POWER ESTIMATION CONSIDERING STATISTICAL IC PARAMETRIC VARIATIONS

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ABSTRACT

Statistical perturbations of process parameters may change propagation delays and alter the switching activity in the circuit due to glitches. In this paper, the problem of estimating glitch/hazard power in CMOS circuits is addressed. A probabilistic min/max delay model is used, where the variation of delays between the minimum and maximum delay may follow any given discrete probability distribution. The first part of this work considers glitching activity assuming fixed gate delays with instantaneous rise/fall times. Next, this is refined to incorporate the effects of fixed transition times. Experimental results on benchmark circuits show that a significant amount of power is dissipated in hazards and glitches and that the hazardous part of power dissipation is sensitive to variations in gate delays.

1. INTRODUCTION

Low power, yet high throughput and computationally intensive circuits are becoming a critical application domain. An important prerequisite of low power design is accurate power estimation and as a result, several researchers have addressed the issue of power estimation in the recent years. A direct and simple approach to estimate power is to simulate the circuit for all possible input vectors, called exhaustive simulation. However, such a technique cannot be used to simulate long-enough input vector sequences to get meaningful power estimates. A Monte Carlo simulation based technique was proposed in [1]. In this technique, the circuit is simulated for a large number of input vectors while gathering statistics on the average power. However, it is based on the assumption that the average power is distributed normally over a finite time. Recently, other approaches have been proposed [2], [3] that require the user to specify typical behavior at the circuit inputs using probabilities. These techniques, referred to as probability-based techniques, are weakly pattern dependent and allow the user to cover a large set of possible input patterns with little effort. Hence, these techniques are much more time efficient than other approaches. In [4], a real delay model is used to correctly compute Boolean conditions that cause glitching, taking into account correlations due to reconvergence fanout. This procedure is exact but suffers from excessive computation time and storage space. In [5], an efficient but approximate tagged probabilistic simulation approach that accounts for reconvergent fanout and glitches is described.

However, none of the above techniques take into account the variation in switching activity due to variations in delay values. It has been shown in [6] that an average of 15-20% (in some cases, upto 70%) of the total power is dissipated in glitching. It was also shown in [6] that the hazardous component of power dissipation is more sensitive to IC parameter fluctuations than the power strictly required to perform the transition between the initial and final state of each node. It is therefore useful to determine the change in the switching activity as a function of these statistical perturbations.

This work presents a technique to probabilistically estimate switching activity of individual gates in combinational CMOS circuits and that due to hazards, taking into account statistical perturbations in delay parameters. Signal and transition probabilities are calculated using, both, a zero-delay model and a real-delay model. The zero-delay model gives an estimate of switching activity due to only essential transitions in the circuit while the real-delay model gives estimates of both essential and spurious (hazards/glitches) transitions in the circuit. A min/max delay model is used by which the gate delays are uncertain but specified to be lying between d_{min} and d_{max}. The difference in the number of transitions from the two models gives an estimate of hazards/glitches in the circuit. The technique is proposed in two parts. The first part assumes zero rise/fall-time delays, while the second part considers rise/fall-time delays to account for transitions that do not cause a full voltage swing of V_{dd} at the output. The technique assumes that there is no correlation between the internal lines of the circuit. The complexity of the power estimation algorithm presented is linear in the number of gates in the circuit.

The rest of the paper is organized as follows. In Section 2, we review the notions of signal and transition probabilities and describe the delay and power consumption models. Section 3 describes the power estimation algorithm when neglecting transition times. In Section 4, the algorithm is extended to account for finite transition times. Experimental results and conclusions are presented in Sections 4 and 5 respectively.

2. BACKGROUND AND TERMINOLOGY

- *Signal probability* of a node is defined as the probability of the signal being logic ONE at time t and is denoted by $p^{one}(t)$. Similarly, the probability of a signal being logic ZERO is denoted by $p^{zero}(t)$ and is equal to $(1 - p^{one}(t))$.
- *Transition probability* of a node is the probability of the signal making a transition from one state to another at any time t and is denoted by $p^{ab}(t)$, where $(a, b) \in (0, 1)$.
- $[d_{min}, d_{max}]$: The delay d of a gate is defined as the time taken to reach 50% of its output value. Gate

delays are uncertain but specified to lie between d_{min} and d_{max}.

- *Power dissipation model*: A dominant source of power dissipation in CMOS circuits is due to the charging and discharging of the node capacitances and is given by [4]:

$$P_{avg} = 0.5 \cdot C_{load} \cdot (\frac{V_{dd}^2}{T_{cyc}}) \cdot E(transitions) \quad (1)$$

where P_{avg} denotes the average power, C_{load} is the load capacitance, T_{cyc} is the global clock period, V_{dd} is the supply voltage and $E(transitions)$ is the *expected value* of the number of gate output transitions per global clock cycle.

3. POWER ESTIMATION NEGLECTING RISE-/FALL-TIME DELAYS

Given a combinational circuit with uncorrelated primary inputs and no reconvergent fanout, assume all input nodes to be stable before applying transitions at the primary inputs. If the transition probabilities at the primary inputs at time $t = 0$ are specified, a simulation approach based on the Critical Path Method (CPM) is used to propagate these probabilities through the circuit: When a probabilistic event occurs at the inputs to some gate g, the appropriate event (shifted by an amount equal to the gate delay and with corresponding signal and transition probabilities) is created at the output of g.

The signal probabilities at $t = 0^-$ at the primary inputs are computed using the transition probabilities at the primary inputs at $t = 0$ as follows:

$$p^{one}(t = 0^-) = p^{10}(t = 0) + p^{11}(t = 0)$$
$$p^{zero}(t = 0^-) = p^{01}(t = 0) + p^{00}(t = 0)$$

Similarly the signal probabilities at $t = 0^+$ are given by,

$$p^{one}(t = 0^+) = p^{01}(t = 0) + p^{11}(t = 0)$$
$$p^{zero}(t = 0^+) = p^{10}(t = 0) + p^{00}(t = 0)$$

The initial conditions at other nodes in the circuit at $t = 0^-$ are calculated assuming a zero-delay model. We illustrate this using an AND gate. Similar results can be derived for other types of gates such as OR, NAND, NOR, NOT, BUFFER. Consider a gate with k inputs, $x_1, \cdots, x_k$ and an output y. The signal probability of y at $t = 0^-$ is found using the signal probabilities at its inputs at $t = 0^-$, as shown:

$$\text{AND gate: } p_y^{one}(t = 0^-) = \prod_{i=1}^{k} p_{x_i}^{one}(t = 0^-)$$

3.1. Propagation of Transition Probabilities

3.1.1. Estimation using Zero-Delay Model

With this information, the signal and transition probabilities are determined using a zero-delay model for the gates. These transition probabilities give an estimate of only the steady-state transitions at output nodes in the circuit due to transitions at the primary inputs. The signal probability of a gate is derived from its Boolean function. Thus, the probability of a *one* at the output of an AND gate is equal to the probability of a *one* at each of its inputs, in other words, the *intersection* of the signal probabilities of each of its inputs, assuming the inputs to be independent.

Hence we can write:

$$\text{AND gate: } p_y^{one}(t = 0) = \prod_{i=1}^{k} p_{x_i}^{one}(t = 0)$$

The output y of an AND gate will have a $(0 \rightarrow 1)$ transition at time t, if one or more of its inputs has a $(0 \rightarrow 1)$ transition and the others have a signal value equal to 1 at time $t = 0^+$. This can be expressed as follows:

$$p_y^{01}(t = 0) = \sum_{j=1}^{k} \sum_{S_j \subseteq (1,2 \cdots k)} (-1)^{j-1} \prod_{i \in S_j} p_{x_i}^{01}(t = 0) \prod_{\substack{l=1, \\ l \neq S_j}}^{k} p_{x_l}^{one}(t = 0^+)$$

Similarly,

$$p_y^{10}(t = 0) = \sum_{j=1}^{k} \sum_{S_j \subseteq (1,2 \cdots k)} (-1)^{j-1} \prod_{i \in S_j} p_{x_i}^{10}(t = 0) \prod_{\substack{l=1, \\ l \neq S_j}}^{k} p_{x_l}^{one}(t = 0^-)$$

3.1.2. Estimation using Real-Delay Model

To determine the switching activity due to both essential and spurious transitions in the circuit, the calculations for probabilities are carried out again using a real-delay model. Prior to this, the transition time points of each gate in the circuit and the longest path delay of the circuit are determined, using CPM. In other words, it is used to determine the time intervals during which there is switching activity for each node in the circuit. Transition probabilities are computed only during these intervals, thereby reducing the number of computations to be performed in calculating switching activity of the circuit. We use the *min/max* delay model by which the gate delays are uncertain but specified to be varying from d_{min} to d_{max}. The distribution of delay values is assumed to be *binomial*. Hence the probability of the delay of the gate being d is given by the following formula [7]:

Let $\Delta = d_{max} - d_{min} + 1$, then the probability, $P(d)$, of the delay of a gate being d is given by,

$$P(d) = \frac{^{\Delta-1}C_{d-d_{min}}}{2^{\Delta-1}} \quad (2)$$

For a k-input AND gate, the signal probability at the output of the gate is equal to the product of the probability of the delay being d and the *intersection* of the signal probabilities of each of its inputs shifted by an amount equal to the delay of the gate. The total signal probability of the gate at each time instant is equal to the sum of the signal probabilities for each of the delays in the range $[d_{min}, d_{max}]$.

Thus,

$$\text{AND gate: } p_y^{one}(t) = \sum_{d=d_{min}}^{d=d_{max}} P(d) \times (\prod_{i=1}^{k} p_{x_i}^{one}(t - d)),$$

Similarly, the transition probabilities are found taking the delay effects into account. The expressions for the transition probabilities for an AND gate, in this case, will be:

$$p_y^{01}(t) = \sum_{d=d_{min}}^{d=d_{max}} P(d) \times (\sum_{j=1}^{k} \sum_{S_j \subseteq (1,2 \cdots k)} (-1)^{j-1} \prod_{i \in S_j} p_{x_i}^{01}(t - d)$$

$$\prod_{\substack{l=1,\\ l\neq S_j}}^{k} p_{x_l}^{one}((t-d)^{+}))$$

$$p_y^{10}(t) = \sum_{d=d_{max}}^{d=d_{min}} P(d) \times (\sum_{j=1}^{k} \sum_{S_j \subseteq (1,2\cdots k)} (-1)^{j-1} \prod_{i \in S_j} p_{x_i}^{10}(t-d) \prod_{\substack{l=1,\\ l\neq S_j}}^{k} p_{x_l}^{one}((t-d)^{-}))$$

3.2. Power Estimation using Transition Probabilities

The total switching activity for one clock cycle for each of the gates in the circuit is the sum of transition probabilities (p_{01} and p_{10}) at each time t, that it was simulated for. Thus,

$$E_g[transitions] = \sum_{t=0}^{MaxDly} [p_{01}[t] + p_{10}[t]]$$

where $MaxDly$ is the longest possible path delay of the circuit and is calculated using CPM.

The difference in $E_g[transitions]$ obtained from the zero-delay and real-delay model, gives $E_g[transitions]$ due to hazards/glitches at that gate. Consequently, the average power dissipated by spurious transitions in the circuit is given by:

$$P_{avg} = 0.5 \cdot V_{dd}^2 \cdot f_{clk} \sum_{\forall gates,g} (C_{load_g} \cdot E_g[transitions]) \quad (3)$$

4. POWER ESTIMATION CONSIDERING FINITE RISE-/FALL-TIME DELAYS

The algorithm presented in Section 3 assumes that all transitions propagated to the outputs of nodes cause a full voltage swing of V_{dd} when the load capacitances switch. However, if we consider finite rise/fall-time delays, multiple transitions at outputs, spaced less than transition delay apart, will not cause a complete voltage swing of V_{dd}. As a result, the power consumed by such transitions will be less than that obtained by using (1) which assumes a full voltage swing of V_{dd} for all transitions.

To correct for the error due to neglecting finite transition times in the power estimation technique proposed earlier, we developed a method for measuring the widths (in terms of time) of high and low transitions and approximating it to the fraction of the output voltage, V, that it would charge/discharge the capacitances to.

4.1. Factors Causing Multiple Transitions

Conditions that cause multiple transitions depend on the type of the gate. The only kind of hazard possible for an AND gate is a static 0-hazard . This occurs when one or more inputs of the AND gate make a $(0 \rightarrow 1)$ transition first and one or more inputs make a $(1 \rightarrow 0)$ transition after a time δ, while all other inputs remain at a constant one. Since we assume the inputs to be independent, both temporally and spatially, the probability of such a transition occurring, which we define as *spikes*, is as follows (for a two-input AND gate):

$$pspike_g = p_1^{01}[t] \cdot p_2^{10}[t+\delta],$$

where δ varies from one to $2d$, and d is gate delay.

For a k-input gate,

$$pspike_\delta = \prod p_{x_i}^{01}[t] \prod_{j \neq i} p_{x_j}^{10}[t+\delta] \prod_{l \neq i,j} p_{x_l}^{11}[t],$$

where $(i,j,l) \in inputs$.

4.2. Calculation of Power Dissipated by the Spikes

The probability of a *spike* is calculated for each time instant in the switching time interval of a gate. The output voltage is approximated from the width of the spike, δ, and the delay of the gate, d, using the formula, $V_\delta = \frac{V_{dd} \times \delta}{2 \cdot d}$ and substituted in the power dissipation expression,

$$P_{spike} = C_{load} \cdot V_{dd} \cdot f_{clk} \cdot \sum_{d=d_{min}}^{d=d_{max}} P(d) \times (\sum_{\delta=1}^{lai} V_\delta \cdot pspike_\delta),$$

to get the total power dissipated by spikes at gate g at each time instance in its switching interval. Here the terms C_{load}, V_{dd} are the same as in (1).

If these transitions were assumed to cause a full voltage swing of V_{dd}, the power consumed by these transitions will be,

$$P_{prev} = C_{load} \cdot V_{dd}^2 \cdot f_{clk} \cdot \sum_{d=d_{min}}^{d=d_{max}} P(d) \cdot pspike_\delta \quad (4)$$

Hence, the corrected power, $P = P_{avg} + P_{spike} - P_{prev}$, where P_{avg} is the power estimate obtained in Section 3.

Table 1. Comparison of results from MCS and Glitch neglecting transition delays ($t(s)$ is the CPU time in seconds)

	Real-Delay				Hazards	
	MCS		Glitch		MCS	Glitch
Ckt	*t(s)*	*pwr*	*t(s)*	*pwr*	*pwr*	*pwr*
c17	22	2.20	0.004	2.20	0.39	0.4
cm42a	152	4.15	0.07	4.20	1.27	1.09
ccmap	393	10.96	0.109	10.94	1.66	1.58
b9map	1398	9.68	0.473	9.75	1.68	1.77
9symm	2725	15.45	0.010	14.51	4.96	4.16
alu2	-	-	0.54	9.17	-	4.06
alu4	-	-	0.59	19.77	-	9.65
c3540	-	-	0.66	59.83	-	38.10

Table 2. Comparison of MCS and Glitch results for finite transition delays

	Real-Delay				Hazards	
	MCS		Glitch		MCS	Glitch
Ckt	*t(s)*	*pwr*	*t(s)*	*pwr*	*pwr*	*pwr*
c17	694	1.98	0.01	2.0	0.17	0.19
cm42a	4275	3.82	0.21	3.99	0.94	0.87
ccmap	56937	10.34	0.15	10.37	1.04	0.99
b9map	47927	9.12	0.22	10.8	1.95	1.42
9symm	169258	13.98	0.191	13.47	3.49	3.11

5. EXPERIMENTAL RESULTS

Power estimates from the proposed algorithm were verified with the results obtained from a 32-bit simulator based on

the Monte-Carlo approach. This approach simulates the circuit for different input patterns until convergence occurs, to estimate signal and transition probabilities. The proposed algorithm was implemented on DEC 3000 workstations. Experiments were conducted on ISCAS '85 and Logic Synthesis '91 benchmark circuits. In Table 1, results of the proposed power estimator (Glitch) assuming negligible rise/fall-time delays are compared with those obtained from Monte-Carlo simulation model (MCS). For both the models, the capacitance at each node is taken to be equal to the fanout of the node. Hence the actual power consumed will be proportional to the results shown as *pwr* in the tables. Results for blank entries in the table could not be obtained due to large computation times. The percentage error in power estimates from MCS and Glitch is on an average, 6.74%, which is negligible when compared to the speedup obtained.

Table 3. Percentage variation in Totalpower vs percentage variation in Hazardpower

	Delay Variations					
	10%		20%		40%	
Ckt	P_{tot}	P_{hz}	P_{tot}	P_{hz}	P_{tot}	P_{hz}
cm42a	2.4	23.1	1.47	28.65	21.17	58.37
9symm	0.42	14.9	0.43	15.0	24.0	41.1
alu2	2.96	18.24	1.42	19.8	40.2	64.67
alu4	0.94	16.53	3.51	17.94	23.96	45.0

Though the ratio between the hazard power and total power varies significantly with the considered circuits (14% to 48%), the average power dissipated by hazards/glitches in static CMOS circuits is 24.95%. These results show that a significant amount of power dissipation in static CMOS circuits is due to glitches/hazards and hence cannot be neglected.

Table 2 compares the results of Glitch, when it considers rise/fall-time delays with the results from MCS. With only a slight increase in computation time, this technique gives more accurate power estimates. Power estimates for all the circuits using this technique are less than those obtained with negligible rise/fall-time assumption as expected.

Table 3 shows the percentage variation in total power dissipated (P_{tot}) and power consumed by hazards (P_{hz}) as the percentage variation in delay is varied. The percentage variations in power (total and hazard) were calculated with respect to power when the gate delay is fixed (that is delay variation is 0%). It can be seen that the percentage variation in hazards is higher than the percentage variation in total power dissipation. These results prove that statistical variations in delay values cause variations in hazard power dissipation and, in fact, the hazardous component of power is more sensitive to these variations than total power dissipated.

6. CONCLUSIONS

We presented a linear-time, probability-based algorithm for estimating glitch/hazard power in CMOS combinational circuits, taking into account statistical perturbations in delay parameters. Experimental results show that an average of 28% of total power dissipated is due to hazards/glitches. It was also found that, in general, the hazardous part of power dissipation is more sensitive to variations in gate delays than total power dissipation. Since this algorithm assumes fixed gate delays with instantaneous rise/fall times, it is extended to incorporate the effects of fixed transition times approximately. The difference between the MCS and Glitch results is small enough to show that this is a reasonable approximation that can be obtained with considerable amount of speed-up over other more exhaustive simulations.

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